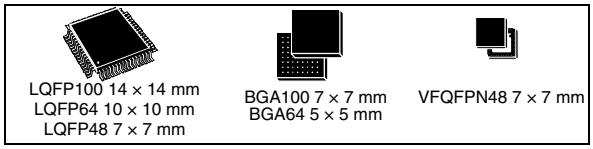
STM32L151xx
STM32L152xx

Ultralow power ARM-based 32-bit MCU with up to 128 KB Flash, RTC, LCD, USB, USART, I2C, SPI, timers, ADC, DAC, comparators

Data brief

Features

- Operating conditions
  - Operating power supply range: 1.65 V to 3.6 V (without BOR) or 1.8 V to 3.6 V (with BOR option)
  - Temperature range: –40 to 85 °C
- Low power features
  - 7 modes: Sleep, Low-power run (10.4 µA at 32 kHz), Low power sleep (5.1 µA), Stop with RTC (1.3 µA), Stop (0.5 µA), Standby with RTC (1 µA), Standby (0.27 µA)
  - Dynamic core voltage scaling down to 230 µA/MHz (from Flash)
  - Ultralow leakage per I/O: 50 nA
  - Three wakeup pins
- Core: ARM 32-bit Cortex™-M3 CPU
  - 32 MHz maximum frequency, 33.3 DMIPS peak (Dhrystone 2.1)
  - Memory protection unit
- Reset and supply management
  - Low power, ultrasafe BOR (brownout reset) with 5 selectable thresholds
  - Ultralow power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 1 to 24 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 16 MHz factory-trimmed RC
  - Internal 37 kHz low consumption RC
  - Internal multispeed low power RC, 64 kHz to 4.1 MHz with a consumption down to 1.5 µA
  - PLL for CPU clock and USB (48 MHz)
- Low power calendar RTC
  - Alarm, periodic wakeup from Stop/Standby
- Memories
  - Up to 128 Kbyte of Flash memory with ECC
  - 4 Kbyte of data EEPROM with ECC



  - Up to 16 Kbyte of RAM
- Up to 83 fast I/Os (73 of which are 5 V-tolerant) all mappable on 16 external interrupt vectors
- Development support
  - Serial wire debug, JTAG and trace
  - Readout protection and JTAG fuse
- DMA: 7-channel DMA controller, supporting timers, ADC, SPIs, I^2Cs and USARTs
- LCD 8 × 40 or 4 × 44 with step-up converter
- 12-bit ADC up to 1 Msps/24 channels
  - Temperature sensor and internal voltage reference
  - Operates down to 1.8 V
- 2 × 12-bit DACs with output buffers
- 2 ultralow power comparators
  - Window mode and wakeup capability
- 10 timers:
  - 6 × 16-bit general-purpose timers, each with up to 4 IC/OC/PWM channels
  - 2 × 16-bit basic timers
  - 2 × watchdog timers (independent and window)
- Up to 8 communication interfaces
  - Up to 2 × I^2C interfaces (SMBus/PMBus)
  - Up to 3 × USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 2 × SPIs (16 Mbit/s)
  - USB 2.0 full-speed interface
- CRC calculation unit, 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32L151xx	STM32L151CB, STM32L151RB, STM32L151VB, STM32L151C8, STM32L151R8, STM32L151V8
STM32L152xx	STM32L152CB, STM32L152RB, STM32L152VB, STM32L152C8, STM32L152R8, STM32L152V8

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151xx and STM32L152xx ultralow power ARM Cortex™-based microcontrollers product line.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the *www.arm.com* website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2 Description

The ultralow power STM32L15xxx incorporates the connectivity power of the universal serial bus (USB) with the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 16 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer a 12-bit ADC, 2 DACs and 2 ultralow power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases. Moreover, the STM32L15xxx devices contain standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs and a USB. They also include a real-time clock and a set of backup registers that remain powered in Standby mode. Finally, the integrated LCD controller has a built-in LCD voltage generator that allows you to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultralow power STM32L15xxx operates from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. It is available in the -40 to +85 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications. The ultralow power STM32L15xxx family includes devices in 3 different package types: from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultralow power STM32L15xxx microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

Figure 1 shows the general block diagram of the device family.

2.1 Device overview

Table 2. Ultralow power STM32L15xxx device features and peripheral counts

Peripheral		STM32L15xCx		STM32L15xRx		STM32L15xVx	
Flash - Kbytes		64	128	64	128	64	128
RAM - Kbytes		10	16	10	16	10	16
Timers	General-purpose	6		6		6	
	Basic	2		2		2	
Communication interfaces	SPI	2		2		2	
	I^2C	2		2		2	
	USART	3		3		3	
	USB	1		1		1	
GPIOs		37		51		80	
12-bit synchronized ADC Number of channels		1 16 channels		1 20 channels		1 24 channels	
12-bit DAC Number of channels		2 2		2 2		2 2	
LCD (STM32L152xx Only) COM x SEG		4x16		4x32 8x28		4x44 8x40	
Comparator		2		2		2	
CPU frequency		32 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V (down to 1.65 V at power-down) without BOR option					
Operating temperatures		Ambient temperatures: –40 to +85 °C Junction temperature: –40 to + 105 °C					
Packages		LQFP48, VFQFN48		LQFP64, BGA64		LQFP100, BGA100	

2.2 Ultralow power device continuum

The ultralow power STM32L151xx and STM32L152xx are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultralow power strategy which also includes STM8L101xx and STM8L15xx devices. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture and features.

They are all based on STMicroelectronics 0.13 µm ultralow leakage process.

Note: The ultralow power STM32L and general-purpose STM32Fxxxx families are pin-to-pin compatible. The STM8L15xxx devices are pin-to-pin compatible with the STM8L101xx devices. Please refer to the STM32F and STM8L documentation for more information on these devices.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex™-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultralow power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L15xxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC, and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xx and STM32L15xx families use a common architecture:

- Same power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xx devices)
- Architecture optimized to reach ultralow consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

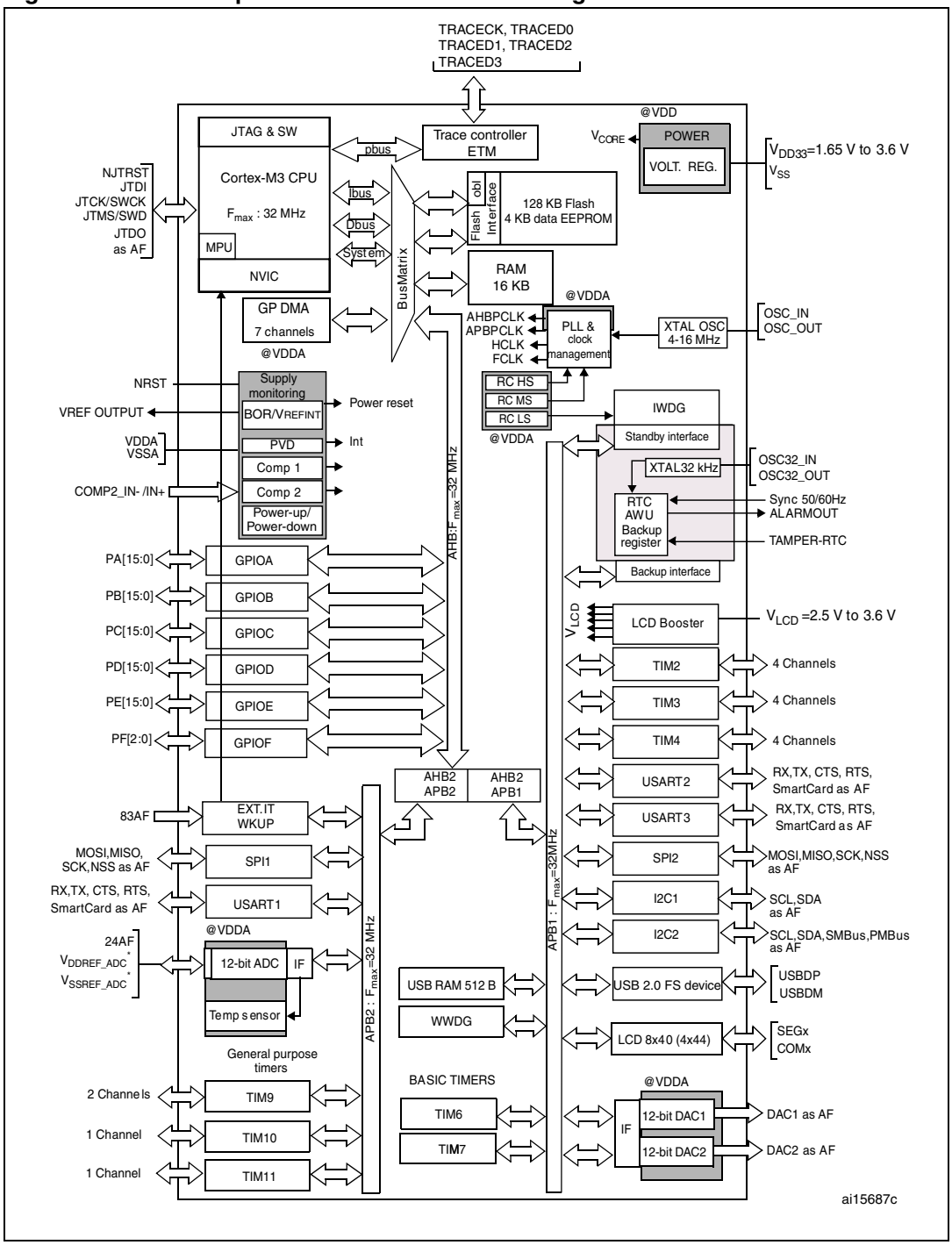
ST ultralow power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbytes

3 Functional overview

Figure 1 shows the block diagrams.

Figure 1. Ultralow power STM32L15xxx block diagram



1. T_A = –40 °C to +105 °C (junction temperature up to 125 °C).
2. AF = alternate function on I/O port pin.

3.1 Low power modes

The ultralow power STM32L15xxx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply. When executing from Flash memory, the consumptions are:

- In range 1 (V_{DD} range limited to 2.0-3.6 V), with the CPU running at up to 32 MHz, the consumption is: 290 µA/MHz
- In range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz, the consumption is: 265 µA/MHz
- In range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4 MHz (generated only with the multispeed internal RC oscillator clock source), the consumption is: 230 µA/MHz.

Seven low power modes are provided to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. The Sleep mode power consumption at 16 MHz is of about 2.5 mA with all peripherals on, and of 650 µA with all peripherals off.

- **Low power run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (64 kHz), execution from SRAM or Flash memory, and internal regulator in low power mode to minimize the regulator's operating current. In the Low power run mode, the clock frequency and the number of enabled peripherals are both limited.

  The Low power run mode consumption can be as low as 10.4 µA when executing code from RAM at 32 kHz.

- **Low power sleep** mode

  This mode is achieved by entering the Sleep mode with the internal voltage regulator in Low power mode to minimize the regulator's operating current. In the Low power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on. The Low power sleep mode consumption is as low as 5.1 µA when no peripheral is enabled. It is of 6.1 µA with one timer operating at 32 kHz.

- **Stop** mode (with or without RTC)

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks in the 1.8 V domain are stopped, the PLL, HSI RC and HSE crystal oscillators are disabled. The voltage regulator is in the low power mode. The device can be woken up from the Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup. The Stop mode consumption with the RTC on the LSE is of 1.3 µA (at 1.8 V) and 1.6 µA (at 3.0 V). The Stop mode consumption without the RTC is of 0.5 µA.

- **Standby** mode (with or without RTC)

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, HSI RC and HSE crystal oscillators are also switched off. After entering Standby

mode, the RAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits the Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins or an RTC alarm occurs. The Standby mode consumption is of 1µA (at 1.8 V) and 1.3 µA (at 3.0 V) with the RTC on, and of 270 nA with the RTC off.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

3.2 ARM® Cortex™-M3 core with MPU

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L15xxx is compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultralow power STM32L15xxx embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

For devices operating between 1.8 and 3.6 V, the BOR is always active at power-on and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V). Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms.
For devices operating between 1.65 V and 3.6 V, the BOR is permanently disabled.
Consequently, the start-up time at power-on can be decreased down to 1ms typically.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and RAM are lost)

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. For further details please refer to AN2606.

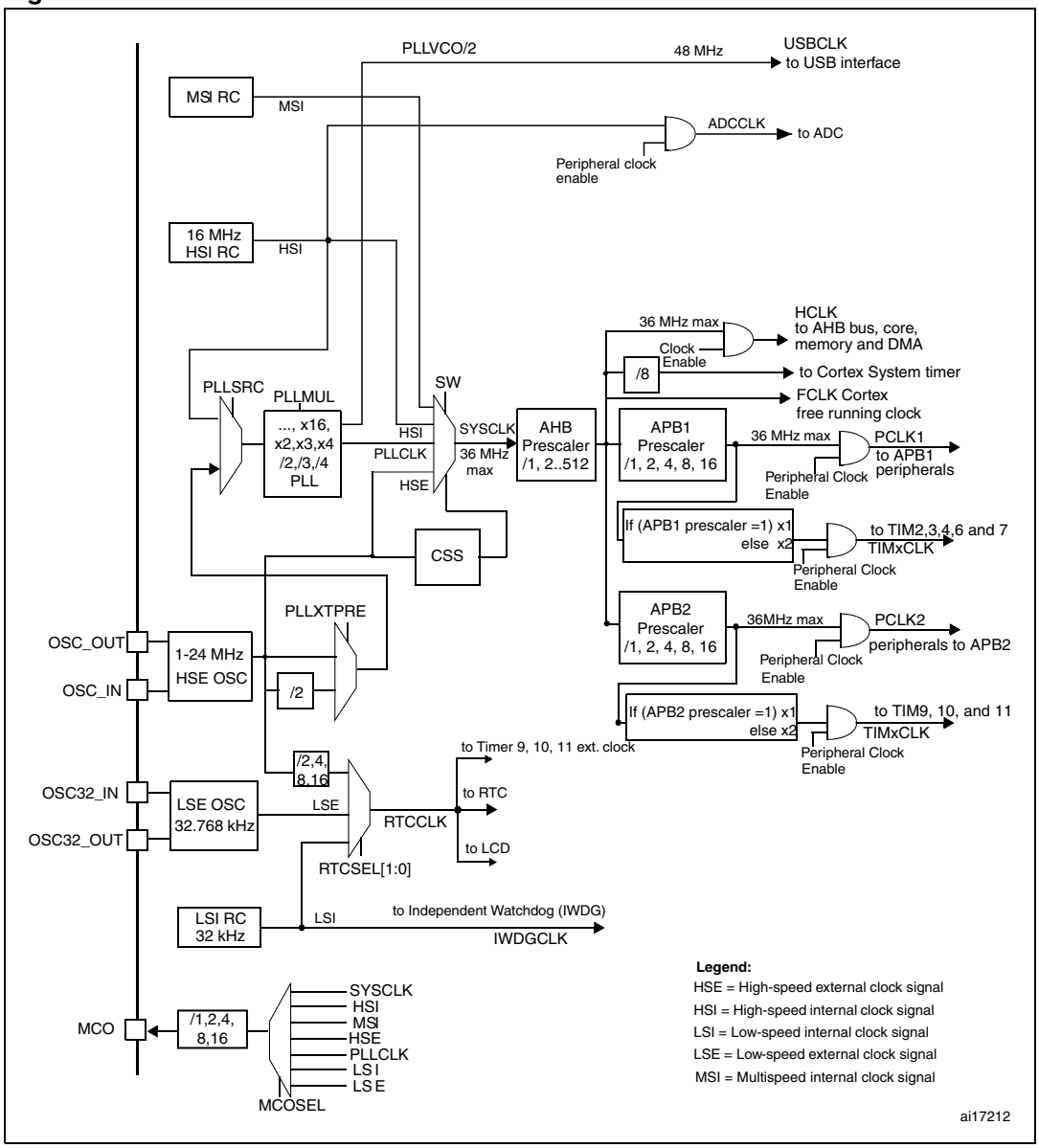
3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best tradeoff between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock source**: three different clock sources can be used to drive the master clock:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (64 kHz, 128 kHz, 256 kHz, 512 kHz, 1.02 MHz, 2.05 MHz, 4.1 MHz) with a consumption proportional to speed, down to 1.5 µA typical. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultralow power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Configurable main clock output (CCO):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Figure 2. Clock tree



3. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 24 MHz or 32 MHz.
4. To have an ADC conversion time of 1 µs, APB2 must be at 16 MHz.

3.5 Low power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made

automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop capability.

- The programmable wakeup time ranges from 62.5 µs to 18 hours
- Stop mode consumption with LSI and Auto-wakeup: 1.2 µA (at 1.8 V) and 1.4 µA (at 3.0 V)
- Stop mode consumption with LSE, calendar and Auto-wakeup: 1.3 µA (at 1.8V), 1.6 µA (at 3.0 V)

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

There are twenty 32-bit backup registers provided to store 80 bytes of user application data. They are cleared in case of tamper detection.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high-current-capable except for analog pins. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines.

3.7 Memories

The STM32L15xxx devices have the following features:

- Up to 16 Kbyte of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 64 or 128 Kbyte of embedded Flash program memory
  - 4 Kbyte of data EEPROM
  - Options bytes

  The options bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L15xxx devices with up to 24 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers.

The ADC includes a specific low power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.8 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in noninverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32L15xxx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultralow power comparators and voltage reference

The STM32L15xxx embeds two comparators sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low power / low current output buffer (driving current capability of 1 µA typical).

3.13 Routing interface

This interface controls the internal routing of I/Os to TIM2, TIM3, TIM4 and to the comparator and voltage reference output.

3.14 Timers and watchdogs

The ultralow power STM32L15xxx devices include six general-purpose timers, two basic timers and two watchdog timers.

Table 3 compares the features of the general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.14.1 General-purpose timers (TIM2, TIM3, TIM4, TIM9, TIM10 and TIM11)

There are six synchronizable general-purpose timers embedded in the STM32L15xxx devices (see *Table 3* for differences).

TIM2, TIM3, TIM4

These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM10, TIM11 and TIM9

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.14.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.14.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.15 Communication interfaces

3.15.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.15.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals. They support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

3.15.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

3.15.4 Universal serial bus (USB)

The STM32L15xxx embeds a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.16 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.17 Development support

Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L15xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

4 Pin descriptions

Figure 3. STM32L15xxx UFBGA100 ballout

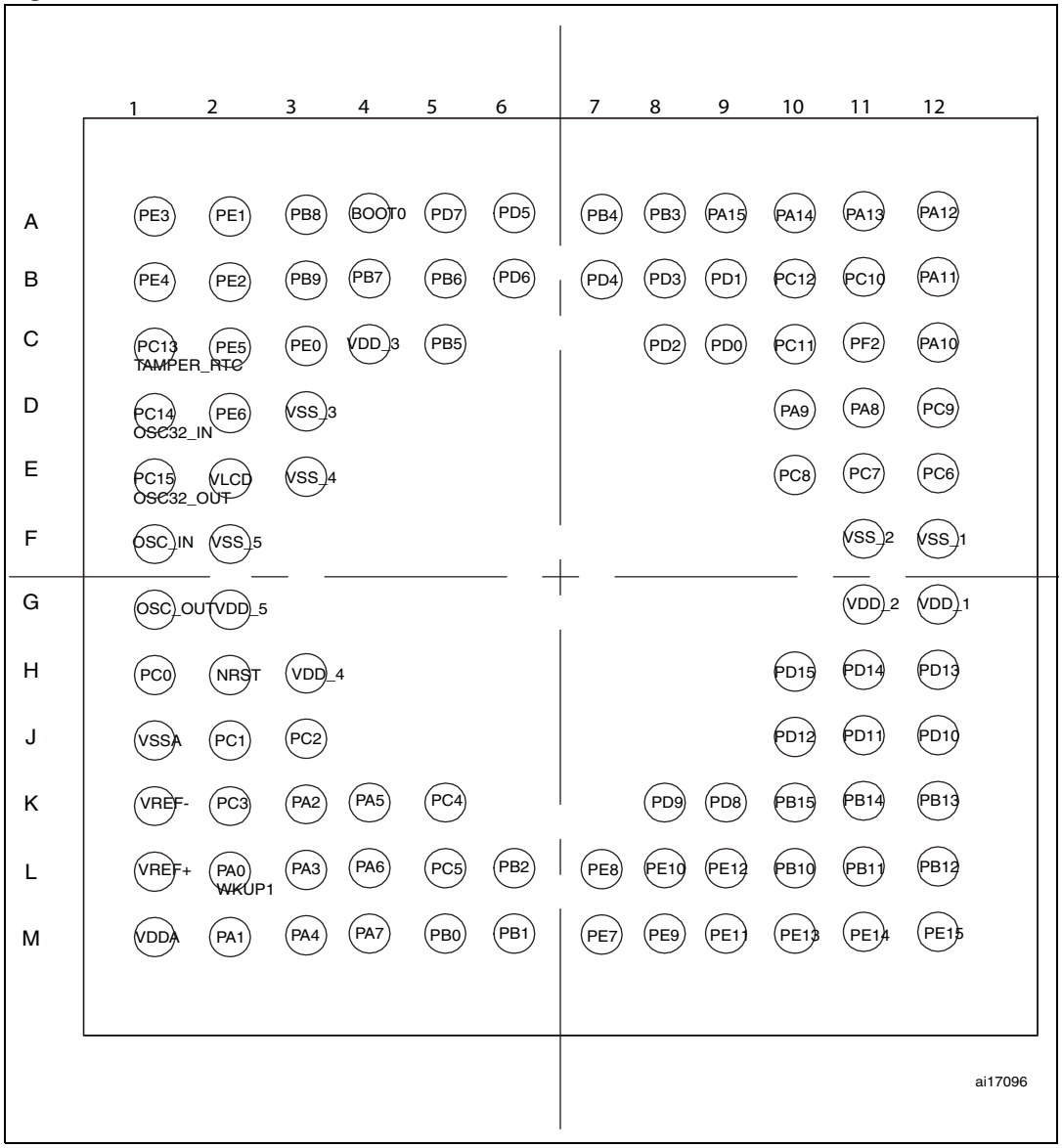


Figure 4. STM32L15xxx TFBGA64 ballout

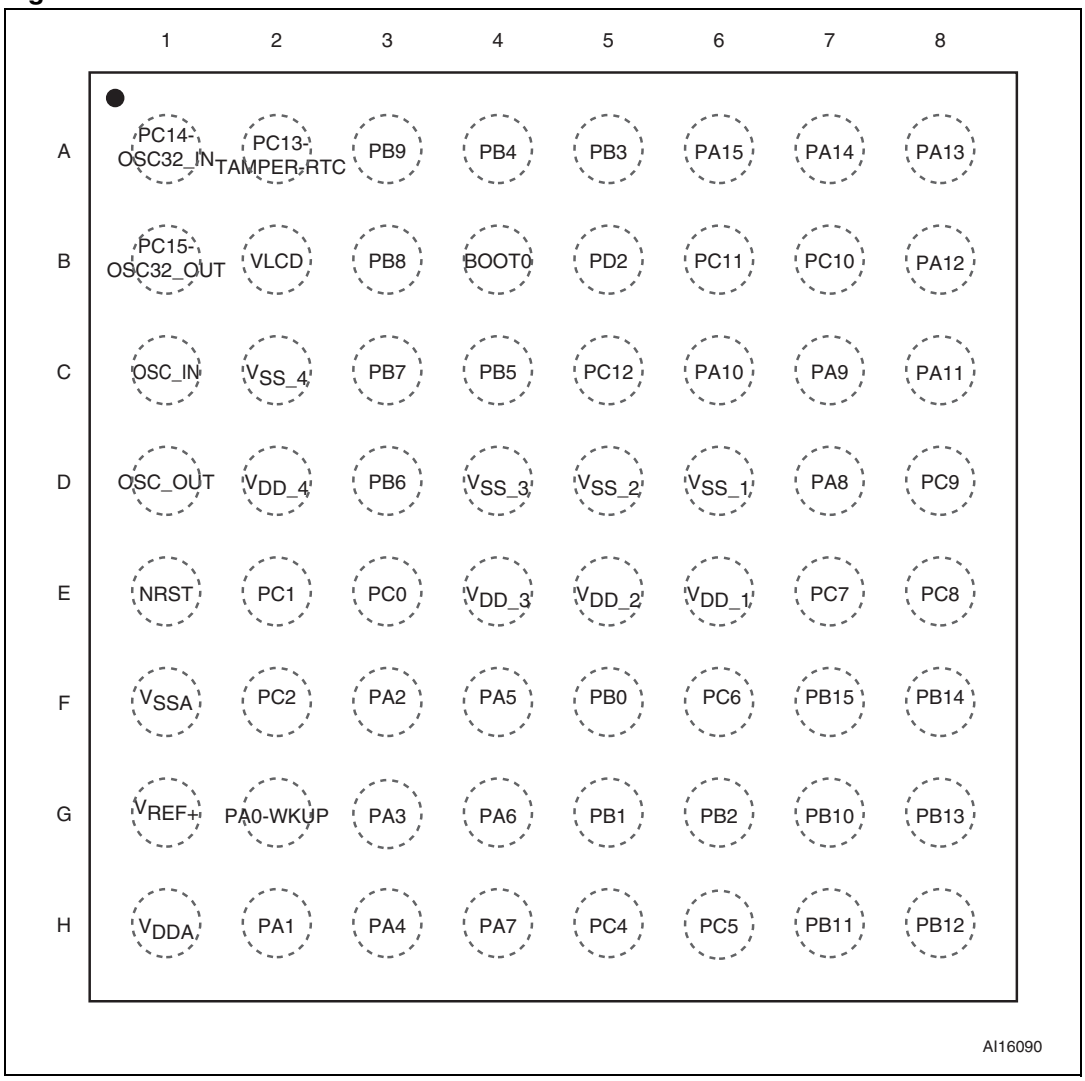


Figure 5. STM32L15xxx LQFP100 pinout

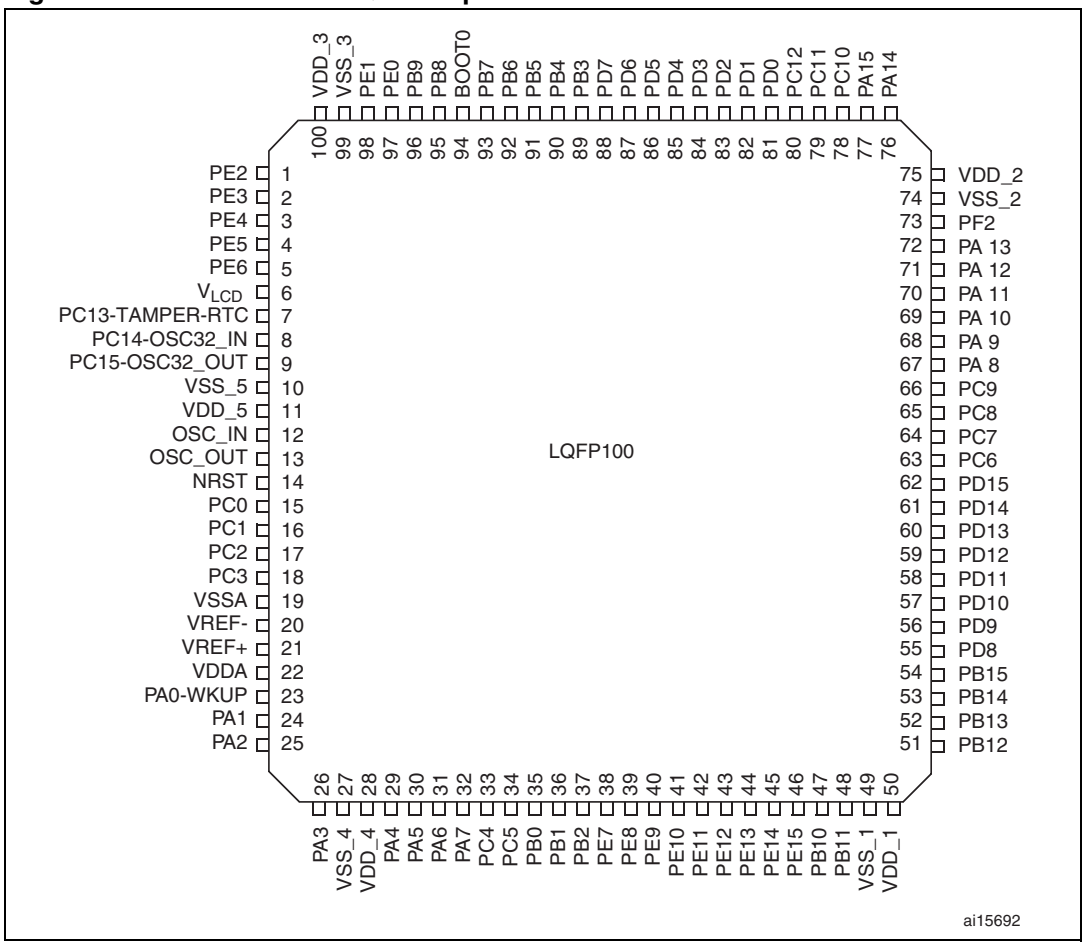


Figure 6. STM32L15xxx LQFP64 pinout

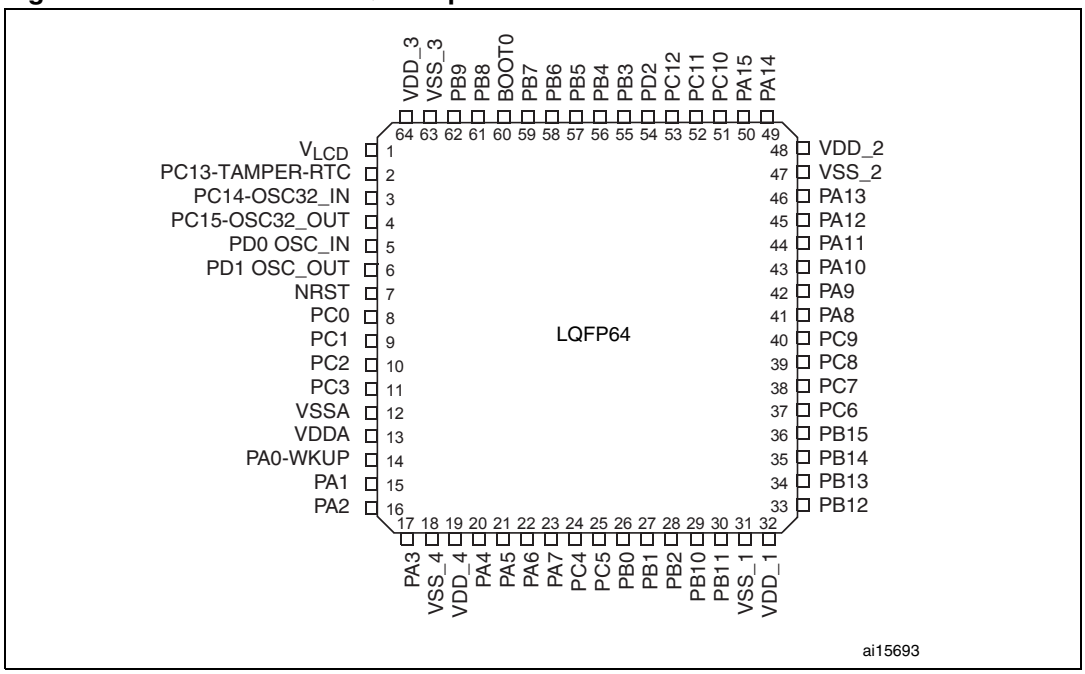


Figure 7. STM32L15xxx LQFP48 pinout

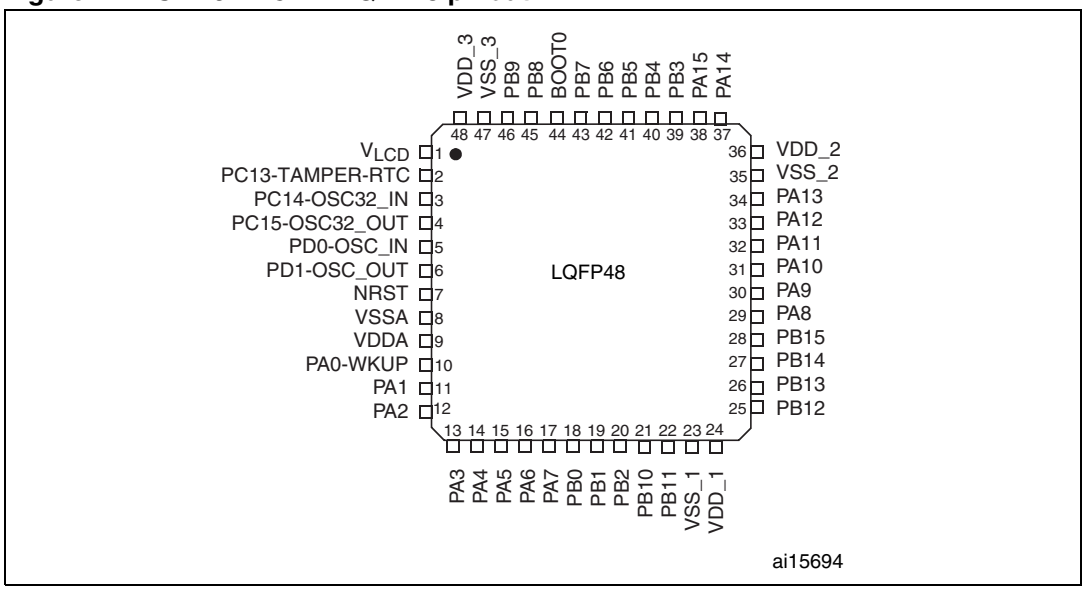


Figure 8. STM32L15xxx VFQFPN48 pinout

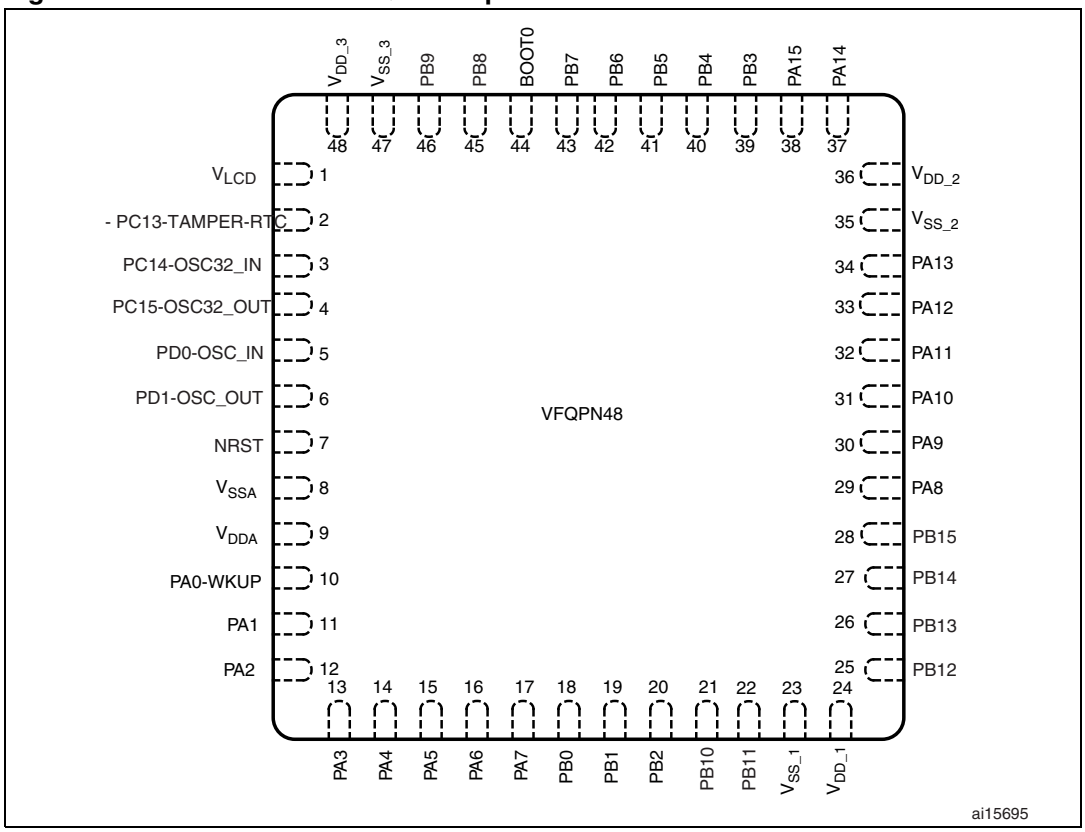


Table 4. STM32L15xxx pin definitions

Pins					Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48					
1	-		B2	-	PE2	I/O	FT	PE2	TRACECK/LCD_SEG38/TIM3_ETR
2	-		A1	-	PE3	I/O	FT	PE3	TRACED0/LCD_SEG39/TIM3_CH1
3	-		B1	-	PE4	I/O	FT	PE4	TRACED1/TIM3_CH2
4	-		C2	-	PE5	I/O	FT	PE5	TRACED2/TIM9_CH1
5	-		D2	-	PE6	I/O	FT	PE6	TRACED3/WKUP3/TIM9_CH2
6	1	B2	E2	1	V_{LCD}(4)	S		V_{LCD}	
7	2	A2	C1	2	PC13-TAMPER-RTC	I/O	FT	PC13	TAMPER/TIMESTAMP/WKUP2/ ALARM_OUT/RTC_512Hz
8	3	A1	D1	3	PC14-OSC32_IN	I/O		PC14	OSC32_IN
9	4	B1	E1	4	PC15-OSC32_OUT	I/O		PC15	OSC32_OUT
10	-	-	F2	-	V_{SS_5}	S		V_{SS_5}	
11	-	-	G2	-	V_{DD_5}	S		V_{DD_5}	
12	5	C1	F1	5	PF0-OSC_IN(5)	I		OSC_IN	PF0
13	6	D1	G1	6	PF1-OSC_OUT	O		OSC_OUT	PF1
14	7	E1	H2	7	NRST	I/O		NRST	
15	8	E3	H1	-	PC0	I/O	FT	PC0	ADC_IN10/LCD_SEG18/ COMP1_INP
16	9	E2	J2	-	PC1	I/O	FT	PC1	ADC_IN11/LCD_SEG19/ COMP1_INP
17	10	F2	J3	-	PC2	I/O	FT	PC2	ADC_IN12/LCD_SEG20/ COMP1_INP
18	11	-(6)	K2	-	PC3	I/O	FT	PC3	ADC_IN13/LCD_SEG21/ COMP1_INP
19	12	F1	J1	8	V_{SSA}	S		V_{SSA}	
20	-	-	K1	-	V_{REF-}	S		V_{REF-}	
21	-	G1 (6)	L1	-	V_{REF+}	S		V_{REF+}	
22	13	H1	M1	9	V_{DDA}	S		V_{DDA}	
23	14	G2	L2	10	PA0-WKUP1	I/O	FT	PA0	WKUP1/USART2_CTS/ADC_IN0/TIM2_CH1_ETR/ COMP1_INP
24	15	H2	M2	11	PA1	I/O	FT	PA1	USART2_RTS/ADC_IN1/ TIM2_CH2/LCD_SEG0/ COMP1_INP
25	16	F3	K3	12	PA2	I/O	FT	PA2	USART2_TX/ADC_IN2/ TIM2_CH3/TIM9_CH1/ LCD_SEG1/COMP1_INP

Table 4. STM32L15xxx pin definitions (continued)

Pins					Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48					
26	17	G3	L3	13	PA3	I/O	FT	PA3	USART2_RX/ADC_IN3/TIM2_CH4/TIM9_CH2/ LCD_SEG2/COMP1_INP
27	18	C2	E3	-	V_{SS_4}	S		V_{SS_4}	
28	19	D2	H3	-	V_{DD_4}	S		V_{DD_4}	
29	20	H3	M3	14	PA4	I/O		PA4	SPI1_NSS/ USART2_CK/ ADC_IN4/DAC_OUT1/COMP1_INP
30	21	F4	K4	15	PA5	I/O		PA5	SPI1_SCK/ADC_IN5/ DAC_OUT2/TIM2_CH1_ETR/COMP1_INP
31	22	G4	L4	16	PA6	I/O	FT	PA6	SPI1_MISO/ADC_IN6/TIM3_CH1/TIM1_BKIN/ LCD_SEG3/TIM10_CH1/ COMP1_INP
32	23	H4	M4	17	PA7	I/O	FT	PA7	SPI1_MOSI/ADC_IN7/TIM3_CH2/TIM1_CH1N/ LCD_SEG4/TIM11_CH1/COMP1_INP
33	24	H5	K5	-	PC4	I/O	FT	PC4	ADC_IN14/LCD_SEG22/COMP1_INP
34	25	H6	L5	-	PC5	I/O	FT	PC5	ADC_IN15/LCD_SEG23/COMP1_INP
35	26	F5	M5	18	PB0	I/O	FT	PB0	ADC_IN8/TIM3_CH3TIM1_CH2N/LCD_SEG5/ COMP1_INP/VREF_OUT
36	27	G5	M6	19	PB1	I/O	FT	PB1	ADC_IN9/TIM3_CH4/TIM1_CH3N/LCD_SEG6/ COMP1_INP/VREF_OUT
37	28	G6	L6	20	PB2	I/O	FT	PB2/BOOT1	
38	-	-	M7	-	PE7	I/O		PE7	ADC_IN22/COMP1_INP
39	-	-	L7	-	PE8	I/O		PE8	ADC_IN23/COMP1_INP
40	-	-	M8	-	PE9	I/O		PE9	ADC_IN24/TIM2_CH1_ETR/COMP1_INP
41	-	-	L8	-	PE10	I/O		PE10	ADC_IN25/TIM2_CH2/COMP1_INP
42	-	-	M9	-	PE11	I/O	FT	PE11	TIM2_CH3
43	-	-	L9	-	PE12	I/O	FT	PE12	TIM2_CH4/SPI1_NSS
44	-	-	M10	-	PE13	I/O	FT	PE13	SPI1_SCK
45	-	-	M11	-	PE14	I/O	FT	PE14	SPI1_MISO
46	-	-	M12	-	PE15	I/O	FT	PE15	SPI1_MOSI
47	29	G7	L10	21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX/TIM2_CH3/LCD_SEG10
48	30	H7	L11	22	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX/TIM2_CH4/LCD_SEG11
49	31	D6	F12	23	V_{SS_1}	S		V_{SS_1}	
50	32	E6	G12	24	V_{DD_1}	S		V_{DD_1}	
51	33	H8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/USART3_CK/LCD_SEG12/ ADC_IN18/COMP1_INP/TIM10_CH1

Table 4. STM32L15xxx pin definitions (continued)

Pins					Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48					
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/LCD_SEG13/ADC_IN19/ COMP1_INP/TIM9_CH1
53	35	F8	K11	27	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS/LCD_SEG14/ADC_IN20/ COMP1_INP/TIM9_CH2
54	36	F7	K10	28	PB15	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N/LCD_SEG15/ADC_IN21/ COMP1_INP/TIM11_CH1/RTC_50_60Hz
55	-	-	K9	-	PD8	I/O	FT	PD8	USART3_TX/LCD_SEG28
56	-	-	K8	-	PD9	I/O	FT	PD9	USART3_RX/LCD_SEG29
57	-	-	J12	-	PD10	I/O	FT	PD10	USART3_CK/LCD_SEG30
58	-	-	J11	-	PD11	I/O	FT	PD11	USART3_CTS/LCD_SEG31
59	-	-	J10	-	PD12	I/O	FT	PD12	TIM4_CH1 / USART3_RTS/ LCD_SEG32
60	-	-	H12	-	PD13	I/O	FT	PD13	TIM4_CH2/LCD_SEG33
61	-	-	H11	-	PD14	I/O	FT	PD14	TIM4_CH3/LCD_SEG34
62	-	-	H10	-	PD15	I/O	FT	PD15	TIM4_CH4/LCD_SEG35
63	37	F6	E12	-	PC6	I/O	FT	PC6	TIM3_CH1/LCD_SEG24
64	38	E7	E11		PC7	I/O	FT	PC7	TIM3_CH2/LCD_SEG25
65	39	E8	E10		PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26
66	40	D8	D12	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27
67	41	D7	D11	29	PA8	I/O	FT	PA8	USART1_CK/MCO/LCD_COM0
68	42	C7	D10	30	PA9	I/O	FT	PA9	USART1_TX / LCD_COM1
69	43	C6	C12	31	PA10	I/O	FT	PA10	USART1_RX / LCD_COM2
70	44	C8	B12	32	PA11	I/O	FT	PA11	USART1_CTS/ USBDM/SPI1_MISO
71	45	B8	A12	33	PA12	I/O	FT	PA12	USART1_RTS/USBDP/SPI1_MOSI
72	46	A8	A11	34	PA13	I/O	FT	JTMS/SWDIO	PA13
73	-	-	C11	-	PF2	I/O	FT	PF2	I2C2_SMBA
74	47	D5	F11	35	V_{SS_2}	S		V_{SS_2}	
75	48	E5	G11	36	V_{DD_2}	S		V_{DD_2}	
76	49	A7	A10	37	PA14	I/O	FT	JTCK/SWCLK	PA14
77	50	A6	A9	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/ PA15/SPI1_NSS/LCD_SEG17
78	51	B7	B11	-	PC10	I/O	FT	PC10	USART3_TX/LCD_SEG28/LCD_SEG40/ LCD_COM4
79	52	B6	C10	-	PC11	I/O	FT	PC11	USART3_RX/LCD_SEG29/LCD_SEG41/LCD_COM5
80	53	C5	B10	-	PC12	I/O	FT	PC12	USART3_CK/LCD_SEG30/LCD_SEG42/LCD_COM6

Table 4. STM32L15xxx pin definitions (continued)

Pins					Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48					
81	5	C1	C9	5	PD0	I/O	FT	OSC_IN	SPI2_NSS/TIM9_CH1
82	6	D1	B9	6	PD1	I/O	FT	OSC_OUT	SPI2_SCK
83	54	B5	C8		PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31/LCD_SEG43/LCD_COM7
84	-	-	B8	-	PD3	I/O	FT	PD3	USART2_CTS/SPI2_MISO
85	-	-	B7	-	PD4	I/O	FT	PD4	USART2_RTS/SPI2_MOSI
86	-	-	A6	-	PD5	I/O	FT	PD5	USART2_TX
87	-	-	B6	-	PD6	I/O	FT	PD6	USART2_RX
88	-	-	A5	-	PD7	I/O	FT	PD7	USART2_CK/TIM9_CH2
89	55	A5	A8	39	PB3	I/O	FT	JTDO	TIM2_CH2 / PB3/TRACESWO SPI1_SCK/COMP2_INM/LCD_SEG7
90	56	A4	A7	40	PB4	I/O	FT	JNTRST	TIM3_CH1/ PB4/ SPI1_MISO/COMP2_INP/LCD_SEG8
91	57	C4	C5	41	PB5	I/O	FT	PB5	I2C1_SMBAI/TIM3_CH2 /SPI1_MOSI/COMP2_INP/LCD_SEG9
92	58	D3	B5	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX/LCD_SEG8
93	59	C3	B4	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/ USART1_RX/PVD_IN
94	60	B4	A4	44	BOOT0	I		BOOT0	
95	61	B3	A3	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL / LCD_SEG16/TIM10_CH1
96	62	A3	B3	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/LCD_COM3 / TIM11_CH1
97	-	-	C3	-	PE0	I/O	FT	PE0	TIM4_ETR/LCD_SEG36 /TIM10_CH1
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/TIM11_CH1
99	63	D4	D3	47	V_{SS_3}	S		V_{SS_3}	
100	64	E4	C4	48	V_{DD_3}	S		V_{DD_3}	

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 7*.
4. Applicable to STM32L152xx devices only. In STM32L151xx devices, this pin should be connected to V_{DD}.
5. The pins number 5 and 6 in the LQFP48 and LQFP64 packages, and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PF0 and PF1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Table 5. Alternate function input/output

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	SCI1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
BOOT0	BOOT0															
NRST	NRST															
PA0-WKUP	WKUP1	TIM2_CH1_ETR						SCI2_CTS							TIMx_IC1	EVENTOUT
PA1		TIM2_CH2						SCI2_RTS				[SEG0]			TIMx_IC2	EVENTOUT
PA2		TIM2_CH3		TIM9_CH1				SCI2_TX				[SEG1]			TIMx_IC3	EVENTOUT
PA3		TIM2_CH4		TIM9_CH2				SCI2_RX				[SEG2]			TIMx_IC4	EVENTOUT
PA4						SPI1_NSS		SCI2_CK							TIMx_IC1	EVENTOUT
PA5		TIM2_CH1_ETR				SPI1_SCK									TIMx_IC2	EVENTOUT
PA6			TIM3_CH1	TIM10_CH1		SPI1_MISO						[SEG3]			TIMx_IC3	EVENTOUT
PA7			TIM3_CH2	TIM11_CH1		SPI1_MOSI						[SEG4]			TIMx_IC4	EVENTOUT
PA8	MCO							SCI1_CK				[COM0]			TIMx_IC1	EVENTOUT
PA9								SCI1_TX				[COM1]			TIMx_IC2	EVENTOUT
PA10								SCI1_RX				[COM2]			TIMx_IC3	EVENTOUT
PA11						SPI1_MISO		SCI1_CTS			DM				TIMx_IC4	EVENTOUT
PA12						SPI1_MOSI		SCI1_RTS			DP				TIMx_IC1	EVENTOUT
PA13	JTMS-SWDAT														TIMx_IC2	EVENTOUT
PA14	JTCK-SWCLK														TIMx_IC3	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR				SPI1_NSS						SEG17			TIMx_IC4	EVENTOUT
PB0			TIM3_CH3									[SEG5]				EVENTOUT
PB1			TIM3_CH4									[SEG6]				EVENTOUT
PB2	BOOT1															EVENTOUT
PB3	JTDO	TIM2_CH2				SPI1_SCK						[SEG7]				EVENTOUT

Table 5. Alternate function input/output *(continued)*

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	SCI1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
PB4	JTRST		TIM3_CH1			SPI1_MISO						[SEG8]				EVENTOUT
PB5			TIM3_CH2		I2C1_SMBAI	SPI1_MOSI						[SEG9]				EVENTOUT
PB6			TIM4_CH1		I2C1_SCL			SCI1_TX								EVENTOUT
PB7			TIM4_CH2		I2C1_SDA			SCI1_RX								EVENTOUT
PB8			TIM4_CH3	TIM10_CH1*	I2C1_SCL							SEG16				EVENTOUT
PB9			TIM4_CH4	TIM11_CH1*	I2C1_SDA							[COM3]				EVENTOUT
PB10		TIM2_CH3			I2C2_SCL			SCI3_TX				SEG10				EVENTOUT
PB11		TIM2_CH4			I2C2_SDA			SCI3_RX				SEG11				EVENTOUT
PB12				TIM10_CH1	I2C2_SMBAI	SPI2_NSS		SCI3_CK				SEG12				EVENTOUT
PB13				TIM9_CH1		SPI2_SCK		SCI3_CTS				SEG13				EVENTOUT
PB14				TIM9_CH2		SPI2_MISO		SCI3_RTS				SEG14				EVENTOUT
PB15	RTC 50/60 Hz			TIM11_CH1		SPI2_MOSI						SEG15				EVENTOUT
PC0												SEG18			TIMx_IC1	EVENTOUT
PC1												SEG19			TIMx_IC2	EVENTOUT
PC2												SEG20			TIMx_IC3	EVENTOUT
PC3												SEG21			TIMx_IC4	EVENTOUT
PC4												SEG22			TIMx_IC1	EVENTOUT
PC5												SEG23			TIMx_IC2	EVENTOUT
PC6			TIM3_CH1									SEG24			TIMx_IC3	EVENTOUT
PC7			TIM3_CH2									SEG25			TIMx_IC4	EVENTOUT
PC8			TIM3_CH3									SEG26			TIMx_IC1	EVENTOUT
PC9			TIM3_CH4									SEG27			TIMx_IC2	EVENTOUT

Table 5. Alternate function input/output *(continued)*

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	SCI1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
PC10								SCI3_TX				COM4 / SEG28 / SEG40			TIMx_IC3	EVENTOUT
PC11								SCI3_RX				COM5 / SEG29 / SEG41			TIMx_IC4	EVENTOUT
PC12								SCI3_CK				COM6 / SEG30 / SEG42			TIMx_IC1	EVENTOUT
PC13-TAMPER-RTC	TAMPER / TIMESTAMP / WKUP2 / ALARM_OUT / 512Hz														TIMx_IC2	EVENTOUT
PC14-OSC32_IN	OSC32_IN														TIMx_IC3	EVENTOUT
PC15-OSC32_OUT	OSC32_OUT														TIMx_IC4	EVENTOUT
PD0				TIM9_CH1		SPI2_NSS									TIMx_IC1	EVENTOUT
PD1						SPI2_SCK									TIMx_IC2	EVENTOUT
PD2			TIM3_ETR									COM7 / SEG31 / SEG43			TIMx_IC3	EVENTOUT
PD3						SPI2_MISO		SCI2_CTS							TIMx_IC4	EVENTOUT
PD4						SPI2_MOSI		SCI2_RTS							TIMx_IC1	EVENTOUT
PD5								SCI2_TX							TIMx_IC2	EVENTOUT
PD6								SCI2_RX							TIMx_IC3	EVENTOUT
PD7				TIM9_CH2				SCI2_CK							TIMx_IC4	EVENTOUT
PD8								SCI3_TX				SEG28			TIMx_IC1	EVENTOUT
PD9								SCI3_RX				SEG29			TIMx_IC2	EVENTOUT
PD10								SCI3_CK				SEG30			TIMx_IC3	EVENTOUT

Table 5. Alternate function input/output *(continued)*

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	SCI1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
PD11								SCI3_CTS				SEG31			TIMx_IC4	EVENTOUT
PD12			TIM4_CH1					SCI3_RTS				SEG32			TIMx_IC1	EVENTOUT
PD13			TIM4_CH2									SEG33			TIMx_IC2	EVENTOUT
PD14			TIM4_CH3									SEG34			TIMx_IC3	EVENTOUT
PD15			TIM4_CH4									SEG35			TIMx_IC4	EVENTOUT
PE0			TIM4_ETR	TIM10_CH1								SEG36			TIMx_IC1	EVENTOUT
PE1				TIM11_CH1								SEG37			TIMx_IC2	EVENTOUT
PE2	TRACECK		TIM3_ETR									SEG 38			TIMx_IC3	EVENTOUT
PE3	TRACED0		TIM3_CH1									SEG 39			TIMx_IC4	EVENTOUT
PE4	TRACED1		TIM3_CH2												TIMx_IC1	EVENTOUT
PE5	TRACED2			TIM9_CH1*											TIMx_IC2	EVENTOUT
PE6	TRACED3 / WKUP3			TIM9_CH2*											TIMx_IC3	EVENTOUT
PE7															TIMx_IC4	EVENTOUT
PE8															TIMx_IC1	EVENTOUT
PE9		TIM2_CH1_ ETR													TIMx_IC2	EVENTOUT
PE10		TIM2_CH2													TIMx_IC3	EVENTOUT
PE11		TIM2_CH3													TIMx_IC4	EVENTOUT
PE12		TIM2_CH4				SPI1_NSS									TIMx_IC1	EVENTOUT
PE13						SPI1_SCK									TIMx_IC2	EVENTOUT
PE14						SPI1_MISO									TIMx_IC3	EVENTOUT
PE15						SPI1_MOSI									TIMx_IC4	EVENTOUT
PF0-OSC_IN	OSC_IN															

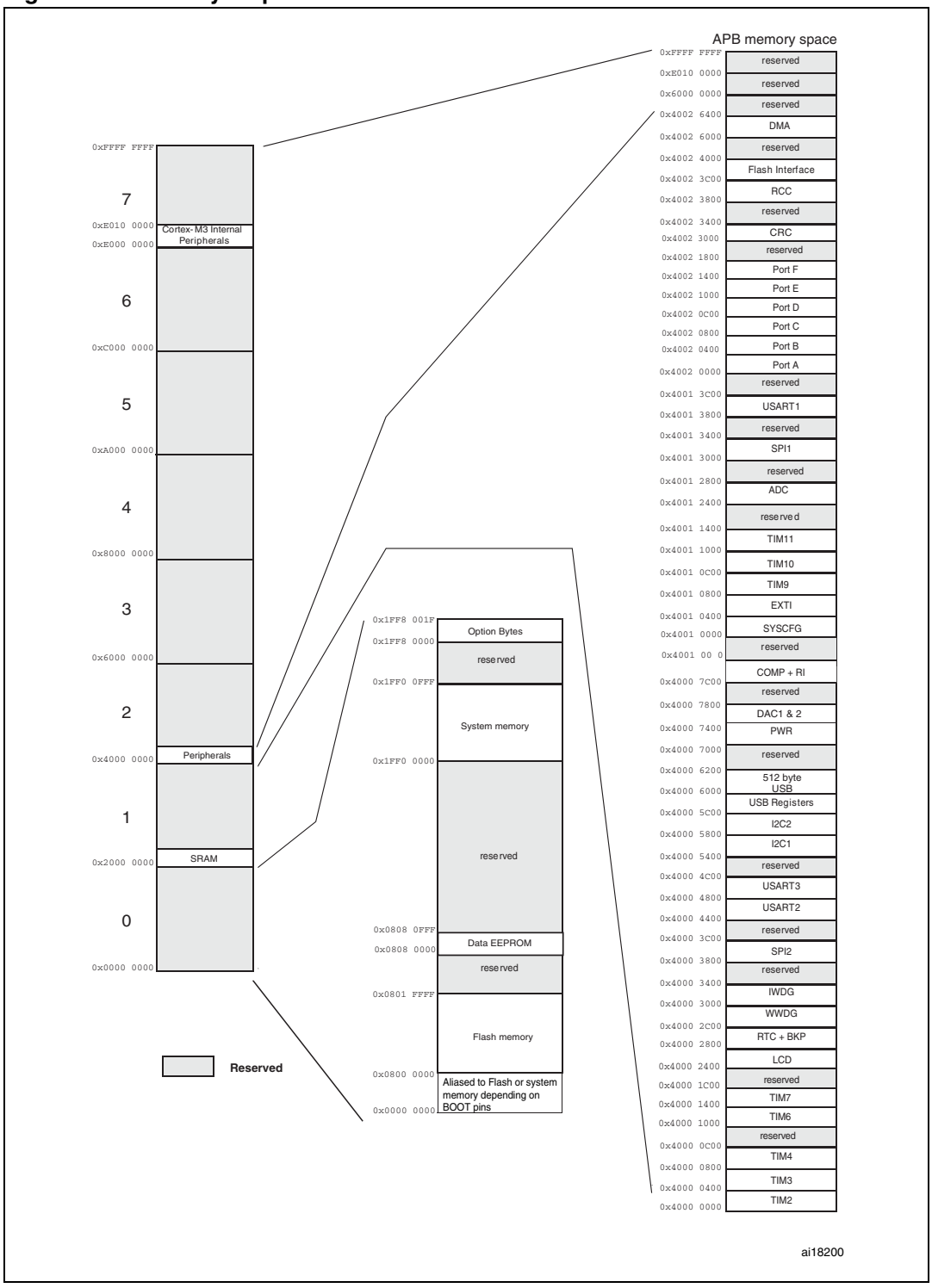
Table 5. Alternate function input/output *(continued)*

Port name	Digital alternate function number															
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO10	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function															
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	SCI1/2/3	N/A	N/A	USBFS	LCD	N/A	N/A	RI	SYSTEM
PF1-OSC_OUT	OSC_OUT															
PF2																EVENTOUT

5 Memory mapping

The memory map is shown in the following figure.

Figure 9. Memory map



6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 10. VFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline(1)

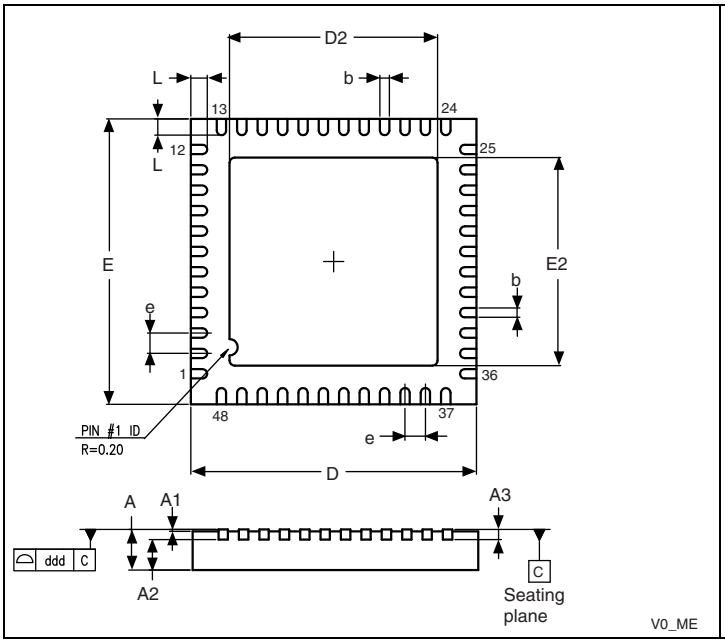
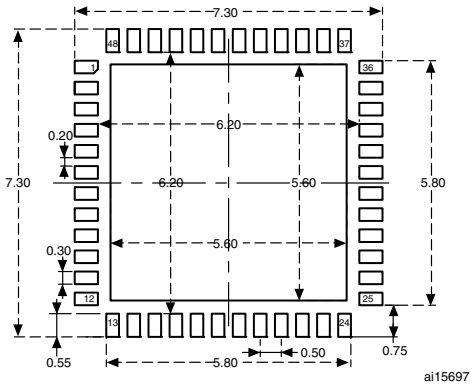


Figure 11. Recommended footprint (dimensions in mm)(1)



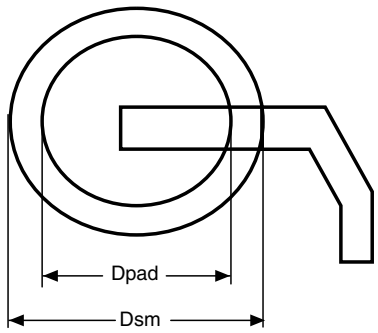
1. Drawing is not to scale.

Table 6. VFQFPN48 – very thin fine pitch quad flat pack nolead 7 × 7 mm, 0.5 mm pitch package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A	0.900	0.800	1.000	0.0354	0.0315	0.0394
A1	0.020		0.050	0.0008		0.0020
A2	0.650		1.000	0.0256		0.0394
A3	0.250			0.0098		
b	0.230	0.180	0.300	0.0091	0.0071	0.0118
D	7.000	6.850	7.150	0.2756	0.2697	0.2815
D2	4.700	2.250	5.250	0.1850	0.0886	0.2067
E	7.000	6.850	7.150	0.2756	0.2697	0.2815
E2	4.700	2.250	5.250	0.1850	0.0886	0.2067
e	0.500	0.450	0.550	0.0197	0.0177	0.0217
L	0.400	0.300	0.500	0.0157	0.0118	0.0197
ddd	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 12. Recommended PCB design rules for pads (0.5 mm pitch BGA)

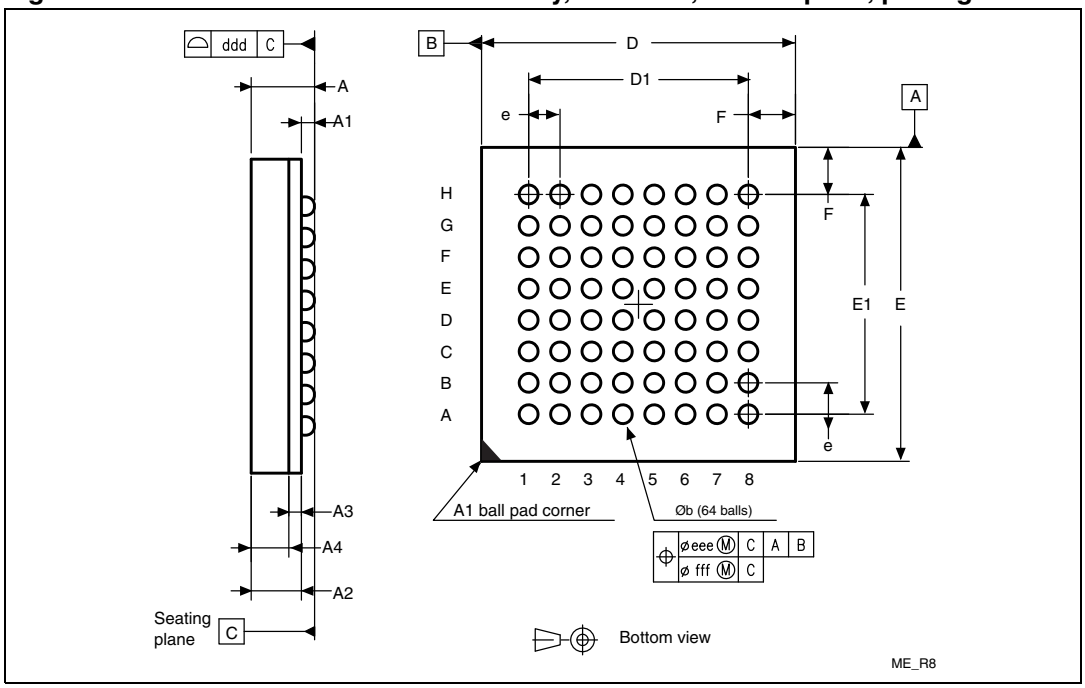


Pitch	0.5 mm
D pad	0.27 mm
Dsm	0.35 mm typ (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter

ai15495

1. Non solder mask defined (NSMD) pads are recommended
2. 4 to 6 mils solder paste screen printing process

Figure 13. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package outline



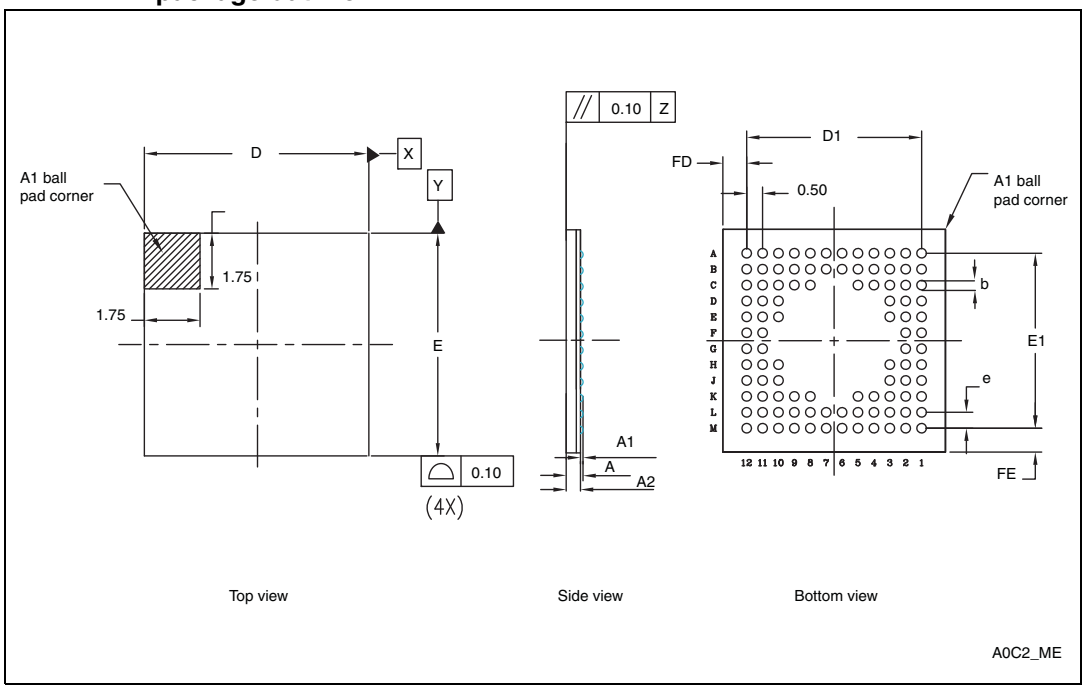
1. Drawing is not to scale.

Table 7. TFBGA64 - 8 x 8 active ball array, 5 x 5 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.200			0.0472
A1	0.150			0.0059		
A2		0.785			0.0309	
A3		0.200			0.0079	
A4			0.600			0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1		3.500			0.1378	
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1		3.500			0.1378	
e		0.500			0.0197	
F		0.750			0.0295	
ddd		0.080			0.0031	
eee		0.150			0.0059	
fff		0.050			0.0020	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 14. UFBGA100 - ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package outline



1. Drawing is not to scale.

Table 8. UFBGA100 - ultra fine pitch ball grid array, 7 x 7 mm, 0.50 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.46	0.53	0.6	0.0181	0.0209	0.0236
A1	0.06	0.08	0.1	0.0024	0.0031	0.0039
A2	0.4	0.45	0.5	0.0157	0.0177	0.0197
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D		7			0.2756	
D1		5.5			0.2165	
E		7			0.2756	
E1		5.5			0.2165	
e		0.5			0.0197	
FD		0.75			0.0295	
FE		0.75			0.0295	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 15. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline(1)

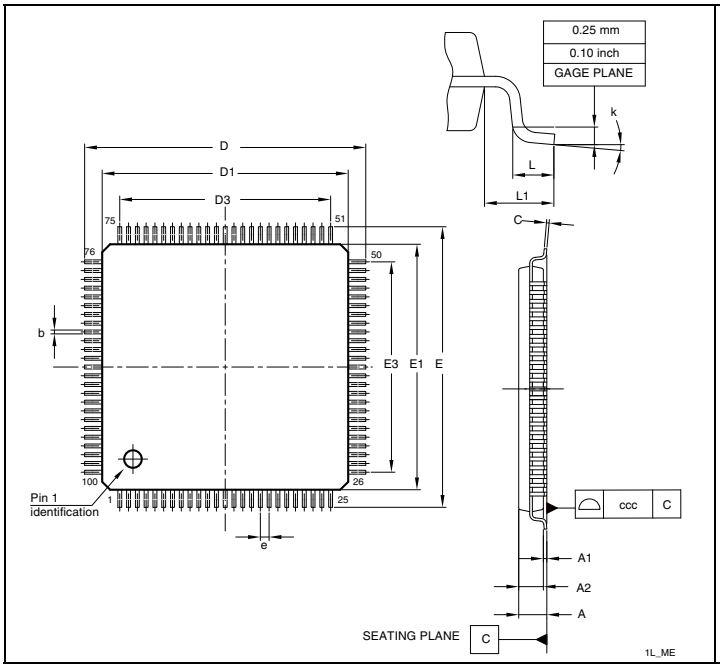
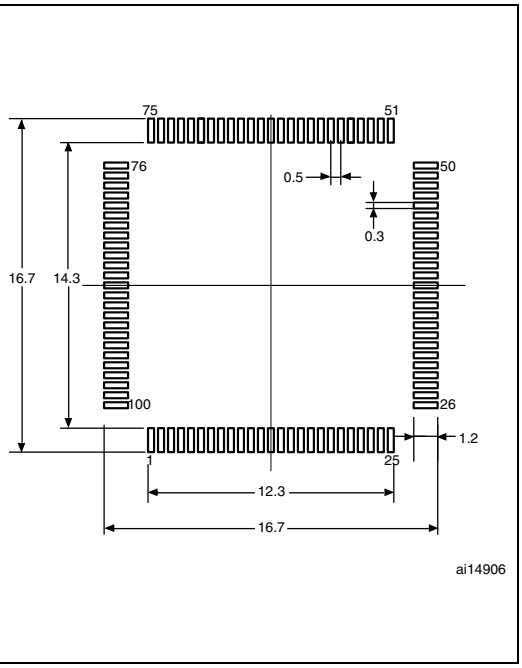


Figure 16. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 9. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.6			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.2	0.0035		0.0079
D	15.8	16	16.2	0.622	0.6299	0.6378
D1	13.8	14	14.2	0.5433	0.5512	0.5591
D3		12			0.4724	
E	15.8	16	16.2	0.622	0.6299	0.6378
E1	13.8	14	14.2	0.5433	0.5512	0.5591
E3		12			0.4724	
e		0.5			0.0197	
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 17. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline(1)

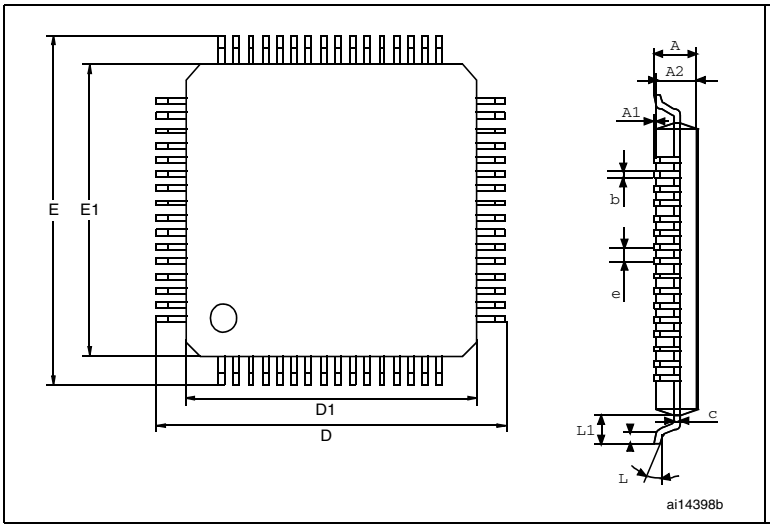
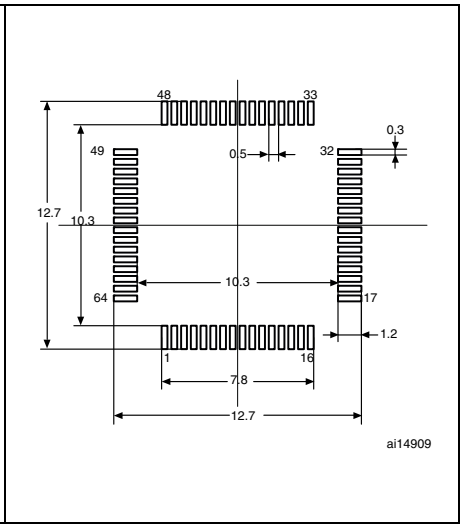


Figure 18. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 10. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 19. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package outline(1)

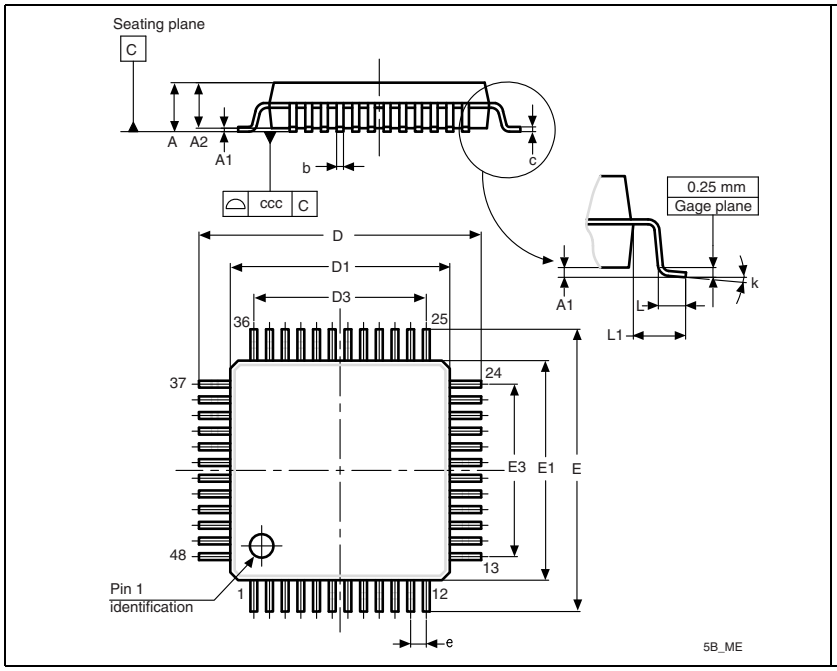
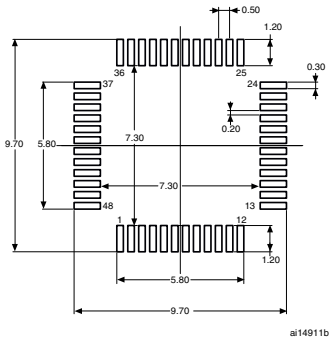


Figure 20. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 11. LQFP48, 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.600			0.0630
A1		0.050	0.150		0.0020	0.0059
A2	1.400	1.350	1.450	0.0551	0.0531	0.0571
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
c		0.090	0.200		0.0035	0.0079
D	9.000	8.800	9.200	0.3543	0.3465	0.3622
D1	7.000	6.800	7.200	0.2756	0.2677	0.2835
D3	5.500			0.2165		
E	9.000	8.800	9.200	0.3543	0.3465	0.3622
E1	7.000	6.800	7.200	0.2756	0.2677	0.2835
E3	5.500			0.2165		
e	0.500			0.0197		
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
k	3.5°	0°	7°	3.5°	0°	7°
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 12. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** BGA100 - 7 x 7 mm	TBD	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient VFQFPN48 - 7 x 7 mm / 0.5 mm pitch	16	

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 13: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L15xxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 12* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 13: Ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 12* T_{Jmax} is calculated as follows:

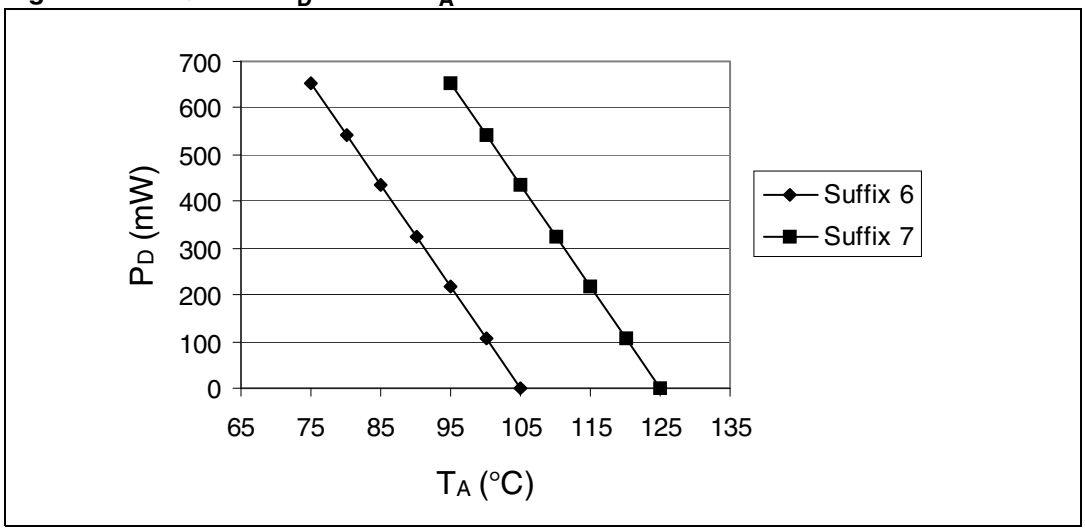
– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 13: Ordering information scheme*).

Figure 21. LQFP100 P_D max vs. T_A



7 Ordering information scheme

Table 13. Ordering information scheme

Example: STM32 L 151 C 8 T 6 D xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

151: Devices without LCD

152: Devices with LCD

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

H = BGA

T = LQFP

U = VFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 14. Document revision history

Date	Revision	Changes
02-Apr-2010	1	Initial release.