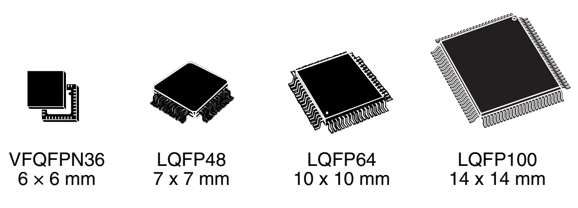
STM32F101x6
STM32F101x8 STM32F101xB

Access line, advanced ARM-based 32-bit MCU with Flash memory, six 16-bit timers, ADC and seven communication interfaces

Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 36 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 32 to 128 Kbytes of Flash memory
  - 6 to 16 Kbytes of SRAM
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC
  - PLL for CPU clock
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC and backup registers
- Debug mode
  - Serial wire debug (SWD) and JTAG interfaces
- DMA
  - 7-channel DMA controller
  - Peripherals supported: timers, ADC, SPIs, I^2Cs and USARTs
- 1 × 12-bit, 1 µs A/D converter (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Temperature sensor
- Up to 80 fast I/O ports
  - 26/37/51/80 I/Os, all mappable on 16 external interrupt vectors, all 5 V-tolerant except for analog inputs



- Up to 6 timers
  - Up to three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - 2 watchdog timers (Independent and Window)
  - SysTick timer: 24-bit downcounter
- Up to 7 communication interfaces
  - Up to 2 x I^2C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 2 SPIs (18 Mbit/s)
- CRC calculation unit, 96-bit unique ID
- ECOPACK® packages

Table 1. Device summary

Reference	Root part number
STM32F101x6	STM32F101C6, STM32F101R6, STM32F101T6
STM32F101x8	STM32F101C8, STM32F101R8 STM32F101V8, STM32F101T8
STM32F101xB	STM32F101RB, STM32F101VB, STM32F101CB

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101x6, STM32F101xB and STM32F101x8 Medium-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The Medium-density STM32F101xx datasheet should be read in conjunction with the Medium- and High-density STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2 Description

The STM32F101x6, STM32F101xB and STM32F101x8 Medium-density access line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 16 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (two I^2Cs, two SPIs, and up to three USARTs), one 12-bit ADC and three general purpose 16-bit timers.

The STM32F101xx Medium-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F101xx Medium-density access line family includes devices in four different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F101xx High-density access line microcontroller family suitable for a wide range of applications:

- Application control and user interface
- Medical and handheld equipment
- PC peripherals, gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

Figure 1 shows the general block diagram of the device family.

2.1 Device overview

Table 2. Device features and peripheral counts (STM32F101xx High-density access line)

Peripheral		STM32F101Tx		STM32F101Cx			STM32F101Rx			STM32F101Vx	
Flash - Kbytes		32	64	32	64	128	32	64	128	64	128
SRAM - Kbytes		6	10	6	10	16	6	10	16	10	16
Timers	**General purpose**	2	3	2	3	3	2	3		3	
Communication	**SPI**	1	1	1	2	2	1	2		2	
	I^{2}C	1	1	1	2	2	1	2		2	
	USART	2	2	2	3	3	2	3		3	
12-bit synchronized ADC number of channels		1 10 channels		1 10 channels			1 16 channels			1 16 channels	
GPIOs		26		37			51			80	
CPU frequency		36 MHz									
Operating voltage		2.0 to 3.6 V									
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 8*) Junction temperature: –40 to +105 °C (see *Table 8*)									
Packages		VFQFPN36		LQFP48			LQFP64			LQFP100	

2.2 Full compatibility throughout the family

The STM32F101xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F101x6, STM32F101x8 and STM32F101xB are referred to as Medium-density devices, while the STM32F101xC, STM32F101xD and STM32F101xE are referred to as High-density devices.

High-density devices are an extension of the STM32F101x6/8/B devices, they are specified in the STM32F101xC/D/E datasheet. They feature higher Flash memory and RAM densities, and additional peripherals like FSMC and DAC, while remaining fully compatible with the other members of the family.
The STM32F101xC, STM32F101xD and STM32F101xE are a drop-in replacement for the STM32F101x6/8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Table 3. STM32F101xx family

Pinout	Memory size					
	Medium-density STM32F101xx devices			High-density STM32F101xx devices		
	32 KB Flash	64 KB Flash	128 KB Flash	256 KB Flash	384 KB Flash	512 KB Flash
	6 KB RAM	10 KB RAM	16 KB RAM	32 KB RAM	48 KB RAM	48 KB RAM
144				5 × USARTs 4 × 16-bit timers, 2 × basic timers 3 × SPIs, 2 × I^2Cs, 1 × ADC, 1 × DAC FSMC (100 and 144 pins)		
100		3 × USARTs 3 × 16-bit timers 2 × SPIs, 2 × I2Cs, 1 × ADC				
64	2 × USARTs 2 × 16-bit timers 1 × SPI, 1 × I^2C 1 × ADC					
48						
36						

2.3 Overview

ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F101xx Medium-density access line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

Embedded Flash memory

Up to 128 Kbytes of embedded Flash is available for storing programs and data.

CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Embedded SRAM

Up to 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Nested vectored interrupt controller (NVIC)

The STM32F101xx Medium-density access line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the High Speed APB (APB2) and the low Speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 36 MHz. See *Figure 2* for details on the clock tree.

Boot modes

At startup, boot pins are used to select one of five boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

Power supply schemes

- V_{DD} = 2.0 to 3.6 V: External power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: External analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to *Table 10: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

Low-power modes

The STM32F101xx Medium-density access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.
- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^{2}C, USART, general purpose timers TIMx and ADC.

RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers (ten 16-bit registers) can be used to store data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

General-purpose timers (TIMx)

There are up to 3 synchronizable standard timers embedded in the STM32F101xx Medium-density access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one pulse mode output. This gives up to 12 input captures / output compares / PWMs on the largest packages. They can work together via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

I^{2}C bus

Up to two I²C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

ADC (analog to digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

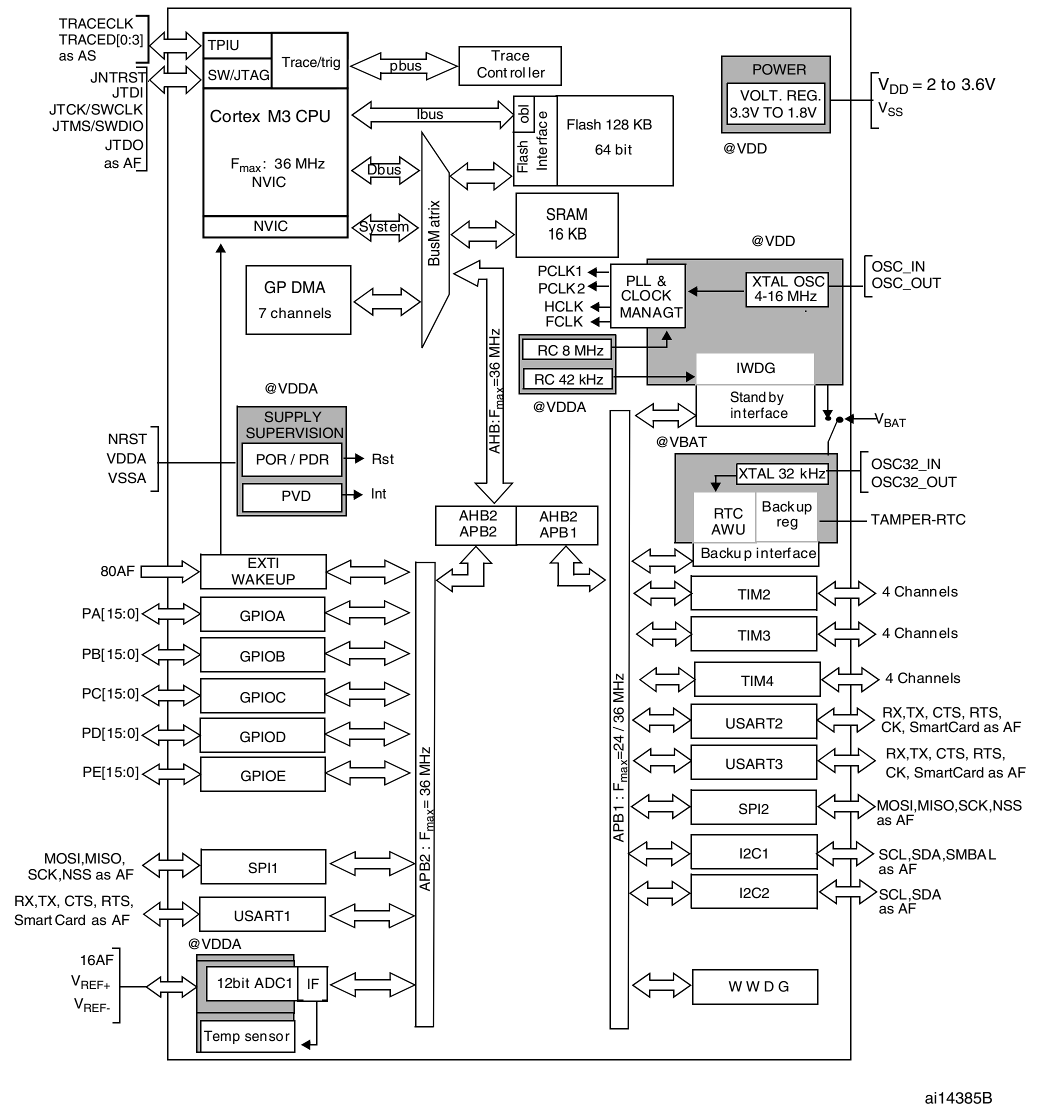
Temperature sensor

The temperature sensor has to generate a linear voltage with any variation in temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

Serial wire JTAG debug port (SWJ-DP)

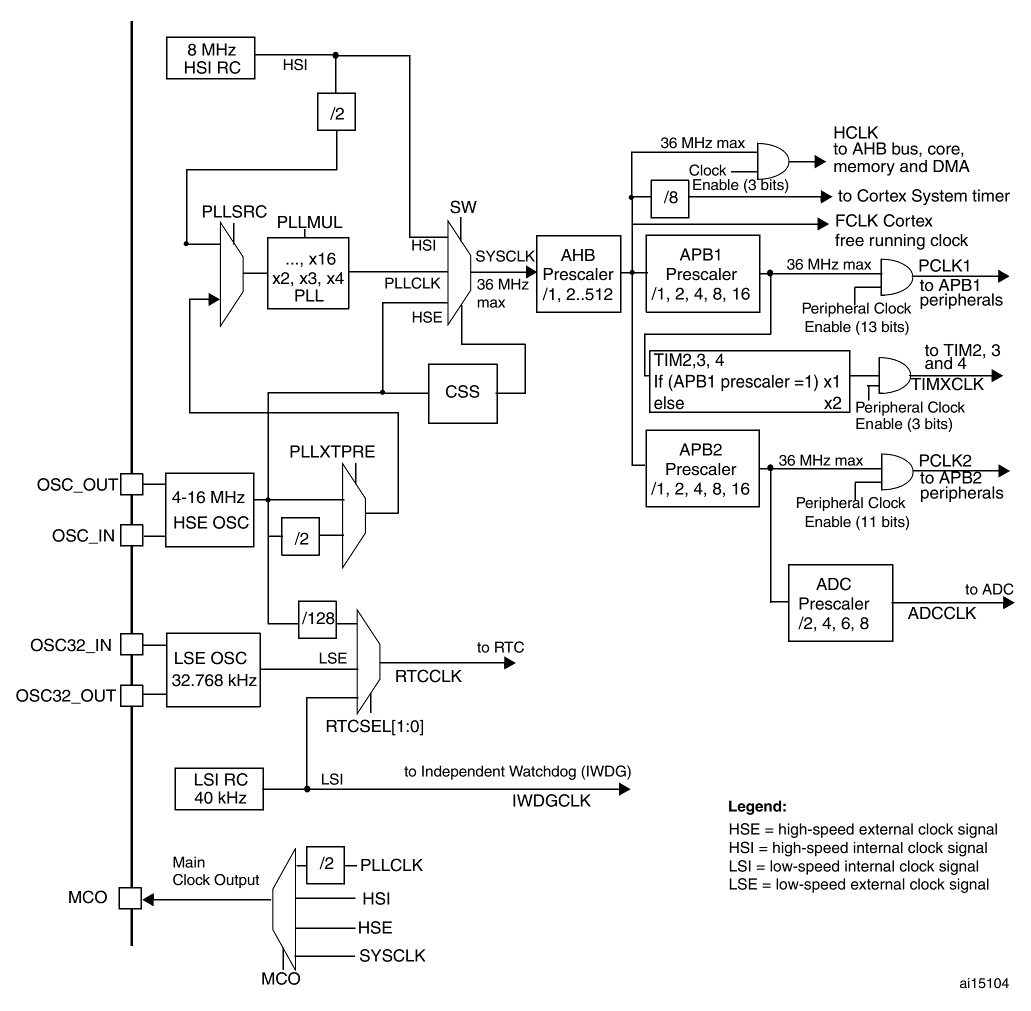
The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 1. STM32F101xx Medium-density access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 125 °C).

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 36 MHz.
2. To have an ADC conversion time of 1 μs, APB2 must be at 14 MHz or 28 MHz.

3 Pin descriptions

Figure 3. STM32F101xx Medium-density access line LQFP100 pinout

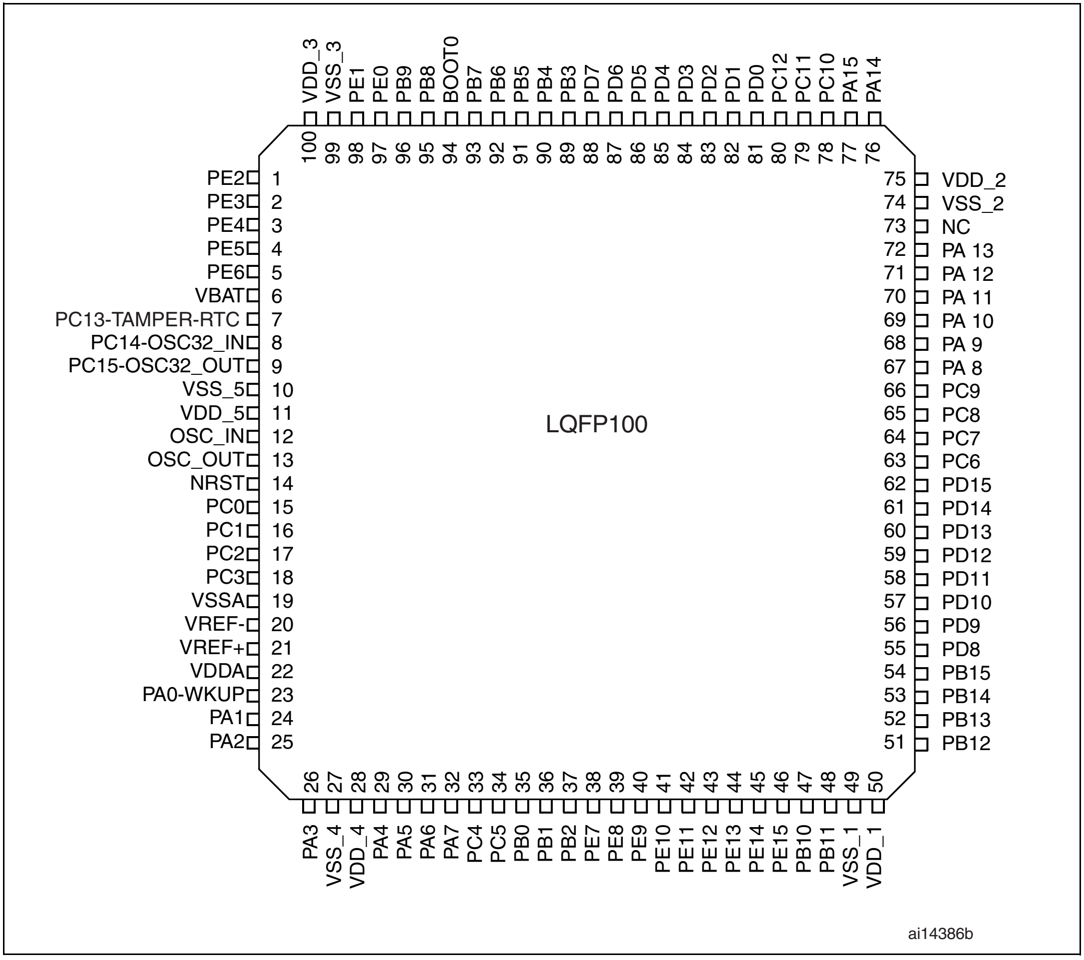


Figure 4. STM32F101xx Medium-density access line LQFP64 pinout

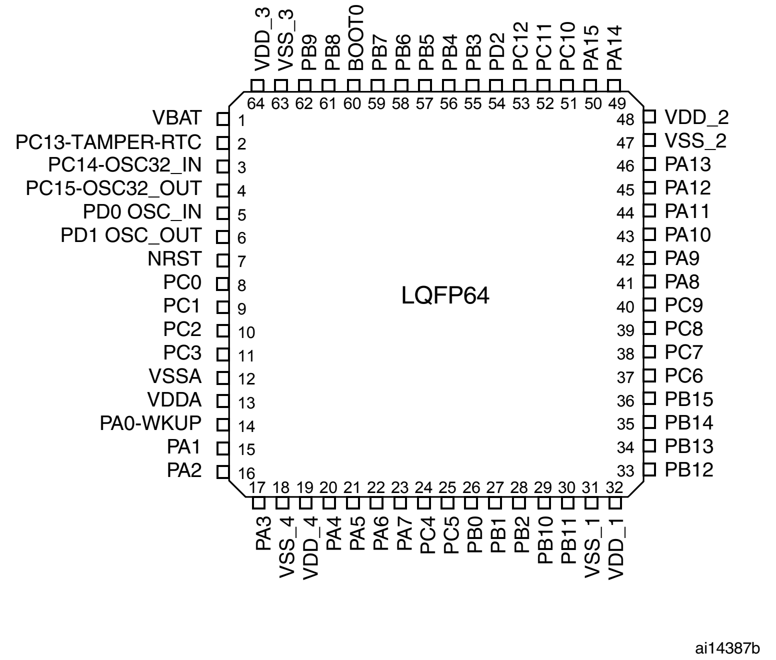


Figure 5. STM32F101xx Medium-density access line LQFP48 pinout

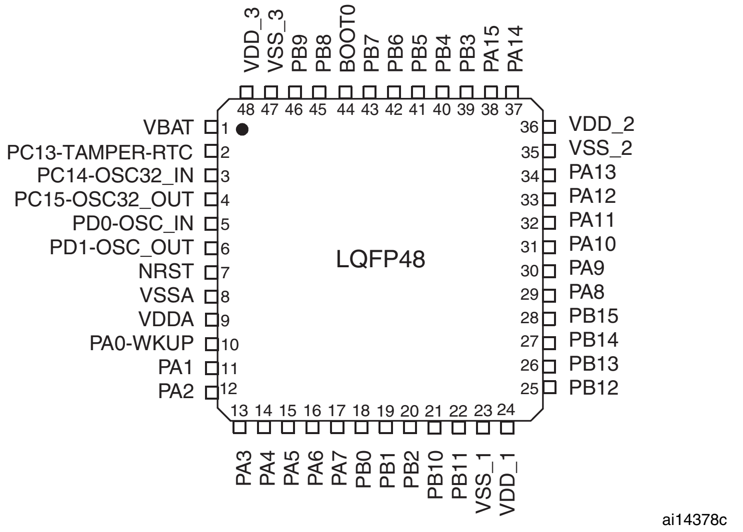


Figure 6. STM32F101xx access line VFQPFN36 pinout

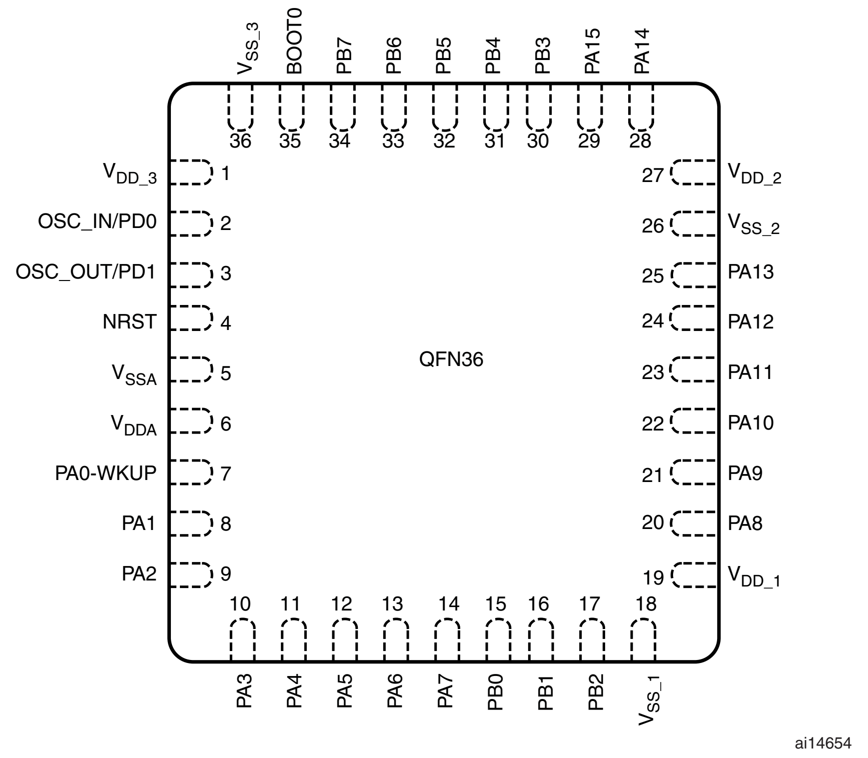


Table 4. Pin definitions

Pins				Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[3]	
LQFP48	LQFP64	LQFP100	VFQFPN36					Default	Remap
-	-	1	-	PE2	I/O	FT	PE2	TRACECLK	
-	-	2	-	PE3	I/O	FT	PE3	TRACED0	
-	-	3	-	PE4	I/O	FT	PE4	TRACED1	
-	-	4	-	PE5	I/O	FT	PE5	TRACED2	
-	-	5	-	PE6	I/O	FT	PE6	TRACED3	
1	1	6	-	V_{BAT}	S		V_{BAT}		
2	2	7	-	PC13-TAMPER-RTC[4]	I/O		PC13[5]	TAMPER-RTC	
3	3	8	-	PC14-OSC32_IN[4]	I/O		PC14[5]	OSC32_IN	
4	4	9	-	PC15-OSC32_OUT[4]	I/O		PC15[5]	OSC32_OUT	
-	-	10	-	V_{SS_5}	S		V_{SS_5}		
-	-	11	-	V_{DD_5}	S		V_{DD_5}		
5	5	12	2	OSC_IN	I		OSC_IN		
6	6	13	3	OSC_OUT	O		OSC_OUT		
7	7	14	4	NRST	I/O		NRST		
-	8	15	-	PC0	I/O		PC0	ADC_IN10	
-	9	16	-	PC1	I/O		PC1	ADC_IN11	
-	10	17	-	PC2	I/O		PC2	ADC_IN12	
-	11	18	-	PC3	I/O		PC3	ADC_IN13	
8	12	19	5	V_{SSA}	S		V_{SSA}		
-	-	20	-	V_{REF-}	S		V_{REF-}		
-	-	21	-	V_{REF+}	S		V_{REF+}		
9	13	22	6	V_{DDA}	S		V_{DDA}		
10	14	23	7	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS[8]/ ADC_IN0/ TIM2_CH1_ETR[8]	
11	15	24	8	PA1	I/O		PA1	USART2_RTS[8]/ ADC_IN1/TIM2_CH2[8]	
12	16	25	9	PA2	I/O		PA2	USART2_TX[8]/ ADC_IN2/TIM2_CH3[8]	
13	17	26	10	PA3	I/O		PA3	USART2_RX[8]/ ADC_IN3/TIM2_CH4[8]	
-	18	27	-	V_{SS_4}	S		V_{SS_4}		

Table 4. Pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)	
LQFP48	LQFP64	LQFP100	VFQFPN36					Default	Remap
-	19	28	-	V_{DD_4}	S		V_{DD_4}		
14	20	29	11	PA4	I/O		PA4	SPI1_NSS/ADC_IN4 USART2_CK(8)/	
15	21	30	12	PA5	I/O		PA5	SPI1_SCK/ADC_IN5	
16	22	31	13	PA6	I/O		PA6	SPI1_MISO/ADC_IN6/TIM3_CH1(8)	
17	23	32	14	PA7	I/O		PA7	SPI1_MOSI/ADC_IN7/TIM3_CH2(8)	
-	24	33		PC4	I/O		PC4	ADC_IN14	
-	25	34		PC5	I/O		PC5	ADC_IN15	
18	26	35	15	PB0	I/O		PB0	ADC_IN8/TIM3_CH3(8)	
19	27	36	16	PB1	I/O		PB1	ADC_IN9/TIM3_CH4(8)	
20	28	37	17	PB2/BOOT1	I/O	FT	PB2/BOOT1		
-	-	38	-	PE7	I/O	FT	PE7		
-	-	39	-	PE8	I/O	FT	PE8		
-	-	40	-	PE9	I/O	FT	PE9		
-	-	41	-	PE10	I/O	FT	PE10		
-	-	42	-	PE11	I/O	FT	PE11		
-	-	43	-	PE12	I/O	FT	PE12		
-	-	44	-	PE13	I/O	FT	PE13		
-	-	45	-	PE14	I/O	FT	PE14		
-	-	46	-	PE15	I/O	FT	PE15		
21	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL(6)/ USART3_TX(6) (8)	TIM2_CH3
22	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA(6)/ USART3_RX(6) (8)	TIM2_CH4
23	31	49	18	V_{SS_1}	S		V_{SS_1}		
24	32	50	19	V_{DD_1}	S		V_{DD_1}		
25	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS(6) (8)/ I2C2_SMBAI(6)/ USART3_CK(6) (8)	
26	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK(6)(8)/ USART3_CTS(6)(8)	
27	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO(6)(8)/ USART3_RTS(6)(8)	

Table 4. Pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)	
LQFP48	LQFP64	LQFP100	VFQFPN36					Default	Remap
28	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI(6) (8)	
-	-	55	-	PD8	I/O	FT	PD8		USART3_TX
-	-	56	-	PD9	I/O	FT	PD9		USART3_RX
-	-	57	-	PD10	I/O	FT	PD10		USART3_CK
-	-	58	-	PD11	I/O	FT	PD11		USART3_CTS
-	-	59	-	PD12	I/O	FT	PD12		TIM4_CH1 / USART3_RTS
-	-	60	-	PD13	I/O	FT	PD13		TIM4_CH2
-	-	61	-	PD14	I/O	FT	PD14		TIM4_CH3
-	-	62	-	PD15	I/O	FT	PD15		TIM4_CH4
-	37	63	-	PC6	I/O	FT	PC6		TIM3_CH1
	38	64	-	PC7	I/O	FT	PC7		TIM3_CH2
	39	65	-	PC8	I/O	FT	PC8		TIM3_CH3
-	40	66	-	PC9	I/O	FT	PC9		TIM3_CH4
29	41	67	20	PA8	I/O	FT	PA8	USART1_CK/MCO	
30	42	68	21	PA9	I/O	FT	PA9	USART1_TX(8)	
31	43	69	22	PA10	I/O	FT	PA10	USART1_RX(8)	
32	44	70	23	PA11	I/O	FT	PA11	USART1_CTS	
33	45	71	24	PA12	I/O	FT	PA12	USART1_RTS	
34	46	72	25	PA13/JTMS/SWDIO	I/O	FT	JTMS-SWDIO	PA13	
-	-	73	-	Not connected					
35	47	74	26	V_{SS_2}	S		V_{SS_2}		
36	48	75	27	V_{DD_2}	S		V_{DD_2}		
37	49	76	28	PA14/JTCK/SWCLK	I/O	FT	JTCK/SWCLK	PA14	
38	50	77	29	PA15/JTDI	I/O	FT	JTDI	PA15	TIM2_CH1_ETR/ SPI1_NSS
-	51	78		PC10	I/O	FT	PC10		USART3_TX
-	52	79		PC11	I/O	FT	PC11		USART3_RX
-	53	80		PC12	I/O	FT	PC12		USART3_CK
5	5	81	2	PD0	I/O	FT	OSC_IN(7)		
6	6	82	3	PD1	I/O	FT	OSC_OUT(7)		
	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	
-	-	84	-	PD3	I/O	FT	PD3		USART2_CTS

Table 4. Pin definitions (continued)

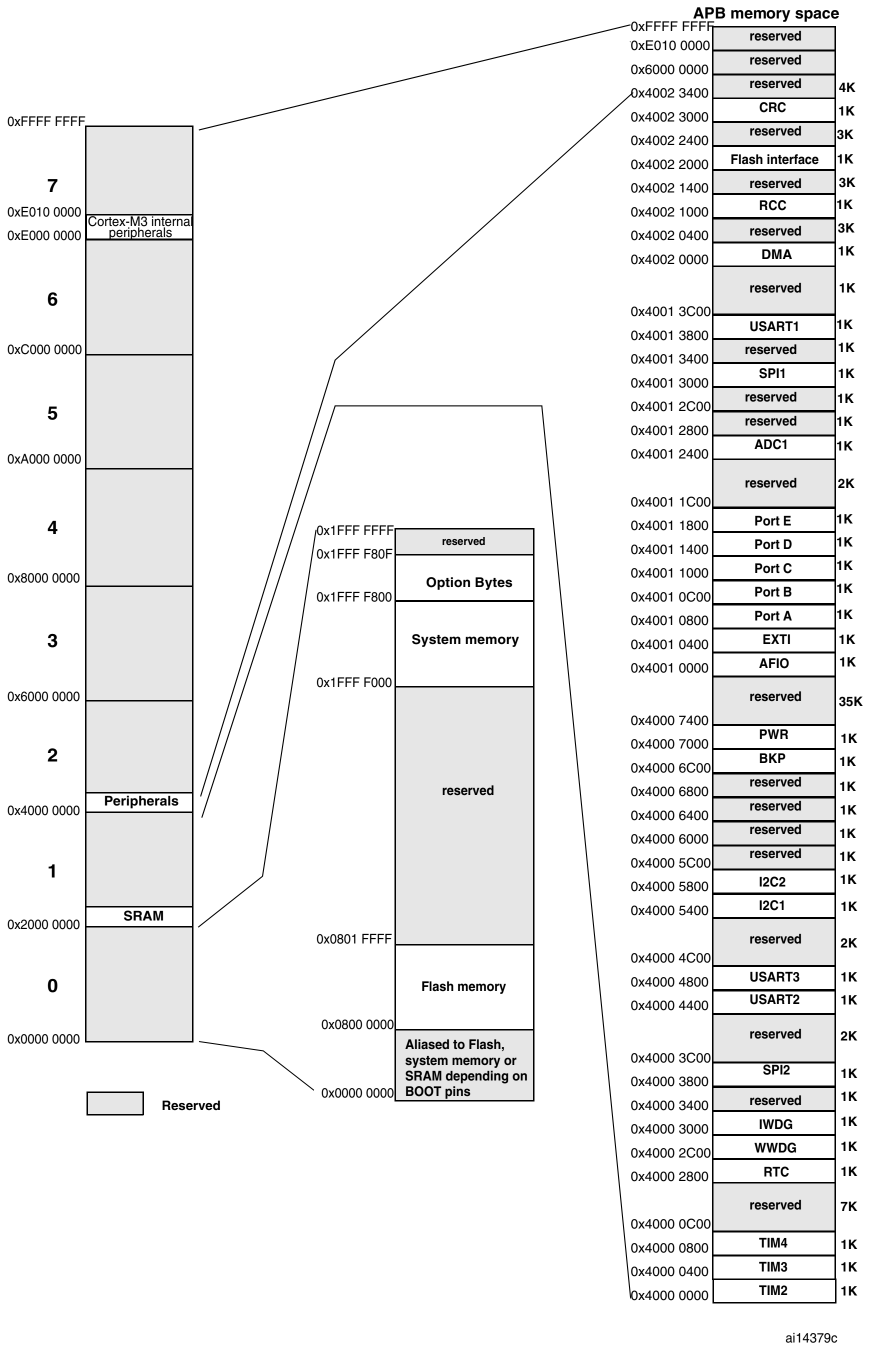
Pins				Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[3]	
LQFP48	LQFP64	LQFP100	VFQFPN36					Default	Remap
-	-	85	-	PD4	I/O	FT	PD4		USART2_RTS
-	-	86	-	PD5	I/O	FT	PD5		USART2_TX
-	-	87	-	PD6	I/O	FT	PD6		USART2_RX
-	-	88	-	PD7	I/O	FT	PD7		USART2_CK
39	55	89	30	PB3/JTDO	I/O	FT	JTDO	PB3/TRACESWO	TIM2_CH2 / SPI1_SCK
40	56	90	31	PB4/JNTRST	I/O	FT	JNTRST	PB4	TIM3_CH1 / SPI1_MISO
41	57	91	32	PB5	I/O		PB5	I2C1_SMBAI	TIM3_CH2 / SPI1_MOSI
42	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL[8]/ TIM4_CH1[6] [8]	USART1_TX
43	59	93	34	PB7	I/O	FT	PB7	I2C1_SDA[8]/ TIM4_CH2[6] [8]	USART1_RX
44	60	94	35	BOOT0	I		BOOT0		
45	61	95	-	PB8	I/O	FT	PB8	TIM4_CH3[6] [8]	I2C1_SCL
46	62	96	-	PB9	I/O	FT	PB9	TIM4_CH4[6] [8]	I2C1_SDA
-	-	97	-	PE0	I/O	FT	PE0	TIM4_ETR[6]	
-	-	98	-	PE1	I/O	FT	PE1		
47	63	99	36	V_{SS_3}	S		V_{SS_3}		
48	64	100	1	V_{DD_3}	S		V_{DD_3}		

1. I = input, O = output, S = supply, HiZ= high impedance.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to *Table 2 on page 8*.
4. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
6. Available only on devices with a Flash memory density equal or higher than 64 Kbytes.
7. The pins number 2 and 3 in the VFQFPN36 package, and 5 and 6 in the LQFP48 and LQFP64 packages are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.
8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

4 Memory mapping

The memory map is shown in *Figure 7*.

Figure 7. Memory map



5 Electrical characteristics

5.1 Test conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V $\leq V_{DD} \leq$ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

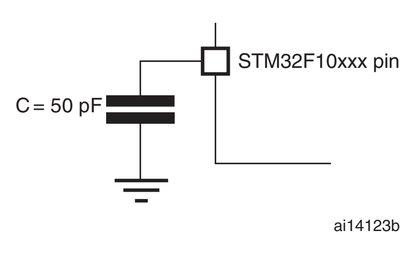
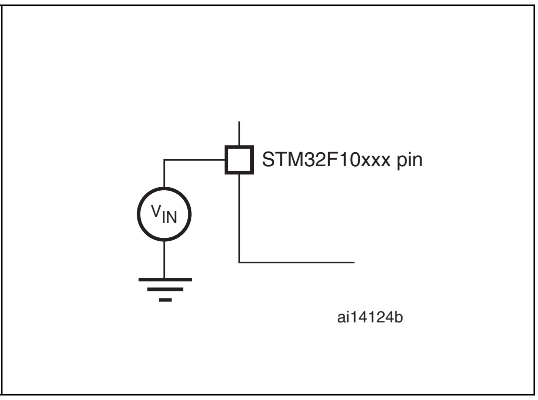
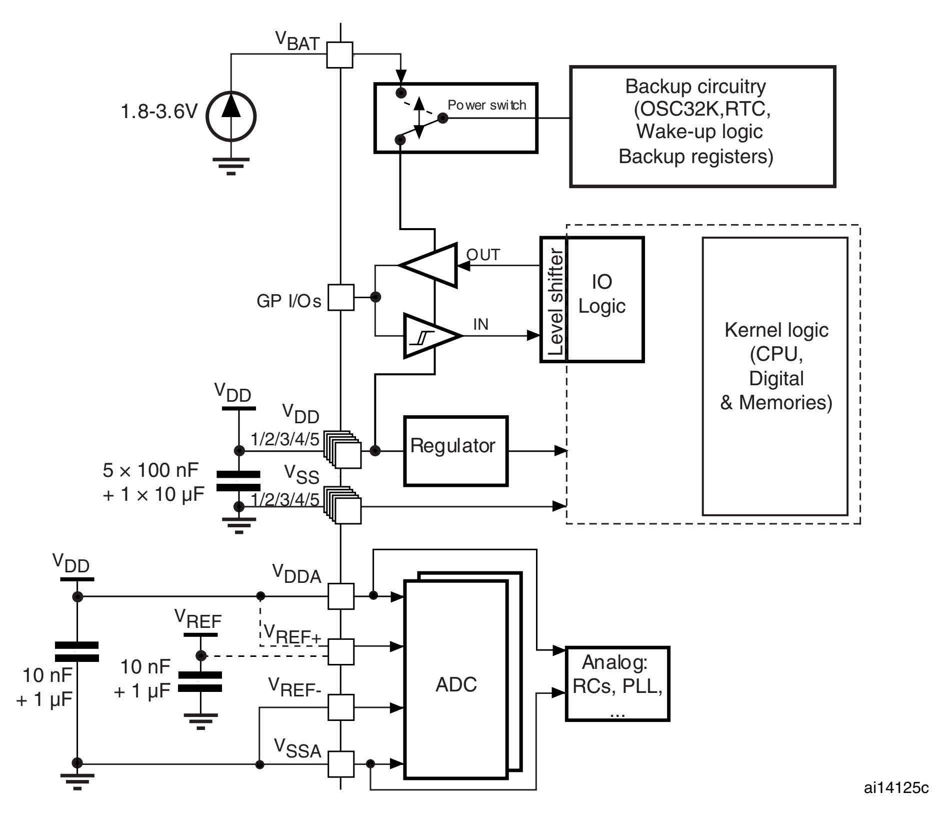


Figure 9. Pin input voltage



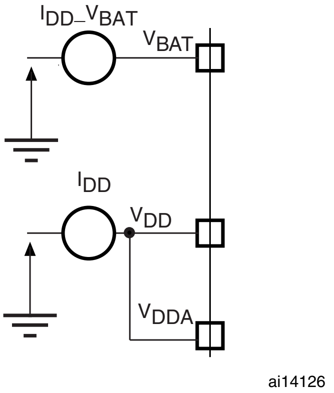
5.1.6 Power supply scheme

Figure 10. Power supply scheme



5.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 5: Voltage characteristics*, *Table 6: Current characteristics*, and *Table 7: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five volt tolerant pin(2)	V_{SS} –0.3	+5.5	
	Input voltage on any other pin(2)	V_{SS} –0.3	V_{DD}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different power pins	50	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	50	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded (see *Table 6: Current characteristics*). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$ (2)(3)	Injected current on NRST pin	± 5	
	Injected current on High-speed external OSC_IN and Low-speed external OSC_IN pins	± 5	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(4)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.16: 12-bit ADC characteristics*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	36	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	36	
f_{PCLK2}	Internal APB2 clock frequency		0	36	
V_{DD}	Standard operating voltage		2	3.6	V
V_{BAT}	Backup operating voltage		1.8	3.6	V
P_D	Power dissipation at T_A = 85 °C[1]	LQFP100		434	mW
		LQFP64		444	
		LQFP48		363	
		VFQFPN36		1110	
TA	Ambient temperature	Maximum power dissipation	–40	85	°C
		Low power dissipation[2]	–40	105	°C
TJ	Junction temperature range		–40	105	°C

1. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 68*).

2. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 68*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 9. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	µs/V
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 10* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis			40		mV
$t_{RSTTEMPO}$(2)	Reset temporization		1.5	2.5	3.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 11. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage			5.1	17.1	µs

1. Shortest sampling time can be determined in the application by multiple iterations.

5.3.5 Supply current characteristics

The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 12. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	36 MHz	28.6	mA
			24 MHz	19.9	
			16 MHz	14.7	
			8 MHz	8.6	
		External clock (4), all peripherals Disabled	36 MHz	19.8	
			24 MHz	13.9	
			16 MHz	10.7	
			8 MHz	6.8	

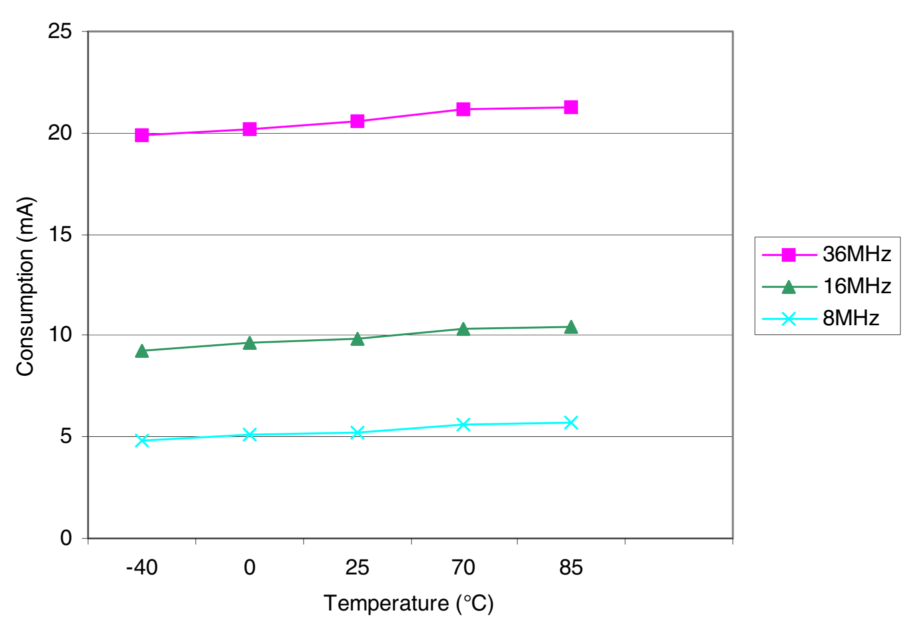
1. Data based on characterization results, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.

Table 13. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Run mode	External clock [1], all peripherals enabled	36 MHz[2]	24	mA
			24 MHz[6]	17.5	
			16 MHz[6]	12.5	
			8 MHz[6]	7.5	
		External clock[4] all peripherals disabled[6]	36 MHz	16	
			24 MHz	11.5	
			16 MHz	8.5	
			8 MHz	5.5	

1. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.
2. Based on characterization, not tested in production.

Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled



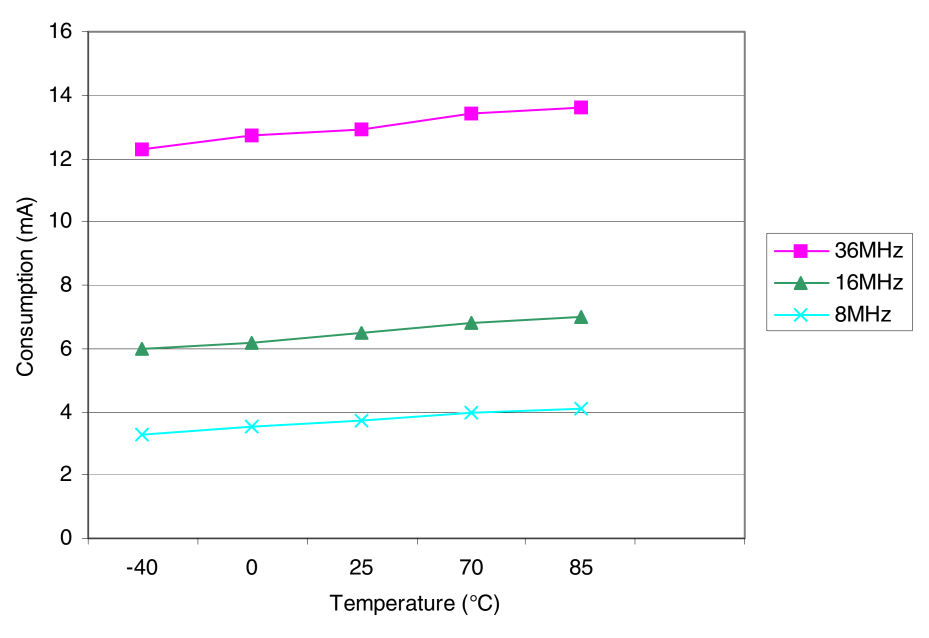


Figure 13. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Sleep mode	External clock[1] all peripherals enabled	36 MHz[2]	15.5	mA
			24 MHz[5]	11.5	
			16 MHz[5]	8.5	
			8 MHz[5]	5.5	
		External clock[4], all peripherals disabled[5]	36 MHz	5	
			24 MHz	4.5	
			16 MHz	4	
			8 MHz	3	

1. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.
2. Based on characterization, not tested in production.

Table 15. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max	Unit
			V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	23.5	24	200(2)	µA
		Regulator in Low-Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	13.5	14	180(6)	
	Supply current in Standby mode(3)	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.7	2	4(6)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	1.9(4)	

1. Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V, unless otherwise specified.
2. Data based on characterization results, tested in production at V_{DD}max and f_{HCLK} max.
3. To have the Standby consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator and RTC ON) to I_{DD} Standby (when V_{DD} is present the Backup Domain is powered by V_{DD} supply).
4. Data based on characterization results, not rested in production.

Figure 14. Current consumption in Stop mode with regulator in Run mode versus temperature at V_{DD} = 3.3 V and 3.6 V

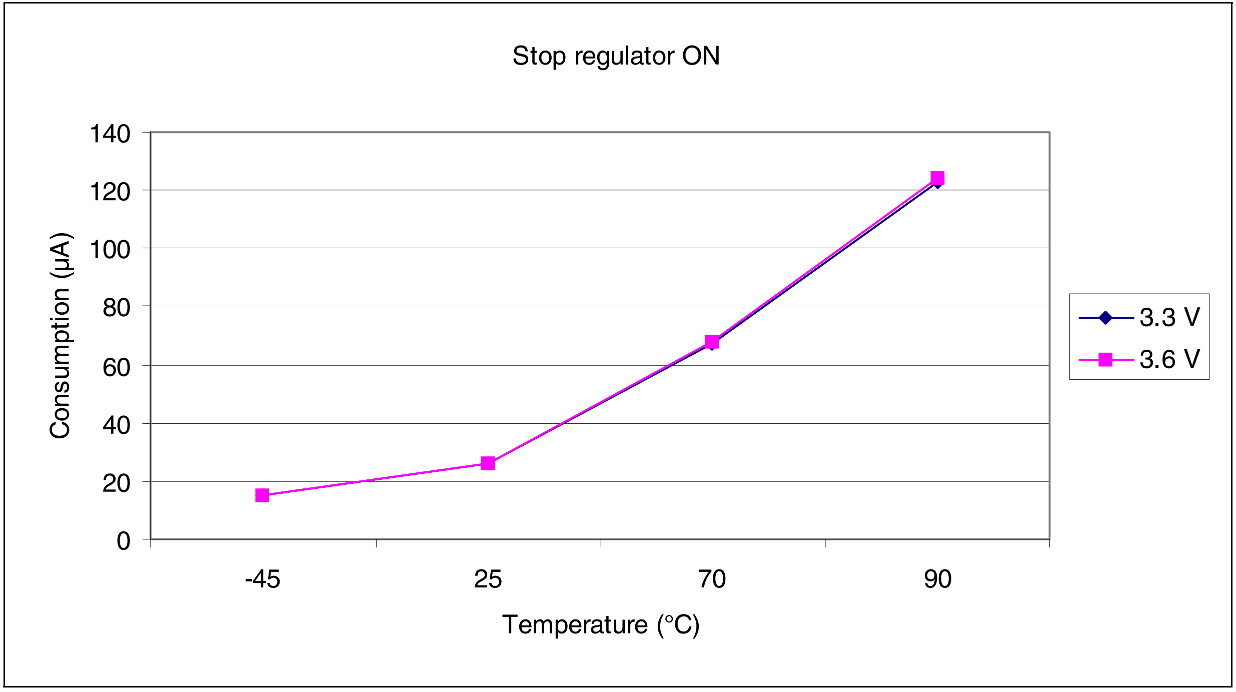


Figure 15. Current consumption in Stop mode with regulator in Low-power mode versus temperature at V_{DD} = 3.3 V and 3.6 V

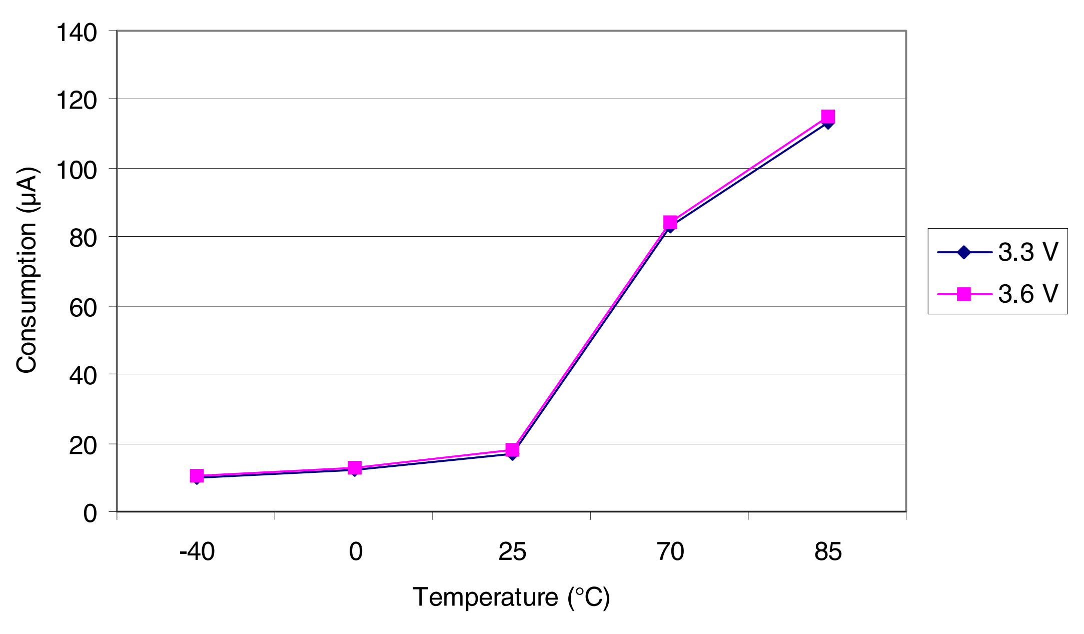
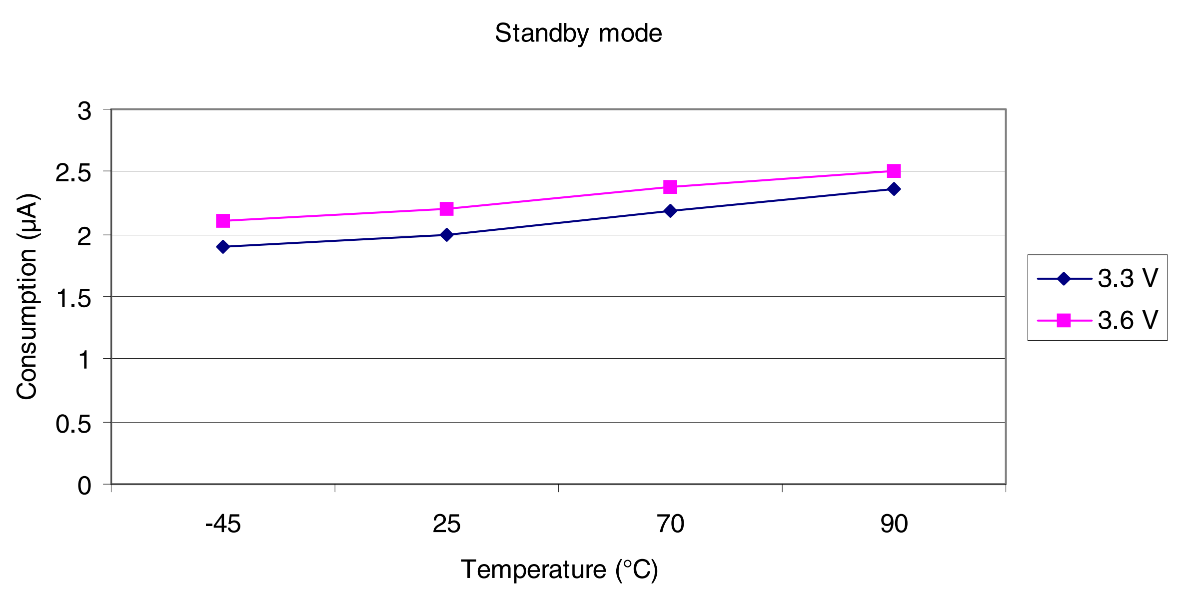


Figure 16. Current consumption in Standby mode versus temperature at V_{DD} = 3.3 V and 3.6 V



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 16* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 16. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ[1]	Typ[1]	Unit
				All peripherals enabled[2]	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock[3]	36 MHz	19	14.8	mA
			24 MHz	12.9	10.1	
			16 MHz	9.3	7.4	
			8 MHz	5.5	4.6	
			4 MHz	3.3	2.8	
			2 MHz	2.2	1.9	
			1 MHz	1.6	1.45	
			500 kHz	1.3	1.25	
			125 kHz	1.08	1.06	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	18.3	14.1	
			24 MHz	12.2	9.5	
			16 MHz	8.5	6.8	
			8 MHz	4.9	4	
			4 MHz	2.7	2.2	
			2 MHz	1.6	1.4	
			1 MHz	1.02	0.9	
			500 kHz	0.73	0.67	
			125 kHz	0.5	0.48	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 17. Typical current consumption in Sleep mode, code with data processing code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ[1] All peripherals enabled[2]	Typ[1] All peripherals disabled	Unit
I_{DD}	Supply current in Sleep mode	External clock[3]	36 MHz	7.6	3.1	mA
			24 MHz	5.3	2.3	
			16 MHz	3.8	1.8	
			8 MHz	2.1	1.2	
			4 MHz	1.6	1.1	
			2 MHz	1.3	1	
			1 MHz	1.11	0.98	
			500 kHz	1.04	0.96	
			125 kHz	0.98	0.95	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	7	2.5	
			24 MHz	4.8	1.8	
			16 MHz	3.2	1.2	
			8 MHz	1.6	0.6	
			4 MHz	1	0.5	
			2 MHz	0.72	0.47	
			1 MHz	0.56	0.44	
			500 kHz	0.49	0.42	
			125 kHz	0.43	0.41	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 18. Typical current consumption in Standby mode

Symbol	Parameter	Conditions	V_{DD}	Typ[1]	Unit
I_{DD}	Supply current in Standby mode[2]	Low-speed internal RC oscillator and independent watchdog OFF	3.3 V	2	µA
			2.4 V	1.5	
		Low-speed internal RC oscillator and independent watchdog ON	3.3 V	3.4	
			2.4 V	2.6	
		Low-speed internal RC oscillator ON, independent watchdog OFF	3.3 V	3.2	
			2.4 V	2.4	

1. Typical values are measures at $T_A = 25$ °C.
2. To obtain Standby consumption with RTC ON, add $I_{DD\_}V_{BAT}$ (Low-speed oscillator, RTC ON) to I_{DD} Standby.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 5*.

Table 19. Peripheral current consumption

Peripheral		Typical consumption at 25 °C(1)	Unit
APB1	TIM2	0.6	mA
	TIM3	0.6	
	TIM4	0.6	
	SPI2	0.08	
	USART2	0.21	
	USART3	0.21	
	I2C1	0.18	
	I2C2	0.18	
APB2	GPIO A	0.21	
	GPIO B	0.21	
	GPIO C	0.21	
	GPIO D	0.21	
	GPIO E	0.21	
	ADC1(2)	1.4	
	SPI1	0.24	
	USART1	0.35	

1. f_{HCLK} = 36 MHz, $f_{APB1} = f_{HCLK/2}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. Specific conditions for ADC: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$, ADON bit in the ADC_CR2 register is set to 1.

5.3.6 External clock source characteristics

High-speed user external clock

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 8*.

Table 20. High-speed user external (HSE) clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)			8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)				5	
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA

1. Value based on design simulation and/or technology characteristics. It is not tested in production.

Low-speed user external clock

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 8*.

Table 21. Low-speed user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)				5	
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA

1. Value based on design simulation and/or technology characteristics. It is not tested in production.

Figure 17. High-speed external clock source AC timing diagram

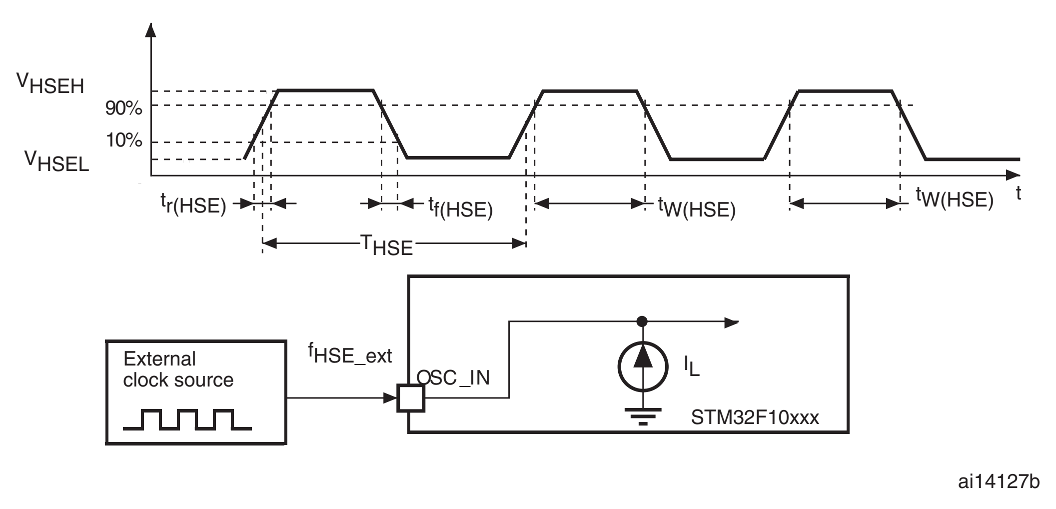
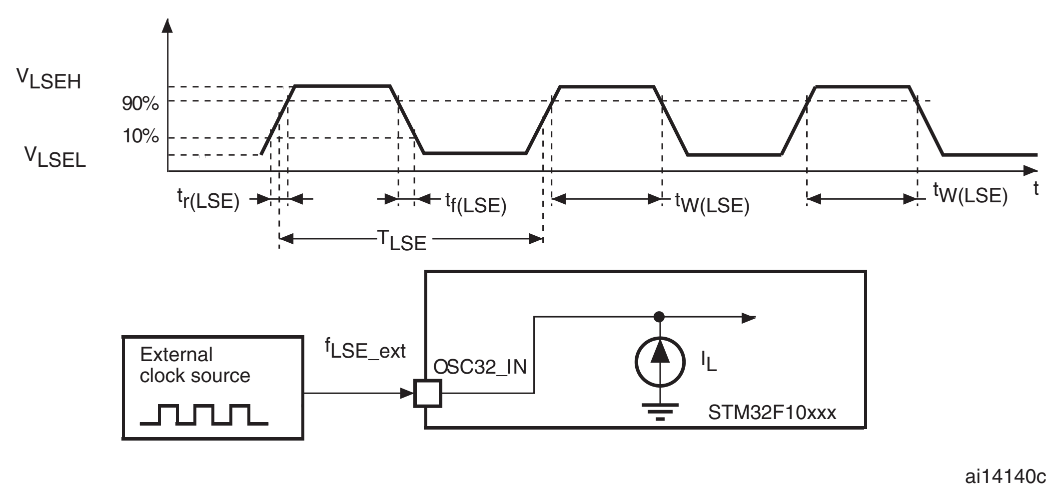


Figure 18. Low-speed external clock source AC timing diagram



High-speed external clock

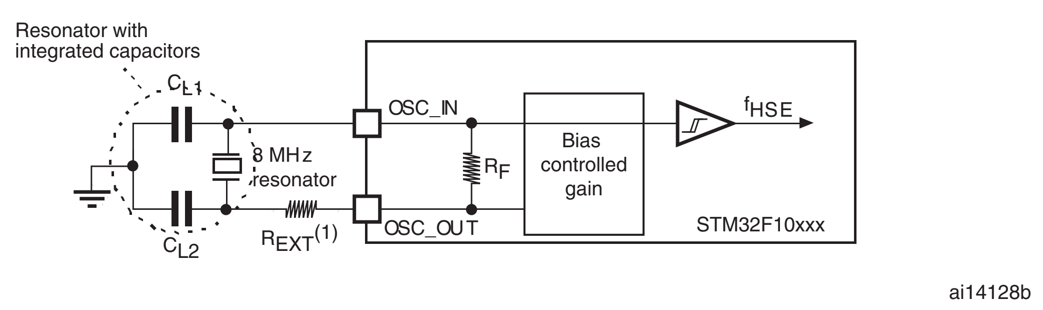
The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. HSE 4-16 MHz oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	16	MHz
R_F	Feedback resistor			200		kΩ
C_{L1} C_{L2}(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω		30		pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load			1	mA
g_m(4)	Oscillator transconductance	Startup	25			mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and $C_{L2,}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. Based on characterization results, not tested in production.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 19. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics. Typical value is in the range of 5 to $6R_S$.

Low-speed external clock

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

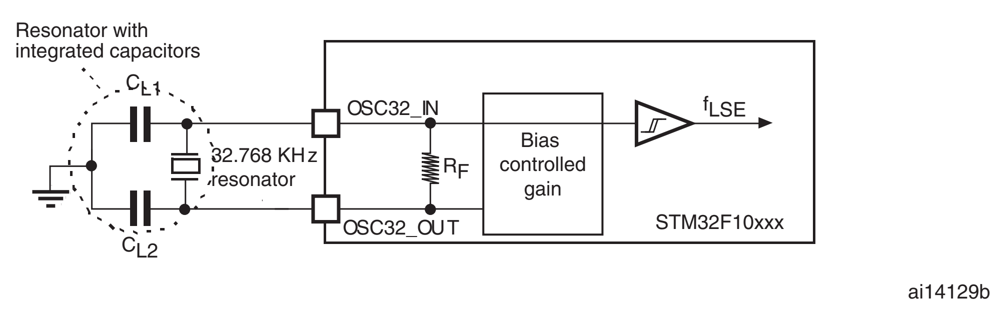
Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor			5		MΩ
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)[1]	R_S = 30 KΩ			15	pF
I_2	LSE driving current	V_{DD} = 3.3 V $V_{IN} = V_{SS}$			1.4	µA
g_m	Oscillator transconductance		5			µA/V
$t_{SU(LSE)}$[2]	Startup time	V_{DD} is stabilized		3		s

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768 kHz. Refer to crystal manufacturer for more details

2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 20. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 85 °C		±1	±3	%
		T_A = –10 to 85 °C		±1	±2.5	%
		T_A = 0 to 70 °C		±1	±2.2	%
		at T_A = 25 °C		±1	±2	%
$t_{su(HSI)}$	HSI oscillator startup time		1		2	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100	µA

1. V_{DD} = 3.3 V, T_A = -40 to 85 °C unless otherwise specified.

LSI low speed internal RC oscillator

Table 25. LSI oscillator characteristics [1]

Symbol	Parameter	Conditions	Min[2]	Typ	Max	Unit
f_{LSI}	Frequency		30	40	60	kHz
$t_{su(LSI)}$	LSI oscillator startup time				85	µs
$I_{DD(LSI)}$	LSI oscillator power consumption			0.65	1.2	µA

1. V_{DD} = 3 V, T_A = -40 to 85 °C unless otherwise specified.
2. Value based on device characterization, not tested in production.

Wakeup time from low power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	Wakeup on HSI RC clock	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	HSI RC wakeup time = 2 µs	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	HSI RC wakeup time = 2 µs, Regulator wakeup from LP mode time = 5 µs	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI RC wakeup time = 2 µs, Regulator wakeup from power down time = 38 µs	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 27. PLL characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock			8.0		MHz
	PLL input clock duty cycle		40		60	%
f_{PLL_OUT}	PLL multiplier output clock		16		36	MHz
t_{LOCK}	PLL lock time				200	µs

1. Data based on device characterization, not tested in production.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = -40 to 85 °C unless otherwise specified.

Table 28. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = -40 to +85 °C	40	52.5	70	µs
t_{ERASE}	Page (1kB) erase time	T_A = -40 to +85 °C	20		40	ms
t_{ME}	Mass erase time	T_A = -40 to +85 °C	20		40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 36MHz with 2 wait states, V_{DD} = 3.3 V			20	mA
		Write / Erase modes f_{HCLK} = 36 MHz, V_{DD} = 3.3 V			5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V			50	µA
V_{prog}	Programming voltage		2		3.6	V

1. Values based on characterization and not tested in production.

Table 29. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END}	Endurance	T_A = –40 °C to 85 °C	10			kcycles
t_{RET}	Data retention	T_A = 85 °C, 1 kcycle(2)	30			Years
		T_A = 55 °C, 10 kcycle(4)	20			

1. Values based on characterization not tested in production.
2. Cycling performed over the whole temperature range.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 30*. They are based on the EMS levels and classes defined in application note AN1709.

Table 30. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK}=48 MHz conforms to IEC 1000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 48 MHz conforms to IEC 1000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

Table 31. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/36 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with SAE J 1752/3	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 32. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Values based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 33. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 34. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(1)	TTL ports	–0.5		0.8	V
V_{IH}	Standard IO input high level voltage(1)		2		V_{DD}+0.5	
	IO FT(2) input high level voltage(1)		2		5.5V	
V_{IL}	Input low level voltage(1)	CMOS ports	–0.5		0.35 V_{DD}	V
V_{IH}	Input high level voltage(1)		0.65 V_{DD}		V_{DD}+0.5	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(3)		200			mV
	IO FT Schmitt trigger voltage hysteresis(3)		5% V_{DD}(4)			mV
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os			±1	μA
		V_{IN} = 5 V I/O FT			3	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(6)	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. Values based on characterization results, and not tested in production.
2. FT = Five-volt tolerant.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. With a minimum of 100 mV.
5. Leakage could be higher than max. if negative current is injected on adjacent pins.
6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed V_{OL}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 6*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 6*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 35. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port, I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(2)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(3) 2.7 V < V_{DD} < 3.6 V		1.3	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3		
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(3) 2 V < V_{DD} < 2.7 V		0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4		

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 21* and *Table 36*, respectively.

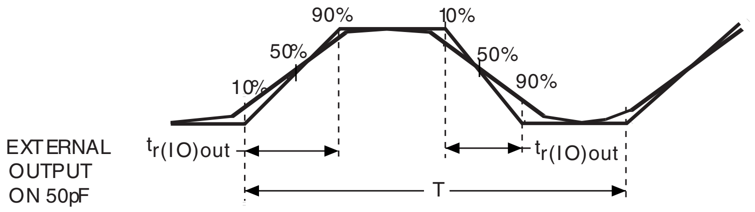
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 21*.
3. Values based on design simulation and validated on silicon, not tested in production.

Figure 21. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 34*).

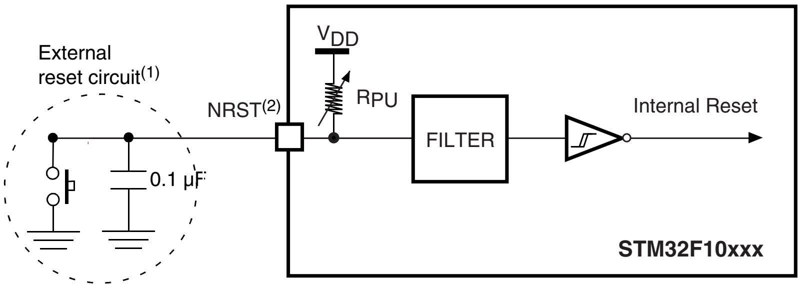
Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 37. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage		–0.5		0.8	V
$V_{IH(NRST)}$	NRST Input high level voltage		2		V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		
R_{PU}	Weak pull-up equivalent resistor[1]	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$	NRST Input filtered pulse[2]				100	ns
$V_{NF(NRST)}$	NRST Input not filtered pulse[2]		300			ns

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Values guaranteed by design, not tested in production.

Figure 22. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 37*. Otherwise the reset will not be taken into account by the device.

5.3.14 TIM timer characteristics

The parameters given in *Table 38* are guaranteed by fabrication.

Refer to *Section 5.3.12: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	27.8		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 36 MHz	0	18	MHz
Res_{TIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz	0.0278	1820	µs
t_{MAX_COUNT}	Maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 36 MHz		119.2	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

5.3.15 Communications interfaces

I^{2}C interface characteristics

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 8*.

The STM32F101xx Medium-density access line I^{2}C interface meets the requirements of the standard I^{2}C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

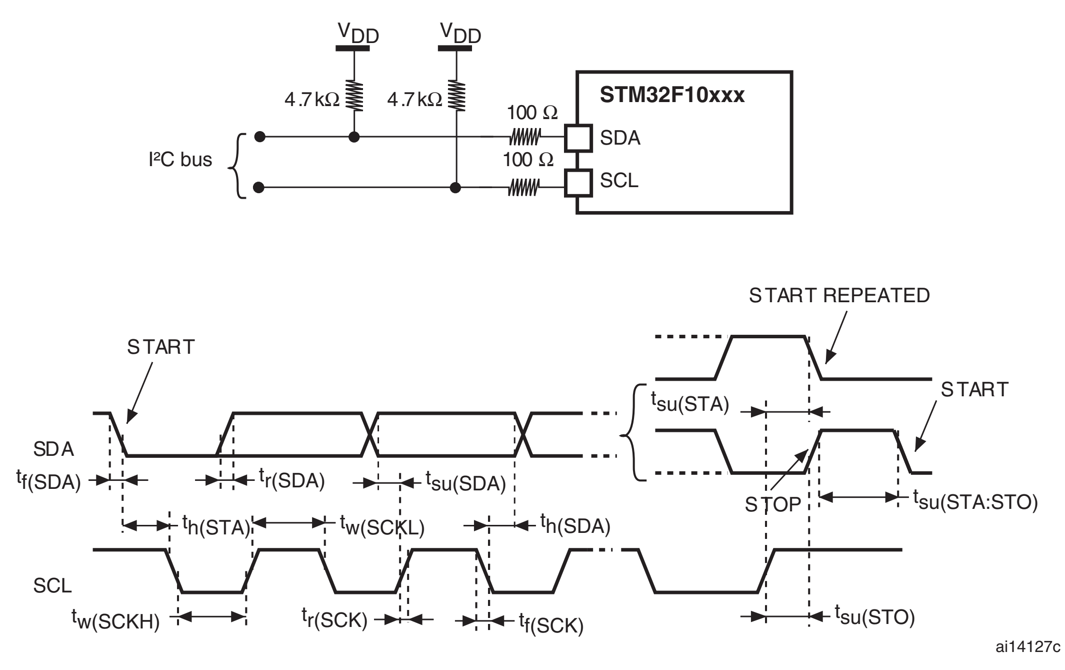
The I^{2}C characteristics are described in *Table 39*. Refer also to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 39. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20+0.1C_b$	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20+0.1C_b$	300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		μs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		μs
C_b	Capacitive load for each bus line		400		400	pF

1. Values based on standard I^2C protocol requirement, not tested in production.
2. f_{PCLK1} must be higher than 2 MHz to achieve the maximum standard mode I^2C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I^2C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 23. I^2C bus AC waveforms and measurement circuit[1]



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = 3.3 V)[1][2]

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I^2C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 8*.

Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	18	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 t_{PCLK}		
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	18		
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (2)	Data input setup time Master mode	SPI1	1		
		SPI2	5		
$t_{su(SI)}$(2)	Data input setup time Slave mode		1		
$t_{h(MI)}$ (2)	Data input hold time Master mode	SPI1	1		
		SPI2	5		
$t_{h(SI)}$(2)	Data input hold time Slave mode		3		
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 24 MHz	0	4 t_{PCLK}	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$(2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$(2)		Master mode (after enable edge)	4		

1. Remapped SPI1 characteristics to be determined.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 24. SPI timing diagram - slave mode and CPHA=0

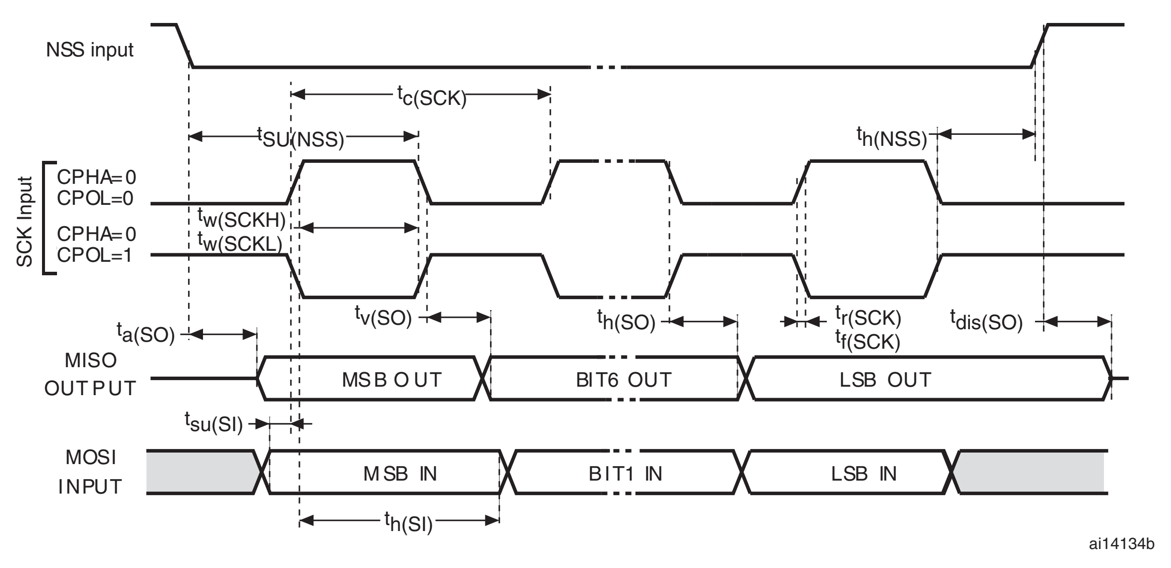
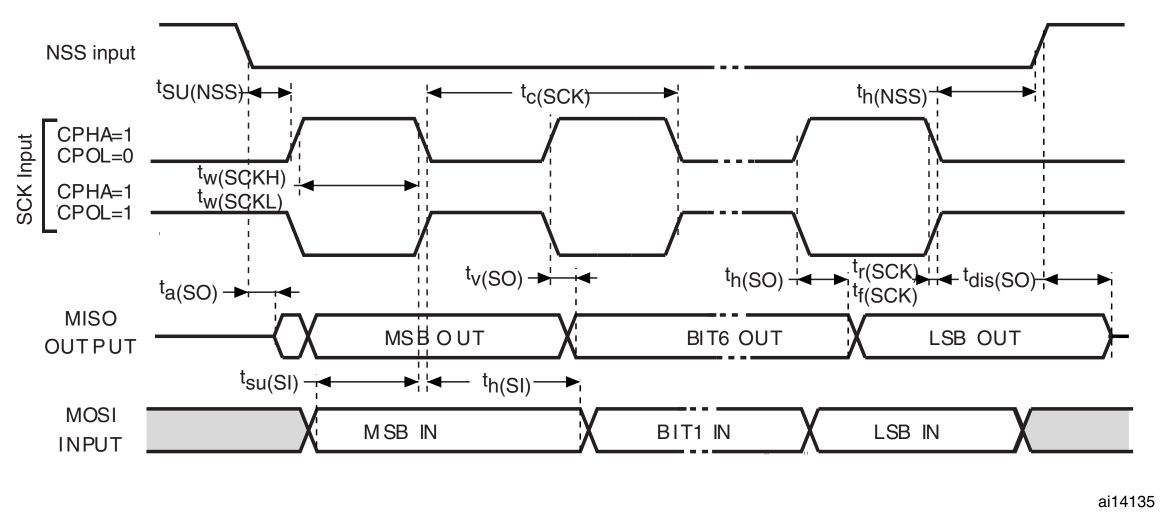
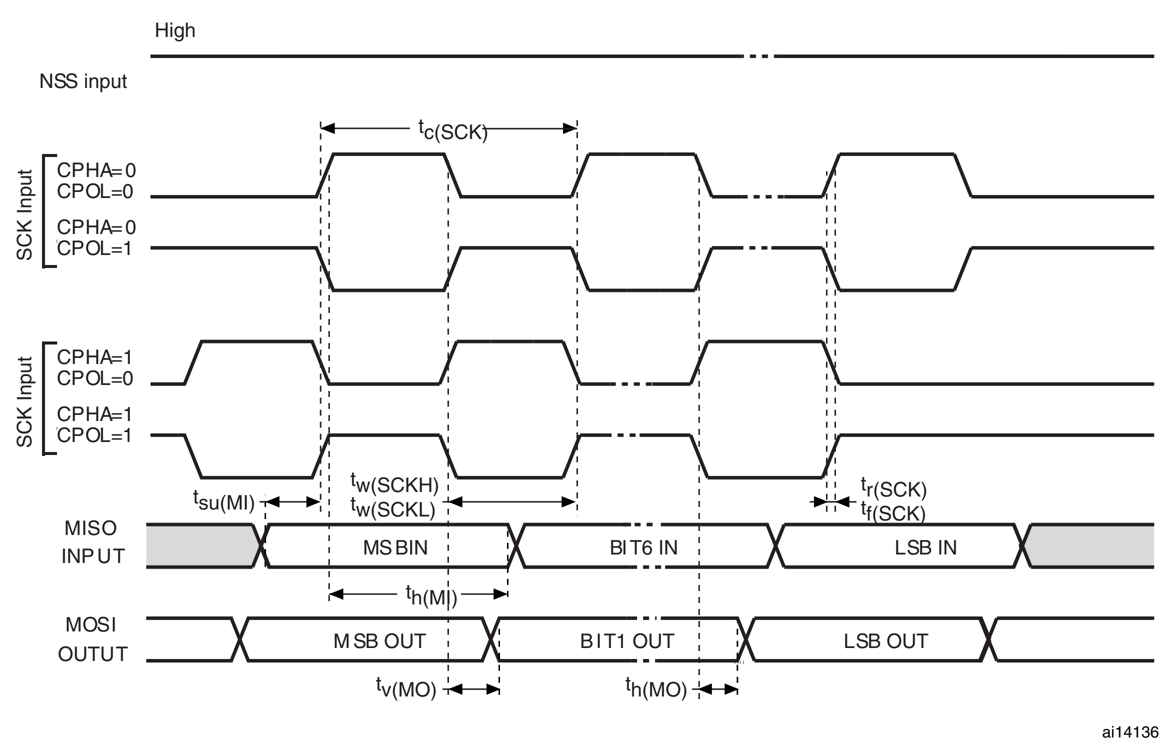


Figure 25. SPI timing diagram - slave mode and CPHA=1[(1)]



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 26. SPI timing diagram - master mode[1]



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 8*.

Note: It is recommended to perform a calibration after each power-up.

Table 42. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	ADC power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin			160(1)	220(1)	µA
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S(2)	Sampling rate		0.05		1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
R_{AIN}(2)	External input impedance		See *Equation 1* and *Table 43*			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				5	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz			0.214	µs
					3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz			0.143	µs
					2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pin descriptions* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 42*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 43. R_{AIN} max for f_{ADC} = 10 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	1.2
7.5	0.54	10
13.5	0.96	19
28.5	2.04	41
41.5	2.96	60
55.5	3.96	80
71.5	5.11	104
239.5	17.1	350

1. Data guaranteed by design, not tested in production.

Table 44. ADC accuracy - limited test conditions(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error(3)	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration $V_{REF+} = V_{DDA}$	±1.3	±2	LSB
EO	Offset error(3)		±1	±1.5	
EG	Gain error(3)		±0.5	±1.5	
ED	Differential linearity error(3)		±0.7	±1	
EL	Integral linearity error(3)		±0.8	±1.5	

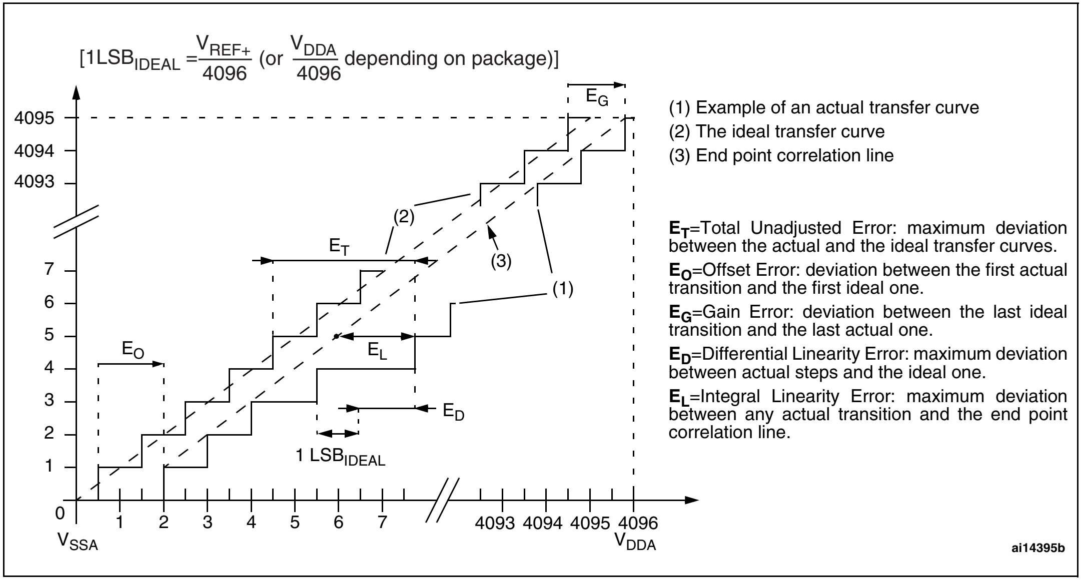
1. ADC DC accuracy values are measured after internal calibration.
2. Data based on characterization, not tested in production.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.

Table 45. ADC accuracy(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error(4)	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error(3)		±1.5	±2.5	
EG	Gain error(3)		±1.5	±3	
ED	Differential linearity error(3)		±1	±2	
EL	Integral linearity error(3)		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. Data based on characterization, not tested in production.
4. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.

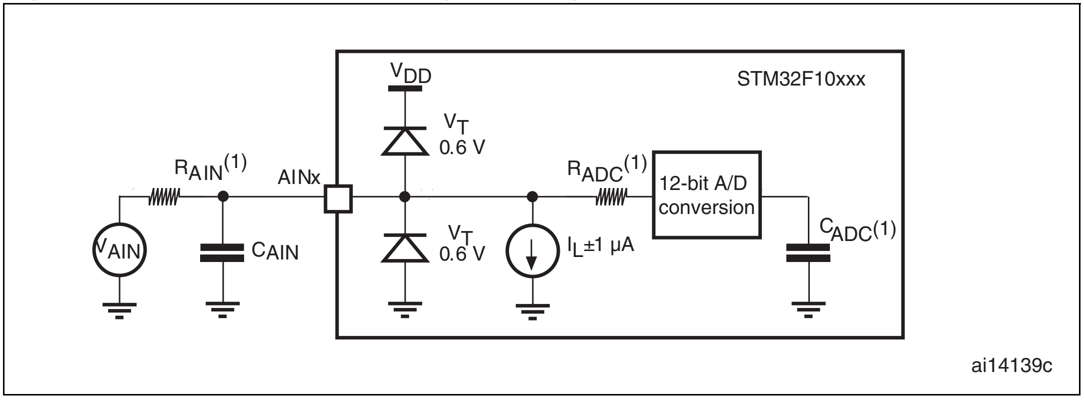
Figure 27. ADC accuracy characteristics



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T=Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
E_O=Offset Error: deviation between the first actual transition and the first ideal one.
E_G=Gain Error: deviation between the last ideal transition and the last actual one.
E_D=Differential Linearity Error: maximum deviation between actual steps and the ideal one.
E_L=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 28. Typical connection diagram using the ADC

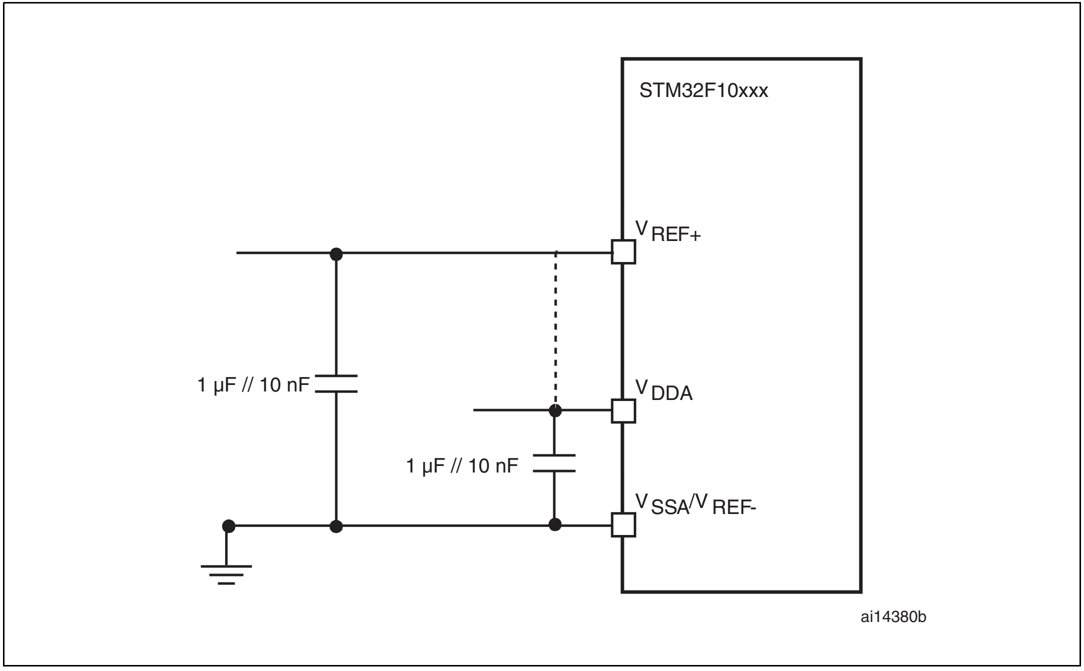


1. Refer to *Table 42* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{PARASITIC}$ must be added to C_{AIN}. It represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

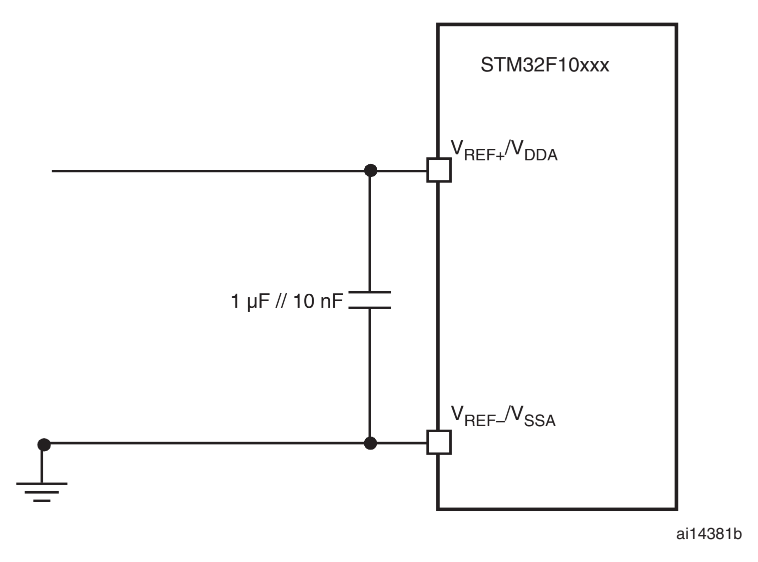
Power supply decoupling should be performed as shown in *Figure 29* or *Figure 30*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 29. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 30. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.17 Temperature sensor characteristics

Table 46. TS characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature			±1	±2	°C
Avg_Slope(1)	Average slope		4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25°C		1.34	1.43	1.52	V
t_{START}(2)	Startup time		4		10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature			2.2	17.1	µs

1. Guaranteed by characterization, not tested in production.
2. Data guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers the STM32F101xx in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.
The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 31. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package outline[1]

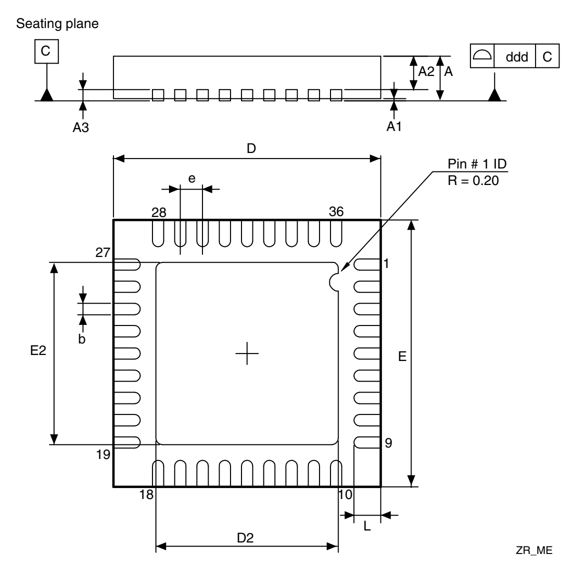
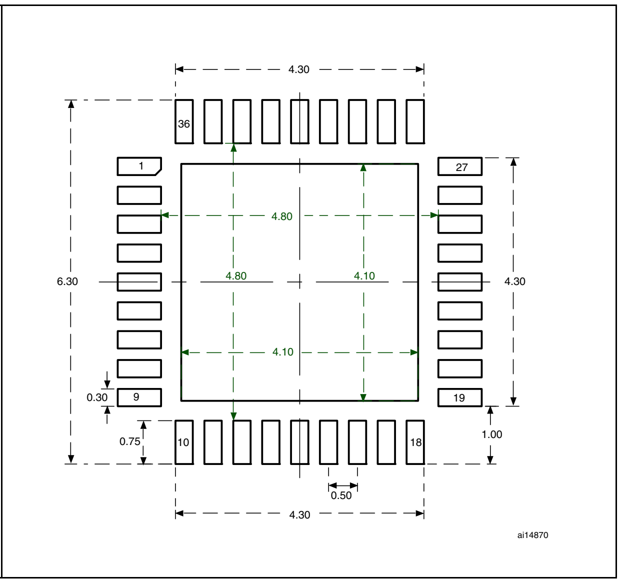


Figure 32. Recommended footprint (dimensions in mm)[1][2][3]



1. Drawing is not to scale.
2. The back-side pad is not internally connected to the V_{SS} or V_{DD} power pads.
3. There is an exposed die pad on the underside of the VFQFPN package. It should be soldered to the PCB. All leads should also be soldered to the PCB.

Table 47. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1		0.020	0.050		0.0008	0.0020
A2		0.650	1.000		0.0256	0.0394
A3		0.250			0.0098	
b	0.180	0.230	0.300	0.0071	0.0091	0.0118
D	5.875	6.000	6.125	0.2313	0.2362	0.2411
D2	1.750	3.700	4.250	0.0689	0.1457	0.1673
E	5.875	6.000	6.125	0.2313	0.2362	0.2411
E2	1.750	3.700	4.250	0.0689	0.1457	0.1673
e	0.450	0.500	0.550	0.0177	0.0197	0.0217
L	0.350	0.550	0.750	0.0138	0.0217	0.0295
ddd		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 33. LQFP100, 100-pin low-profile quad flat package outline[1]

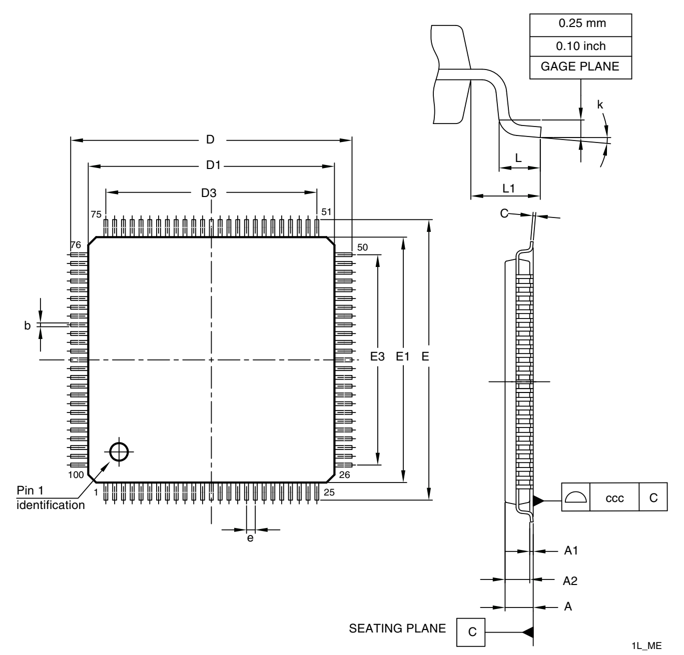
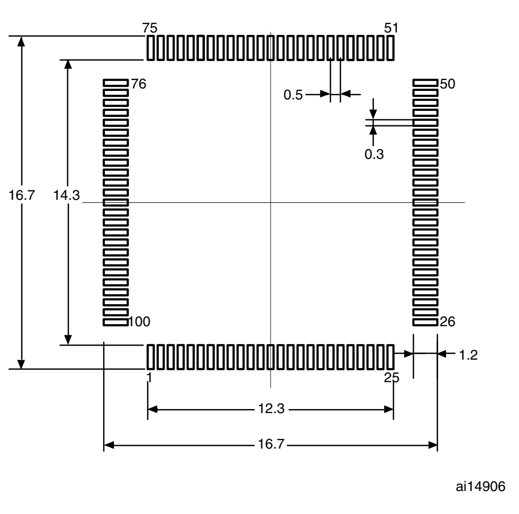


Figure 34. Recommended footprint[1][2]



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 48. LQPF100 – 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.60			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.40	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.2		0.0035	0.0079
D	16.00	15.80	16.2	0.6299	0.622	0.6378
D1	14.00	13.80	14.2	0.5512	0.5433	0.5591
D3	12.00			0.4724		
E	16.00	15.80	16.2	0.6299	0.622	0.6378
E1	14.00	13.80	14.2	0.5512	0.5433	0.5591
E3	12.00			0.4724		
e	0.50			0.0197		
L	0.60	0.45	0.75	0.0236	0.0177	0.0295
L1	1.00			0.0394		
k	3.5°	0°	7°	3.5°	0.0°	7.0°
ccc	0.08			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. LQFP64 – 64 pin low-profile quad flat package outline(1)

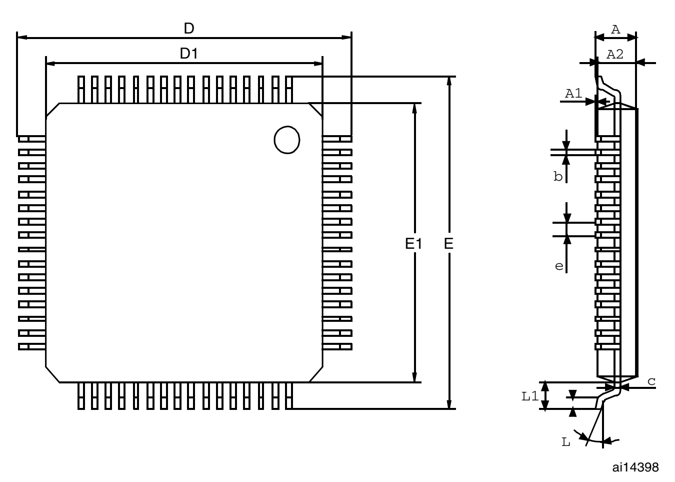
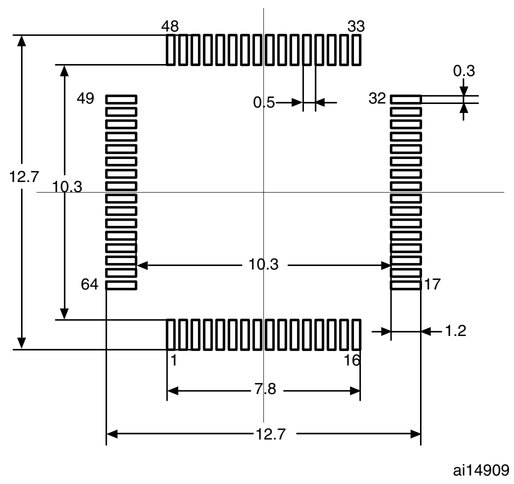


Figure 36. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 49. LQFP64 – 64-pin low-profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
Number of pins						
N	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. LQFP48 – 48-pin low-profile quad flat package outline(1)

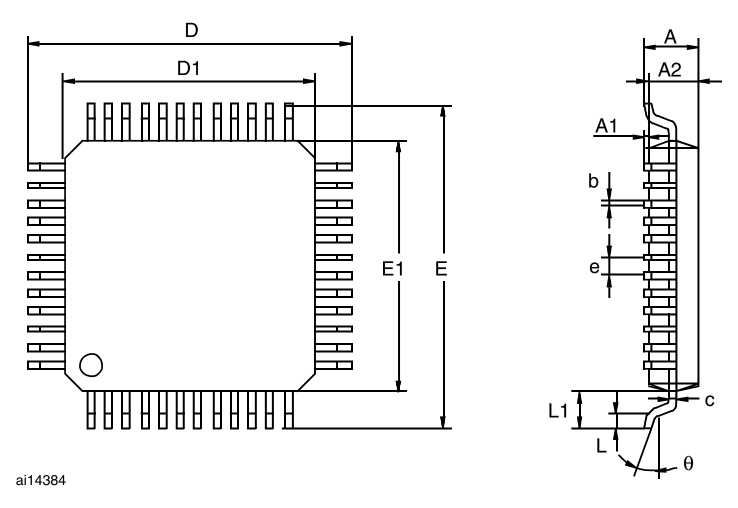
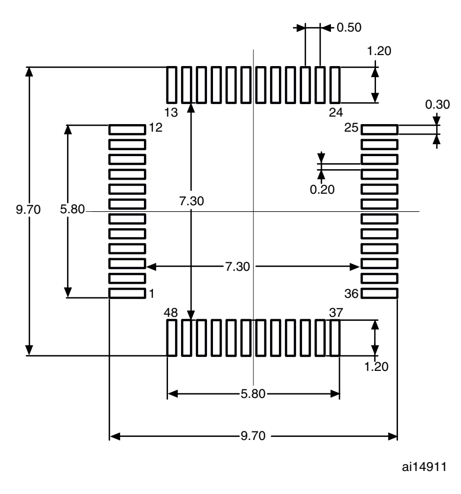


Figure 38. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 50. LQFP48 – 48-pin low-profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
C	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
Number of pins						
N	48					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 8: General operating conditions on page 29*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max x } \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in ° C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in ° C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma\ (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 51. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient VFQFPN 36 - 6 x 6 mm / 0.5 mm pitch	18	

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

6.2.2 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 52: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F101xx junction temperature range.

Example: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 464 mW

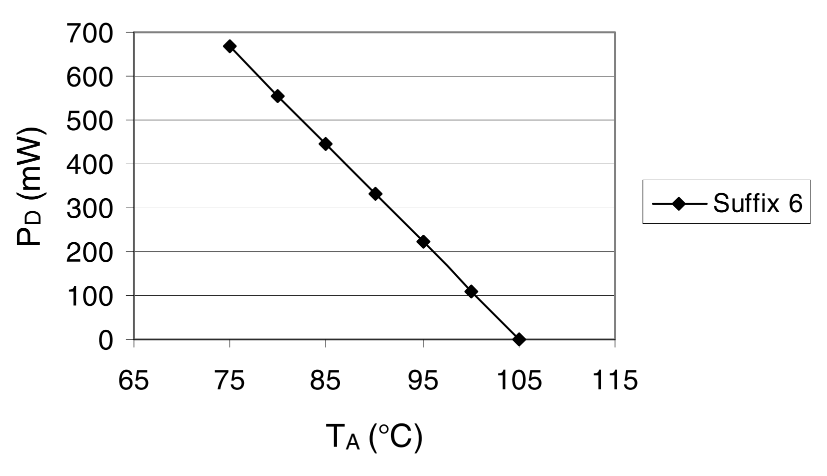
Using the values obtained in *Table 51* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the junction temperature range of the STM32F101xx (–40 < T_J < 105 °C).

Figure 39. LQFP64 P_D max vs. T_A



7 Ordering information scheme

Table 52. Ordering information scheme

Example: STM32 F 101 C 6 T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

101 = access line

Pin count

T = 36 pins
C = 48 pins
R = 64 pins
V = 100 pins

Flash memory size

6 = 32 Kbytes of Flash memory
8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory

Package

H = BGA
T = LQFP
U = VFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Options

xxx = programmed parts with 64 or 128 Kbytes of Flash memory
Axx = programmable parts with 32 Kbytes of Flash memory
TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

7.1 Future family enhancements

Further developments of the STM32F101xx Medium-density access line will see an expansion of the current options. Larger packages will soon be available with up to 512 KB Flash, 48 KB SRAM and with extended features such as flexible static memory controller (FSMC) support, DAC and additional timers and USARTS.

8 Revision history

Table 53. Document revision history

Date	Revision	Changes
06-Jun-2007	1	First draft.
20-Jul-07	2	I_{DD} values modified in *Table 11: Maximum current consumption in Run and Sleep modes (TA = 85 °C)*. V_{BAT} range modified in *Power supply schemes*. V_{REF+} min value, t_{STAB}, t_{lat} and f_{TRIG} added to *Table 42: ADC characteristics*. *Table 38: TIMx characteristics* modified. *Note 6* modified and *Note 8*, *Note 4* and *Note 7* added below *Table 4: Pin definitions*. *Figure 18: Low-speed external clock source AC timing diagram*, *Figure 10: Power supply scheme*, *Figure 22: Recommended NRST pin protection* and *Figure 23: I2C bus AC waveforms and measurement circuit(1)* modified. Sample size modified and machine model removed in *Electrostatic discharge (ESD)*. Number of parts modified and standard reference updated in *Static latch-up*. 25 °C and 85 °C conditions removed and class name modified in *Table 33: Electrical sensitivities*. $t_{SU(LSE)}$ changed to $t_{SU(LSE)}$ in *Table 22: HSE 4-16 MHz oscillator characteristics*. In *Table 29: Flash memory endurance and data retention*, typical endurance added, data retention for T_A = 25 °C removed and data retention for T_A = 85 °C added. Note removed below *Table 8: General operating conditions*. V_{BG} changed to V_{REFINT} in *Table 11: Embedded internal reference voltage*. I_{DD} max values added to *Table 11: Maximum current consumption in Run and Sleep modes (TA = 85 °C)*. $I_{DD(HSI)}$ max value added to *Table 24: HSI oscillator characteristics*. R_{PU} and R_{PD} min and max values added to *Table 34: I/O static characteristics*. R_{PU} min and max values added to *Table 37: NRST pin characteristics* (two notes removed). Datasheet title corrected. USB characteristics section removed. *Features on page 1* list optimized. Small text changes.

Table 53. Document revision history (continued)

Date	Revision	Changes
18-Oct-2007	3	$V_{ESD(CDM)}$ value added to *Table 32: ESD absolute maximum ratings*. Note added below *Table 10: Embedded reset and power control block characteristics*. and below *Table 22: HSE 4-16 MHz oscillator characteristics*. Note added below *Table 35: Output voltage characteristics* and V_{OH} parameter description modified. *Table 42: ADC characteristics* and *Table 44: ADC accuracy - limited test conditions* modified. *Figure 27: ADC accuracy characteristics* modified. Packages are ECOPACK® compliant. Tables modified in *Section 5.3.5: Supply current characteristics*. ADC and ANTI_TAMPER signal names modified (see *Table 4: Pin definitions*). *Table 4: Pin definitions* modified. Note 4 removed and values updated in *Table 18: Typical current consumption in Standby mode*. V_{hys} modified in *Table 34: I/O static characteristics*. Updated: *Table 30: EMS characteristics* and *Table 31: EMI characteristics*. t_{VDD} modified in *Table 9: Operating conditions at power-up / power-down*. Typical values modified, note 2 modified and note 3 removed in *Table 26: Low-power mode wakeup timings*. Maximum current consumption *Table 12*, *Table 13* and *Table 14* updated. Values added and notes added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. *On-chip peripheral current consumption on page 38* added. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see *Section 6: Package characteristics*). V_{prog} added to *Table 28: Flash memory characteristics*. T_{S_temp} added to *Table 46: TS characteristics*. $T_{S\_vrefint}$ added to *Table 11: Embedded internal reference voltage*. Handling of unused pins specified in *General input/output characteristics on page 48*. All I/Os are CMOS and TTL compliant. *Table 4: Pin definitions*: table clarified and *Note 7* modified. Internal LSI RC frequency changed from 32 to 40 kHz (see *Table 25: LSI oscillator characteristics*). Values added to *Table 26: Low-power mode wakeup timings*. N_{END} modified in *Table 29: Flash memory endurance and data retention*. Option byte addresses corrected in *Figure 7: Memory map*. ACC_{HSI} modified in *Table 24: HSI oscillator characteristics*. t_{JITTER} removed from *Table 27: PLL characteristics*. *Appendix A: Important notes on page 71* added. Added: *Figure 12*, *Figure 13*, *Figure 14* and *Figure 16*.

Table 53. Document revision history (continued)

Date	Revision	Changes
22-Nov-2007	4	Document status promoted from preliminary data to datasheet. Small text changes. STM32F101CB part number corrected in *Table 1: Device summary*. Number of communication peripherals corrected for STM32F101Tx in *Table 2: Device features and peripheral counts (STM32F101xx High-density access line)* and Number of GPIOs corrected for LQFP package. *Power supply schemes on page 11* modified. Main function and default alternate function modified for PC14 and PC15 in *Table 4: Pin definitions*, *Note 5* added, Remap column added. *Figure 10: Power supply scheme* modified. V_{DD} –V_{SS} ratings modified and *Note 1* modified in *Table 5: Voltage characteristics*. *Note 1* modified in *Table 6: Current characteristics*. *Note 2* added in *Table 10: Embedded reset and power control block characteristics*. 48 and 72 MHz frequencies removed from *Table 12*, *Table 13* and *Table 14*. MCU ‘s operating conditions modified in *Typical current consumption on page 36*. I_{DD_VBAT} typical value at 2.4 V modified and I_{DD_VBAT} maximum value added in *Table 15: Typical and maximum current consumptions in Stop and Standby modes*. Note added in *Table 16 on page 36* and *Table 17 on page 37*. *Table 19: Peripheral current consumption* modified. *Figure 15: Current consumption in Stop mode with regulator in Low-power mode versus temperature at VDD = 3.3 V and 3.6 V* added. Note removed below *Figure 24: SPI timing diagram - slave mode and CPHA=0*. Note added below *Figure 25: SPI timing diagram - slave mode and CPHA=1(1)*. *Figure 28: Typical connection diagram using the ADC* modified. $t_{SU(HSE)}$ and $t_{SU(LSE)}$ conditions modified in *Table 22* and *Table 23*, respectively. Maximum values removed from *Table 26: Low-power mode wakeup timings*. t_{RET} conditions modified in *Table 29: Flash memory endurance and data retention*. Conditions modified in *Table 30: EMS characteristics*. Impedance size specified in *A.4: Voltage glitch on ADC input 0 on page 71*. Small text changes in *Table 35: Output voltage characteristics*. *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)* updated. Details on unused pins removed from *General input/output characteristics on page 48*. *Table 41: SPI characteristics* updated. Notes added and I_{lkg} removed in *Table 42: ADC characteristics*. Note added in *Table 43* and *Table 46*. *Note 2* and *Note 3* added below *Table 44: ADC accuracy - limited test conditions*. Avg_Slope and V_{25} modified in *Table 46: TS characteristics*. Θ_{JA}value for VFQFPN36 package added in *Table 51: Thermal characteristics*. *I2C interface characteristics on page 52* modified. Order codes replaced by *Section 7: Ordering information scheme*.

Table 53. Document revision history (continued)

Date	Revision	Changes
14-Mar-2008	5	*Figure 2: Clock tree on page 16* added. CRC added (see *CRC (cyclic redundancy check) calculation unit on page 9* and *Figure 7: Memory map on page 24* for address). Maximum T_J value given in *Table 7: Thermal characteristics on page 29*. P_D, T_A and T_J added, t_{prog} values modified and t_{prog} description clarified in *Table 28: Flash memory characteristics on page 45*. I_{DD} modified in *Table 15: Typical and maximum current consumptions in Stop and Standby modes on page 34*. ACC_{HSI} modified in *Table 24: HSI oscillator characteristics on page 43*, note 2 removed. t_{RET} modified in *Table 29: Flash memory endurance and data retention*. $V_{NF(NRST)}$ unit corrected in *Table 37: NRST pin characteristics on page 51*. *Table 41: SPI characteristics on page 55* modified. I_{VREF} added in *Table 42: ADC characteristics on page 58*. *Table 44: ADC accuracy - limited test conditions* added. *Table 45: ADC accuracy* modified. LQFP100 package specifications updated (see *Section 6: Package characteristics on page 63*). Recommended LQFP100, LQFP64, LQFP48 and VFQFPN36 footprints added (see *Figure 34*, *Figure 36*, *Figure 38* and *Figure 32*). *Section 6.2: Thermal characteristics on page 68* modified. *Appendix A: Important notes* removed.
21-Mar-2008	6	Small text changes. In *Table 29: Flash memory endurance and data retention*: – N_{END} tested over the whole temperature range – cycling conditions specified for t_{RET} – t_{RET} min modified at $T_A = 55$ °C *Figure 2: Clock tree* corrected. *Figure 7: Memory map* clarified. V_{25}, Avg_Slope and T_L modified in *Table 46: TS characteristics*. CRC feature removed.
22-May-2008	7	*Section 1: Introduction* modified, *Section 2.2: Full compatibility throughout the family* added. CRC feature added. I_{DD_VBAT} removed from *Table 18: Typical current consumption in Standby mode on page 37*. Values added to *Table 40: SCL frequency (fPCLK1= 36 MHz, VDD = 3.3 V) on page 54*. *Figure 24: SPI timing diagram - slave mode and CPHA=0 on page 56* modified. *Equation 1* corrected. *Section 6.2.2: Evaluating the maximum junction temperature for an application on page 69* added. Axx option added to *Table 52: Ordering information scheme on page 70*.

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