## SN65C3232, SN75C3232 3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

SLLS540B - JULY 2002 - REVISED NOVEMBER 2004

- Operate With 3-V to 5.5-V V<sub>CC</sub> Supply
- Operate Up To 1 Mbit/s
- Low Supply Current . . . 300 μA Typ
- External Capacitors . . .  $4 \times 0.1 \mu F$
- Accept 5-V Logic Input With 3.3-V Supply
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)
- Applications
  - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment

#### D, DB, DW, OR PW PACKAGE (TOP VIEW) 16 V<sub>CC</sub> С1+ Г ∨+ Π 2 15 GND C1− ∏ 3 14∏ DOUT1 C2+ [] 4 13 RIN1 C2- [] 5 12 ROUT1 11 DIN1 V- [] 6 DOUT2 17 10 ☐ DIN2 RIN2 🛮 8 9 ROUT2

### description/ordering information

The SN65C3232 and SN75C3232 consist of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). These devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ $\mu$ s to 150 V/ $\mu$ s.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	2010 D	Tube of 40	SN65C3232D	0500000
	SOIC – D	Reel of 2500	SN65C3232DR	65C3232
	2010 DW	Tube of 40	SN65C3232DW	050000
–40°C to 85°C	SOIC – DW	Reel of 2000	SN65C3232DWR	65C3232
	SSOP – DB	Reel of 2000	SN65C3232DBR	65C3232
	TOOOD DW	Tube of 90	SN65C3232PW	00000
	TSSOP – PW	Reel of 2000	SN65C3232PWR	CB3232
	2010 D	Tube of 40	SN75C3232D	7500000
	SOIC – D	Reel of 2500	SN75C3232DR	75C3232
	2010 DW	Tube of 40	SN75C3232DW	7500000
0°C to 70°C	SOIC – DW	Reel of 2000	SN75C3232DWR	75C3232
	SSOP – DB	Reel of 2000	SN75C3232DBR	75C3232
	TCCOD DW	Tube of 90	SN75C3232PW	CA2020
	TSSOP – PW	Reel of 2000	SN75C3232PWR	CA3232

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **Function Tables**

### **EACH DRIVER**

INPUT DIN	OUTPUT DOUT
L	Н
Н	L

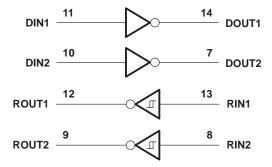
H = high level, L = low level

#### **EACH RECEIVER**

INPUT RIN	OUTPUT ROUT				
L	Н				
Н	L				
Open	Н				

H = high level, L = low level, Open = input disconnected or connected driver off

## logic diagram (positive logic)



## SN65C3232, SN75C3232 3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4 and Figure 4)

				MIN	NOM	MAX	UNIT
	Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	.,
			V <sub>CC</sub> = 5 V	4.5	5	5.5	V
	Driver high-level input voltage	DIN	V <sub>CC</sub> = 3.3 V	2			V
VIH		DIN	V <sub>CC</sub> = 5 V	2.4			
VIL	Driver low-level input voltage		DIN			0.8	V
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Driver input voltage		DIN	0		5.5	.,
VI Receiver input voltage			-25		25	V	
т.	Operating free-air temperature		SN65C3232	-40		85	00
TA			SN75C3232	0		70	°C

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at V $_{CC}$  = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V $_{CC}$  = 5 V  $\pm$  0.5 V.

# electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
ICC	Supply current	No load,	V <sub>CC</sub> = 3.3 V or 5 V		0.3	1	mA

<sup>‡</sup> All typical values are at  $V_{CC}$  = 3.3 V or  $V_{CC}$  = 5 V, and  $T_A$  = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V.



<sup>2.</sup> Maximum power dissipation is a function of T<sub>J</sub>(max), θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J</sub>(max) – T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

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#### **DRIVER SECTION**

# electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS			TYP	MAX	UNIT
Vон	High-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	DIN = GND	5	5.4		V
VOL	Low-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	$DIN = V_{CC}$	-5	-5.4		V
lіН	High-level input current	VI = VCC			±0.01	±1	μΑ
Ι <sub>Ι</sub> L	Low-level input current	V <sub>I</sub> at GND			±0.01	±1	μΑ
la at	Chart singuit autout aurona	V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0 V		±35	±60	A
los‡	Short-circuit output current	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0 V		±35	±90	mA
r <sub>O</sub>	Output resistance	$V_{CC}$ , V+, and V- = 0 V,	V <sub>O</sub> = ±2 V	300	10M		Ω

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V or  $V_{CC}$  = 5 V, and  $T_A$  = 25°C.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS			MIN	TYP <sup>†</sup>	MAX	UNIT
			C <sub>L</sub> = 1000 pF		250			
Maximum data rate (see Figure 1)		$R_L = 3 k\Omega$ , One DOUT switching	C <sub>L</sub> = 250 pF,	V <sub>CC</sub> = 3 V to 4.5 V	1000			kbit/s
	(occ rigare r)	One Boot switching	C <sub>L</sub> = 1000 pF,	1000				
t <sub>sk(p)</sub>	Pulse skew§	C <sub>L</sub> = 150 pF to 2500 pF	$R_L$ = 3 kΩ to 7 kΩ, See Figure 2			300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	$R_L$ = 3 kΩ to 7 kΩ, V <sub>CC</sub> = 3.3 V	C <sub>L</sub> = 150 pF to 1000	pF	18		150	V/μs

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^{\circ}\text{C}$ .

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V.



<sup>\$</sup> Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

<sup>§</sup> Pulse skew is defined as |tplh - tphl| of each channel of the same device.

#### RECEIVER SECTION

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT
Vон	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> – 0.6 V	V <sub>CC</sub> – 0.1 V		V
VOL	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
.,	Desiring a sign is not the selection of	V <sub>CC</sub> = 3.3 V		1.5	2.4	
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 5 V		1.8	2.4	V
.,	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.2		.,
V <sub>IT</sub> _		V <sub>CC</sub> = 5 V	0.8	1.5		V
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.3	·	V
rį	Input resistance	$V_I = \pm 3 \text{ V to } \pm 25 \text{ V}$	3	5	7	kΩ

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^{\circ}\text{C}$ .

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V.

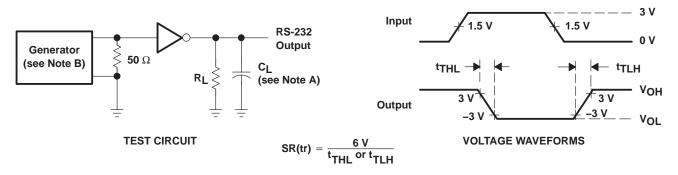
## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 3)

	PARAMETER	TEST CONDITIONS	MIN TYP <sup>†</sup> MAX	UNIT
<sup>t</sup> PLH	Propagation delay time, low- to high-level output	0. 450 = 5	300	ns
tPHL	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF	300	ns
tsk(p)	Pulse skew <sup>‡</sup>		300	ns

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V or  $V_{CC}$  = 5 V, and  $T_A$  = 25°C.

NOTE 4: Test conditions are C1-C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2-C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V.

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

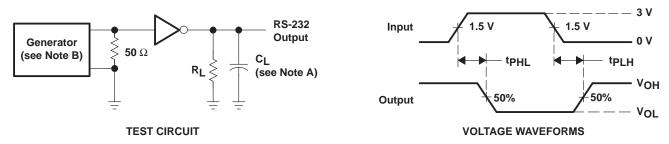
B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50~\Omega$ , 50% duty cycle,  $t_\Gamma \le 10$  ns.  $t_f \le 10$  ns.

Figure 1. Driver Slew Rate



<sup>‡</sup> Pulse skew is defined as |tpLH - tpHL| of each channel of the same device.

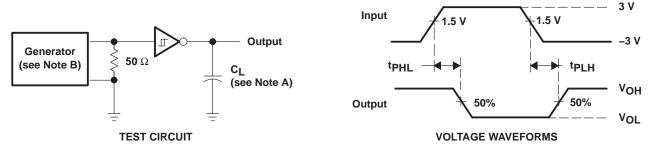
#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_\Gamma \le 10$  ns.  $t_f \le 10$  ns.

Figure 2. Driver Pulse Skew

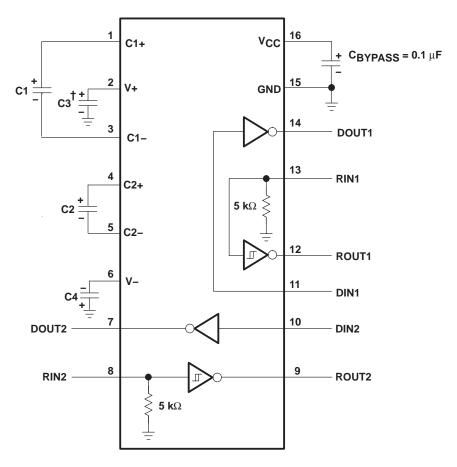


NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50~\Omega$ , 50% duty cycle,  $t_\Gamma \le 10~\text{ns}$ .

Figure 3. Receiver Propagation Delay Times

## **APPLICATION INFORMATION**



 $^\dagger$  C3 can be connected to V<sub>CC</sub> or GND.

## V<sub>CC</sub> vs CAPACITOR VALUES

VCC	C1	C2, C3, C4		
3.3 V ± 0.3 V	0.1 μF	0.1 μF		
5 V ± 0.5 V	0.047 μF	0.33 μF		
3 V to 5.5 V	0.1 μF	0.47 μF		

Figure 4. Typical Operating Circuit and Capacitor Values



## **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65C3232D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3232PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM





.com 28-May-2007

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75C3232DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3232PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)



### PACKAGE OPTION ADDENDUM

28-May-2007

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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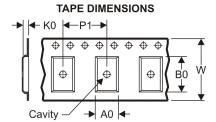




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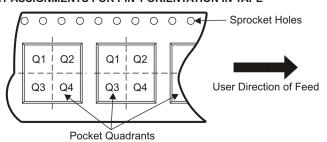
### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

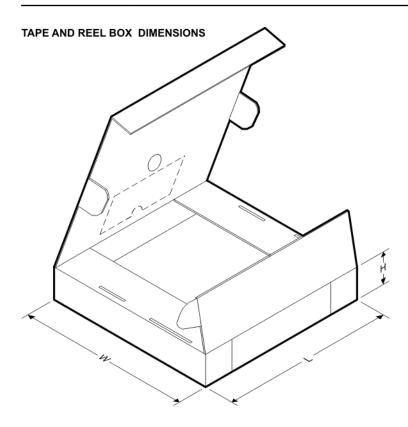
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

All differsions are nonlinal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3232DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN65C3232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65C3232DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65C3232PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN75C3232DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75C3232DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75C3232DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN75C3232PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1





\*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3232DBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN65C3232DR	SOIC	D	16	2500	333.2	345.9	28.6
SN65C3232DWR	SOIC	DW	16	2000	346.0	346.0	33.0
SN65C3232PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN75C3232DBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN75C3232DR	SOIC	D	16	2500	333.2	345.9	28.6
SN75C3232DWR	SOIC	DW	16	2000	346.0	346.0	33.0
SN75C3232PWR	TSSOP	PW	16	2000	346.0	346.0	29.0

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

#### 14 PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

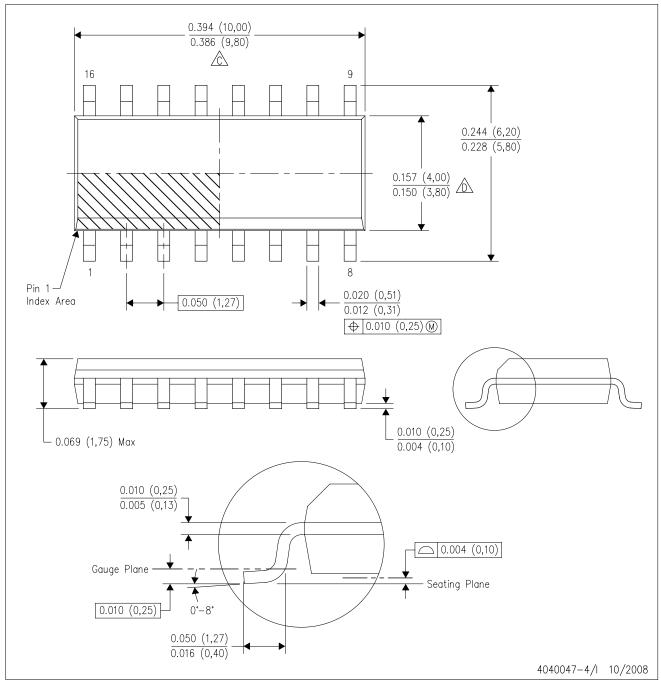
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE

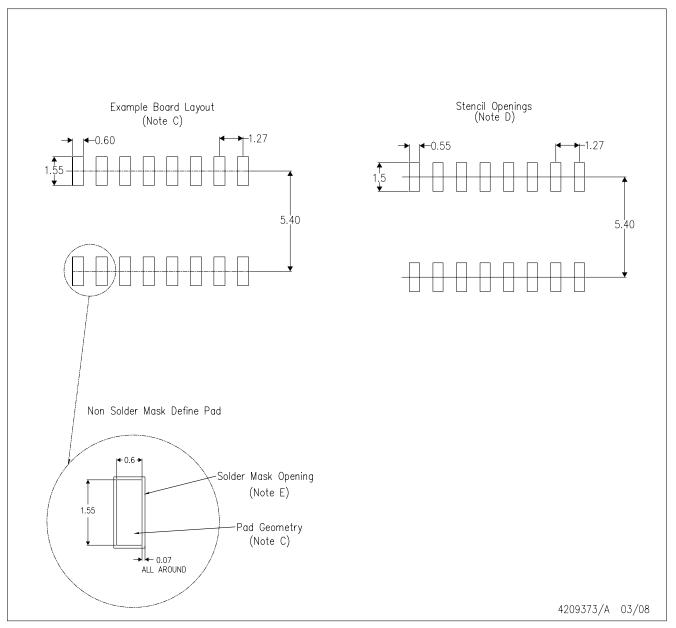


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



## D(R-PDSO-G16)



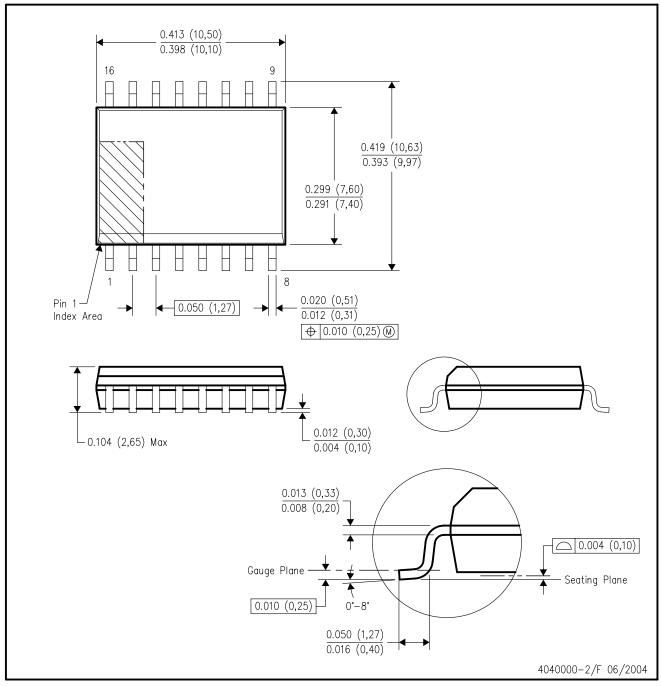
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## DW (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



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