SBOS365C − JUNE 2006 − REVISED APRIL 2007

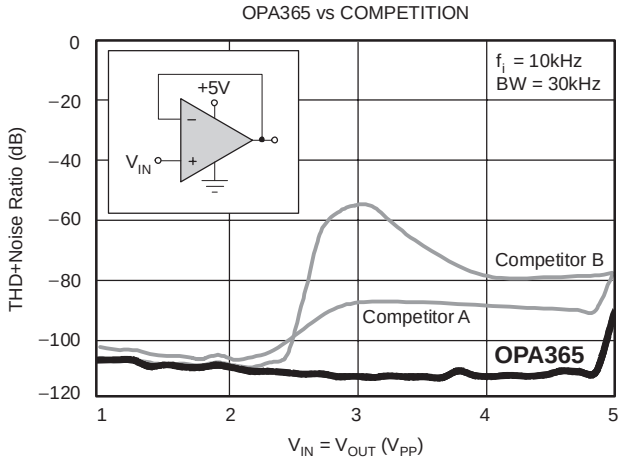
2.2V, 50MHz, Low-Noise, Single-Supply Rail-to-Rail OPERATIONAL AMPLIFIERS

FEATURES

- **RAIL-TO-RAIL INPUT *WITHOUT CROSSOVER***
- **2.2V OPERATION**
- **LOW OFFSET: 200μV**
- **WIDE BANDWIDTH: 50MHz**
- **CMRR: 100dB (min)**
- **HIGH SLEW RATE: 25V/μs**
- **LOW NOISE: 4.5nV/√Hz**
- **LOW THD+NOISE: 0.0006%**
- **QUIESCENT CURRENT: 5mA (max)**
- ***micro*PACKAGE: SOT23-5**

APPLICATIONS

- **SIGNAL CONDITIONING**
- **DATA ACQUISITION**
- **PROCESS CONTROL**
- **ACTIVE FILTERS**
- **TEST EQUIPMENT**
- **AUDIO**
- **WIDEBAND AMPLIFIERS**



DESCRIPTION

The OPAx365 zer∅-crossover series rail-to-rail high-performance CMOS operational amplifiers are optimized for very low voltage, single-supply applications. Rail-to-rail input/output, low-noise (4.5nV/√Hz) and high-speed operations (50MHz Gain Bandwidth) make them ideal for driving sampling analog-to-digital converters (ADCs). Applications incude audio, signal conditioning, and sensor amplification. The OPA365 family of op amps are well-suited for cell phone power amplifier control loops.

Special features include excellent common-mode rejection ratio (CMRR), no input stage crossover distortion, high input impedance and rail-to-rail input and output swing. The input common-mode range includes both the negative and positive supplies. The output voltage swing is within 10mV of the rails.

The OPA365 (single version) is available in the *micro*-SIZE SOT23-5 and SO-8 packages. The OPA2365 (dual version) is offered in the SO-8 package. All versions are specified for operation from −40°C to +125°C. Single and dual versions have identical specifications for maximum design flexibility.

PACKAGE	OPA365	OPA2365
SOT23-5	✓	
SO-8	✓	✓

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+5.5V
Signal Input Terminals, Voltage(2)	(V−) −0.5V to (V+) + 0.5V
Signal Input Terminals, Current(2)	±10mA
Output Short-Circuit(3)	Continuous
Operating Temperature	−40°C to +150°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
ESD Rating	
Human Body Model	4000V
Charged Device Model	1000V
Machine Model	400V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Short-circuit to ground, one amplifier per package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

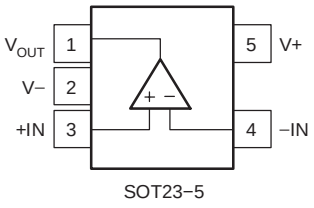
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA365	SOT23-5	DBV	OAVQ
	SO-8	D	O365A
OPA2365	SO-8	D	O2365A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS

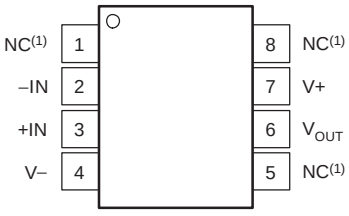
Top View

OPA365



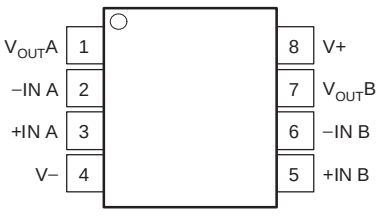
SOT23−5

OPA365



SO−8

OPA2365



SO−8

(1) NC denotes no internal connection.

ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = −40°C to +125°C.**

At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

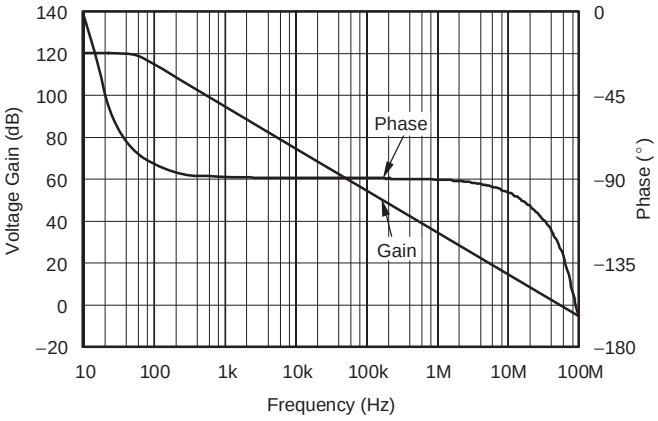
PARAMETER		TEST CONDITIONS	OPAx365 MIN	OPAx365 TYP	OPAx365 MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}			100	200	µV
Drift	**dV_{OS}/dT**			**1**		**µV/°C**
vs Power Supply	**PSRR**	**V_S = +2.2V to +5.5V**		**10**	**100**	**µV/V**
Channel Separation, dc				0.2		µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.2	±10	pA
over Temperature				See Typical Characteristics		
Input Offset Current	I_{OS}			±0.2	±10	pA
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz	e_n			5		μV_{PP}
Input Voltage Noise Density, f = 100kHz	e_n			4.5		$nV/\sqrt{Hz}$
Input Current Noise Density, f = 10kHz	i_n			4		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	**CMRR**	**(V−) − 0.1V ≤ V_{CM} ≤ (V+) + 0.1V**	**100**	**120**		**dB**
INPUT CAPACITANCE						
Differential				6		pF
Common-Mode				2		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**R_L = 10kΩ, 100mV < V_O < (V+) − 100mV**	**100**	**120**		**dB**
		R_L = 600Ω, 200mV < V_O < (V+) − 200mV	100	120		dB
		R_L = 600Ω, 200mV < V_O < (V+) − 200mV	**94**			**dB**
FREQUENCY RESPONSE		V_S = 5V				
Gain-Bandwidth Product	GBW			50		MHz
Slew Rate	SR	G = +1		25		V/µs
Settling Time, 0.1%	t_S	4V Step, G = +1		200		ns
0.01%		4V Step, G = +1		300		ns
Overload Recovery Time		V_{IN} x Gain > V_S		< 0.1		µs
Total Harmonic Distortion + Noise(1)	THD+N	R_L = 600Ω, V_O = $4V_{PP}$, G = +1, f = 1kHz		0.0004		%
OUTPUT						
Voltage Output Swing from Rail						
over Temperature		**R_L = 10kΩ, V_S = 5.5V**		**10**	**20**	**mV**
Short-Circuit Current	I_{SC}			±65		mA
Capacitive Load Drive	C_L			See Typical Characteristics		
Open-Loop Output Impedance		f = 1MHz, I_O = 0		30		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.2		5.5	V
Quiescent Current Per Amplifier	I_Q	I_O = 0		4.6	5	mA
over Temperature					**5**	**mA**
TEMPERATURE RANGE						
Specified Range			−40		+125	°C
Thermal Resistance	θ_{JA}					°C/W
SOT23-5				200		°C/W
SO-8				150		°C/W

(1) 3rd-order filter; bandwidth 80kHz at −3dB.

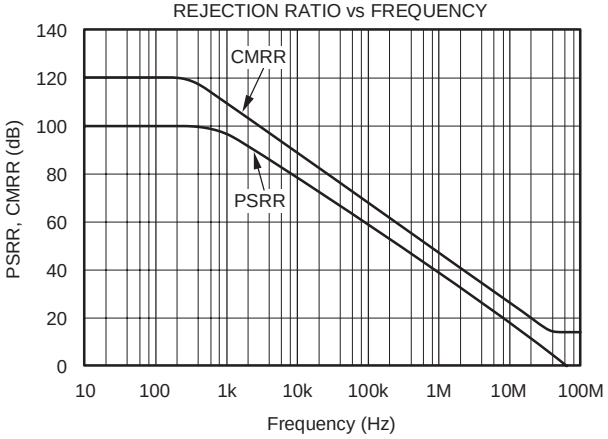
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, and C_L = 0pF, unless otherwise noted.

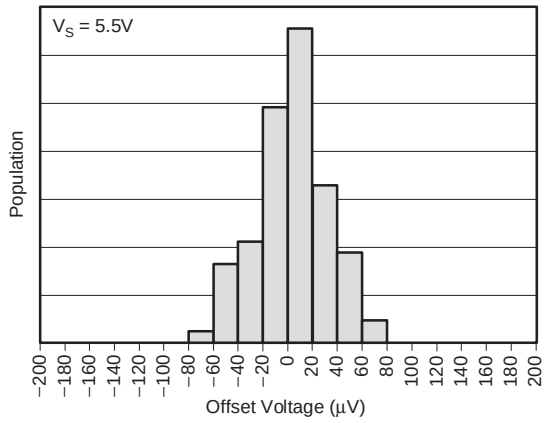
OPEN−LOOP GAIN/PHASE vs FREQUENCY



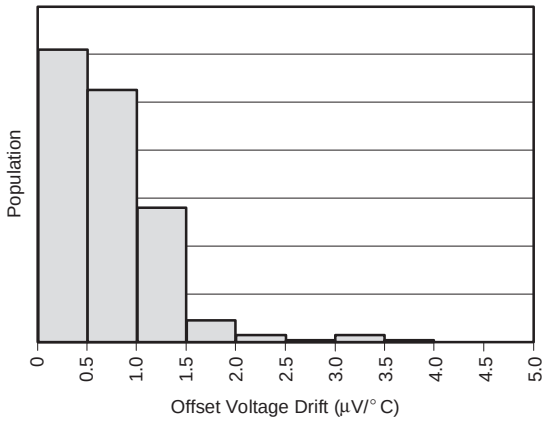
POWER SUPPLY AND COMMON−MODE REJECTION RATIO vs FREQUENCY



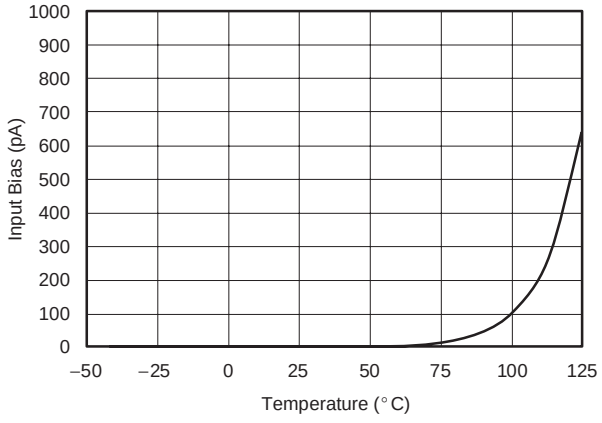
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



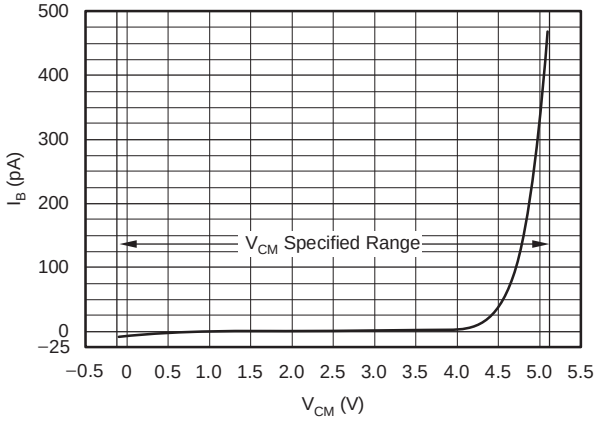
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



INPUT BIAS CURRENT vs TEMPERATURE



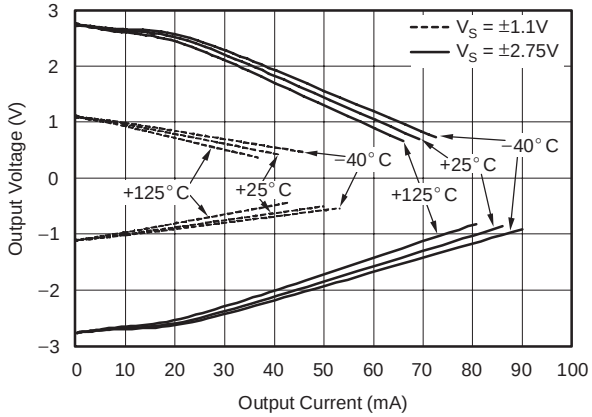
INPUT BIAS CURRENT vs COMMON−MODE VOLTAGE



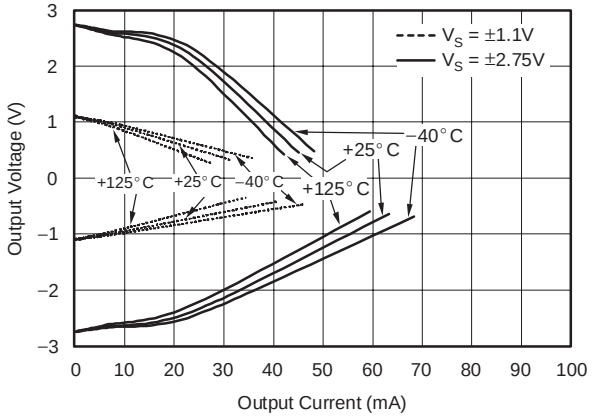
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, and C_L = 0pF, unless otherwise noted.

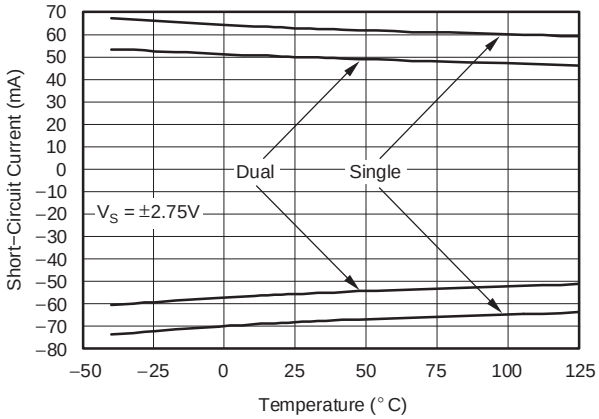
OPA365 OUTPUT VOLTAGE
vs OUTPUT CURRENT



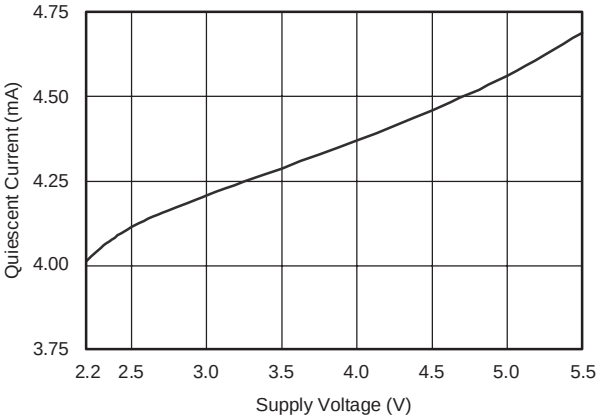
OPA2365 OUTPUT VOLTAGE SWING
vs OUTPUT CURRENT



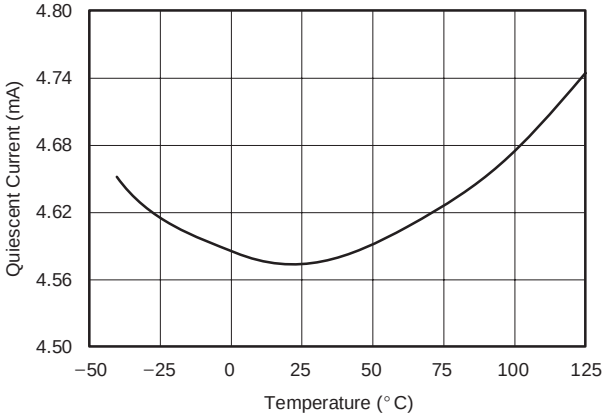
SHORT−CIRCUIT CURRENT vs TEMPERATURE



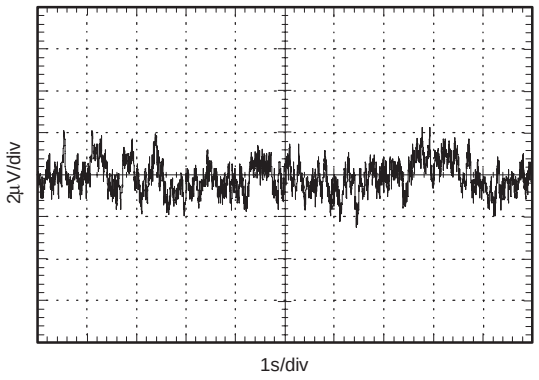
QUIESCENT CURRENT vs SUPPLY VOLTAGE



QUIESCENT CURRENT vs TEMPERATURE



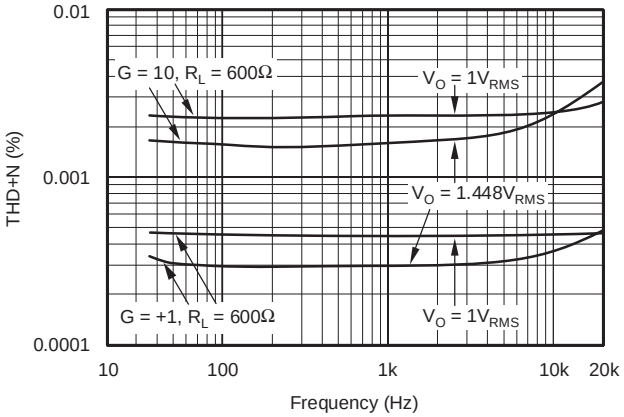
0.1Hz to 10Hz
INPUT VOLTAGE NOISE



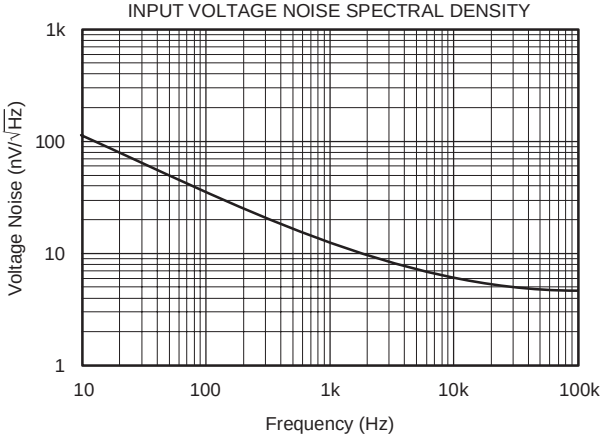
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, and C_L = 0pF, unless otherwise noted.

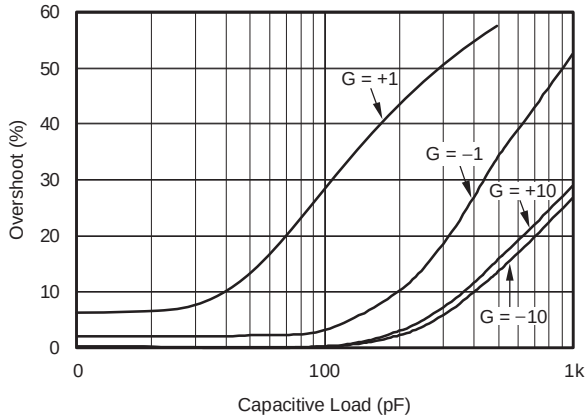
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



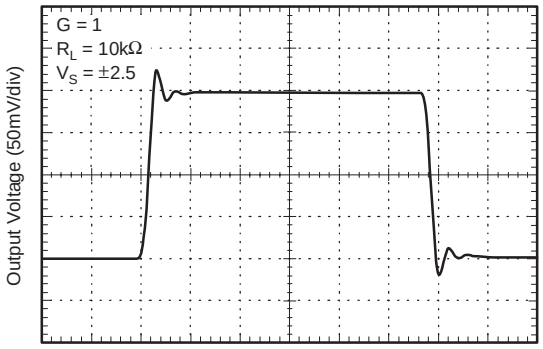
INPUT VOLTAGE NOISE SPECTRAL DENSITY



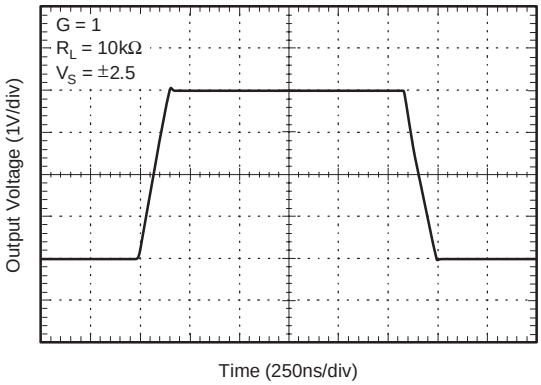
OVERSHOOT vs CAPACITIVE LOAD



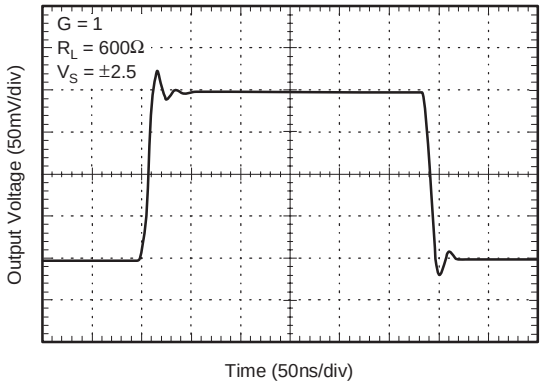
SMALL−SIGNAL STEP RESPONSE



LARGE−SIGNAL STEP RESPONSE



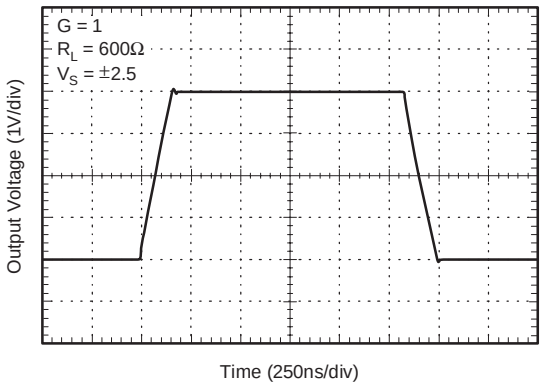
SMALL−SIGNAL STEP RESPONSE



TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, and C_L = 0pF, unless otherwise noted.

LARGE−SIGNAL STEP RESPONSE



APPLICATIONS INFORMATION

OPERATING CHARACTERISTICS

The OPA365 amplifier parameters are fully specified from +2.2V to +5.5V. Many of the specifications apply from −40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

GENERAL LAYOUT GUIDELINES

The OPA365 is a wideband amplifier. To realize the full operational performance of the device, good high-frequency printed circuit board (PCB) layout practices are required. Low-loss, 0.1µF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

BASIC AMPLIFIER CONFIGURATIONS

As with other single-supply op amps, the OPA365 may be operated with either a single supply or dual supplies. A typical dual-supply connection is shown in Figure 1, which is accompanied by a single-supply connection. The OPA365 is configured as a basic inverting amplifier with a gain of −10V/V. The dual-supply connection has an output voltage centered on zero, while the single−supply connection has an output centered on the common-mode voltage V_{CM}. For the circuit shown, this voltage is 1.5V, but may be any value within the common-mode input voltage range. The OPA365 V_{CM} range extends 100mV beyond the power-supply rails.

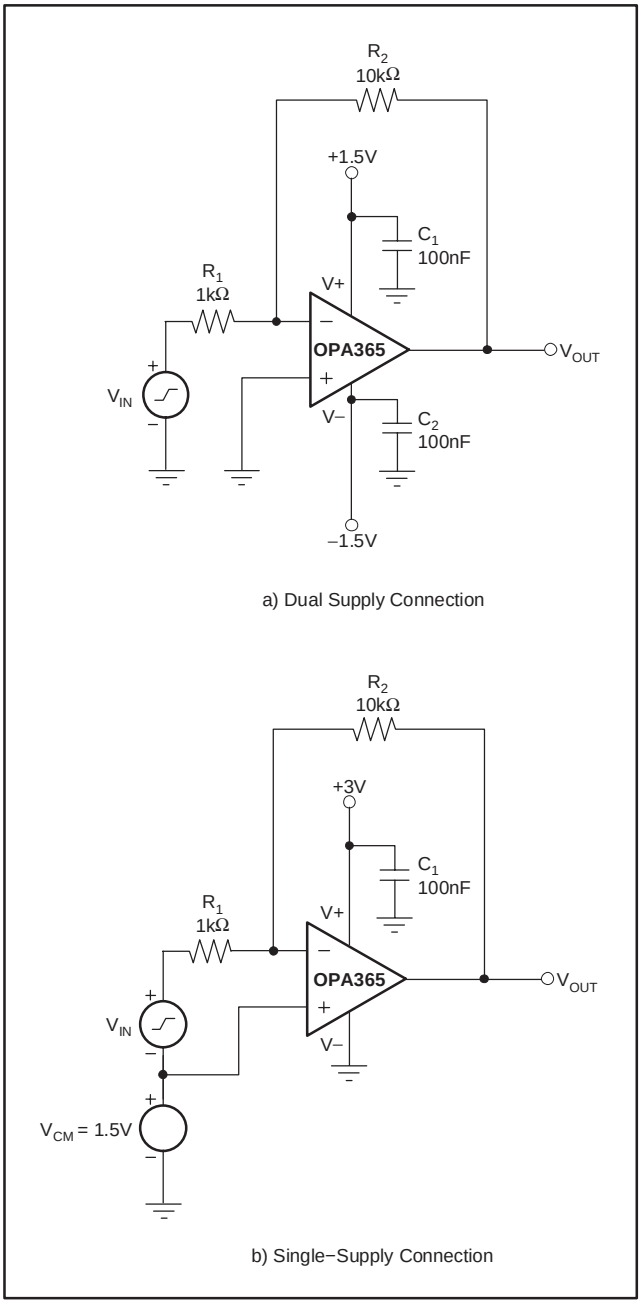


Figure 1. Basic Circuit Connections

Figure 2 shows a single-supply, electret microphone application where V_{CM} is provided by a resistive divider. The divider also provides the bias voltage for the electret element.

INPUT AND ESD PROTECTION

The OPA365 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, provided that the current is limited to 10mA as stated in the Absolute Maximum Ratings. Figure 3 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to the minimum in noise-sensitive applications.

RAIL−TO−RAIL INPUT

The OPA365 product family features true rail-to-rail input operation, with supply voltages as low as ±1.1V (2.2V). A unique zer∅-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary stage operational amplifiers. This topology also allows the OPA365 to provide superior common−mode performance over the entire input range, which extends 100mV beyond both power-supply rails; see Figure 4. When driving ADCs, the highly linear VCM range of the OPA365 assures that the op amp/ADC system linearity performance is not compromised.

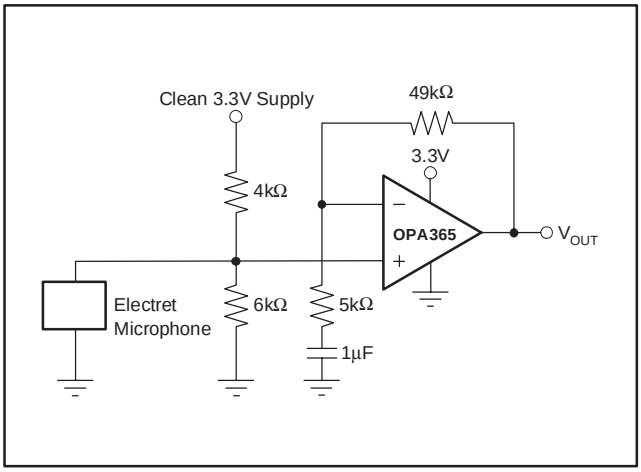


Figure 2. Microphone Preamplifier

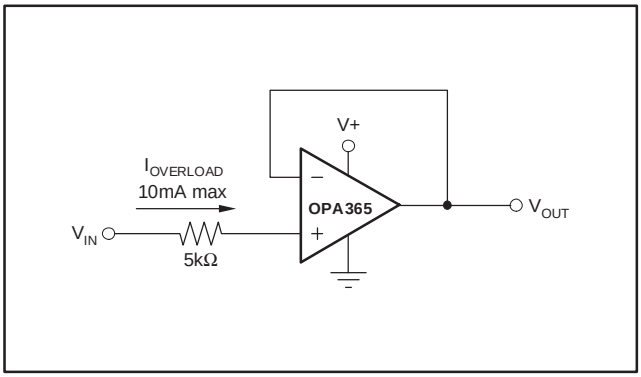


Figure 3. Input Current Protection

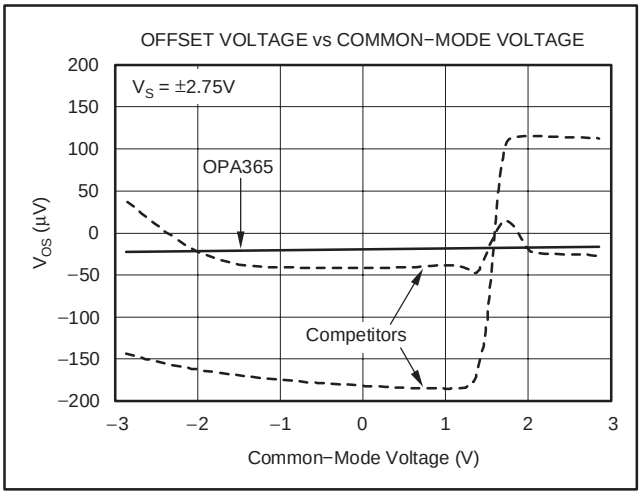


Figure 4. OPA365 has Linear Offset Over the Entire Common-Mode Range

A simplified schematic illustrating the rail-to-rail input circuitry is shown in Figure 5.

CAPACITIVE LOADS

The OPA365 may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA365 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (+1V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

When operating in the unity-gain configuration, the OPA365 remains stable with a pure capacitive load up to approximately 1nF. The equivalent series resistance (ESR) of some very large capacitors (C_L > 1µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the typical characteristic graph, *Small-Signal Overshoot vs. Capacitive Load*.

One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor, typically 10Ω to 20Ω, in series with the output; see Figure 6. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider may be insignificant. For instance, with a load resistance, R_L = 10kΩ, and R_S = 20Ω, the gain error is only about 0.2%. However, when R_L is decreased to 600Ω, which the OPA365 is able to drive, the error increases to 7.5%.

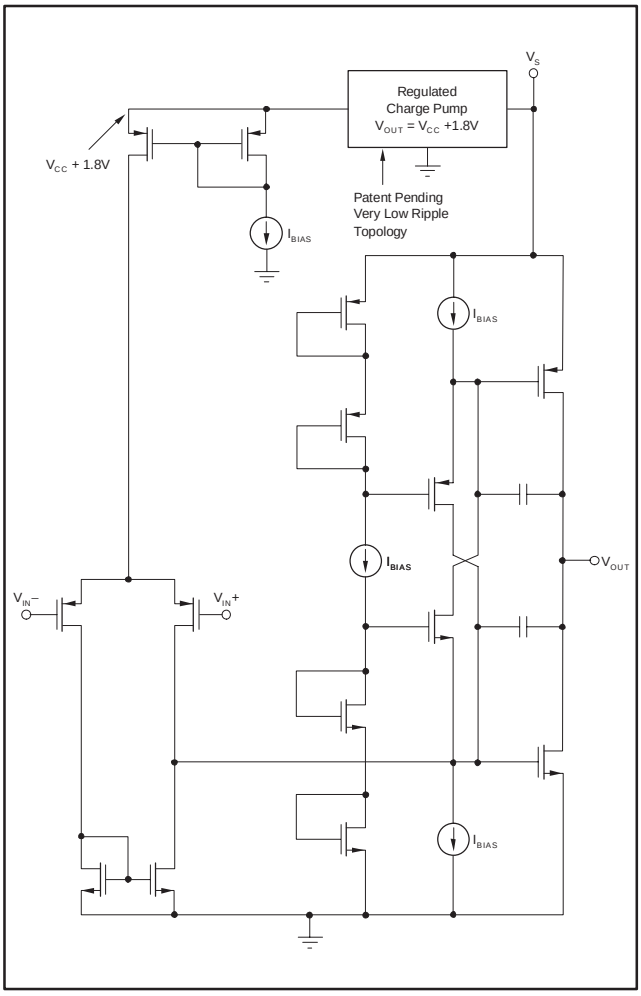


Figure 5. Simplified Schematic

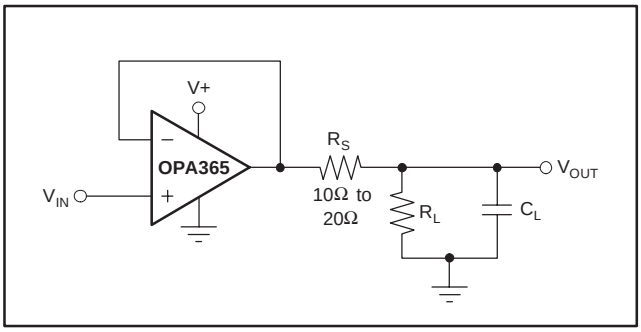


Figure 6. Improving Capacitive Load Drive

ACHIEVING AN OUTPUT LEVEL OF ZERO VOLTS (0V)

Certain single-supply applications require the op amp output to swing from 0V to a positive full-scale voltage and have high accuracy. An example is an op amp employed to drive a single-supply ADC having an input range from 0V to +5V. Rail-to-rail output amplifiers with very light output loading may achieve an output level within millivolts of 0V (or $+V_S$ at the high end), but not 0V. Furthermore, the deviation from 0V only becomes greater as the load current required increases. This increased deviation is a result of limitations of the CMOS output stage.

When a pull-down resistor is connected from the amplifier output to a negative voltage source, the OPA365 can achieve an output level of 0V, and even a few millivolts below 0V. Below this limit, nonlinearity and limiting conditions become evident. Figure 7 illustrates a circuit using this technique.

A pull-down current of approximately 500µA is required when OPA365 is connected as a unity-gain buffer. A practical termination voltage (V_{NEG}) is −5V, but other convenient negative voltages also may be used. The pull-down resistor R_L is calculated from $R_L = [(V_O - V_{NEG})/(500\mu A)]$. Using a minimum output voltage (V_O) of 0V, $R_L = [0V-(-5V)]/(500\mu A)] = 10k\Omega$. Keep in mind that lower termination voltages result in smaller pull-down resistors that load the output during positive output voltage excursions.

Note that this technique does not work with all op amps and should only be applied to op amps such as the OPA365 that have been specifically designed to operate in this manner. Also, operating the OPA365 output at 0V changes the output stage operating conditions, resulting in somewhat lower open-loop gain and bandwidth. Keep these precautions in mind when driving a capacitive load because these conditions can affect circuit transient response and stability.

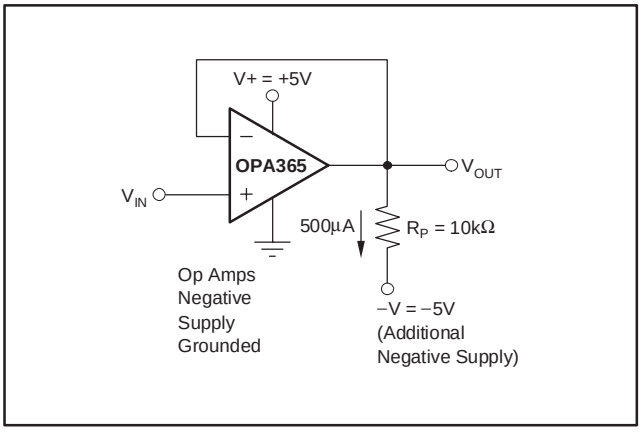


Figure 7. Swing-to-Ground

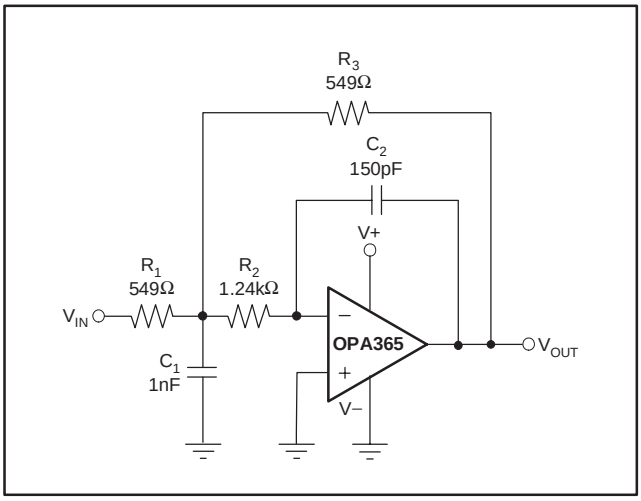


Figure 8. Second-Order Butterworth 500kHz Low-Pass Filter

ACTIVE FILTERING

The OPA365 is well-suited for active filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 8 shows a 500kHz, 2nd-order, low-pass filter utilizing the multiple−feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is −40dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics such as the anti-aliasing filter used ahead of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options: 1) adding an inverting amplifier; 2) adding an additional 2nd-order MFB stage; or 3) using a noninverting filter topology such as the Sallen-Key (shown in Figure 9).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro program. This software is available as a free download at www.ti.com.

DRIVING AN ANALOG-TO-DIGITAL CONVERTER

Very wide common-mode input range, rail-to-rail input and output voltage capability and high speed make the OPA365 an ideal driver for modern ADCs. Also, because it is free of the input offset transition characteristics inherent to some rail-to-rail CMOS op amps, the OPA365 provides low THD and excellent linearity throughout the input voltage swing range.

Figure 10 shows the OPA365 driving an ADS8326, 16-bit, 250kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer and has an output swing to 0V, making it directly compatible with the ADC minus full-scale input level. The 0V level is achieved by powering the OPA365 V− pin with a small negative voltage established by the diode forward voltage drop. A small, signal-switching diode or Schottky diode provides a suitable negative supply voltage of −0.3 to −0.7V. The supply rail-to-rail is equal to V+, plus the small negative voltage.

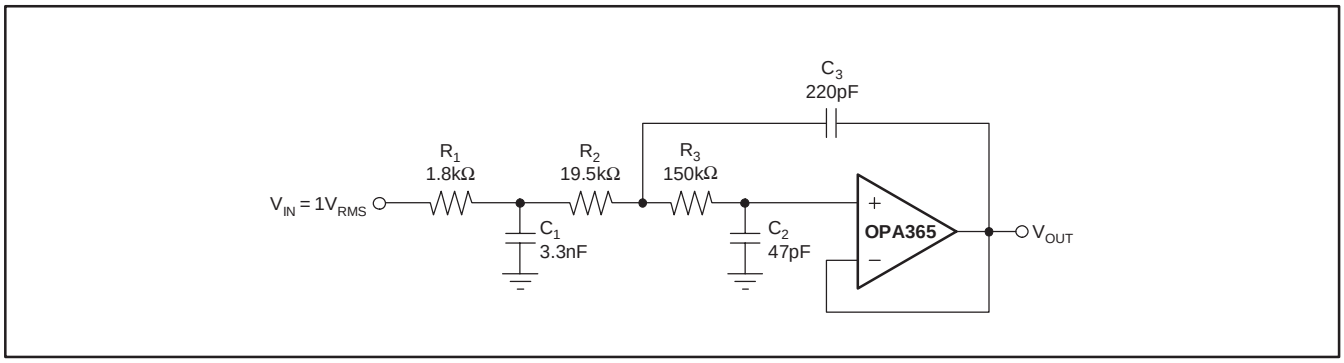
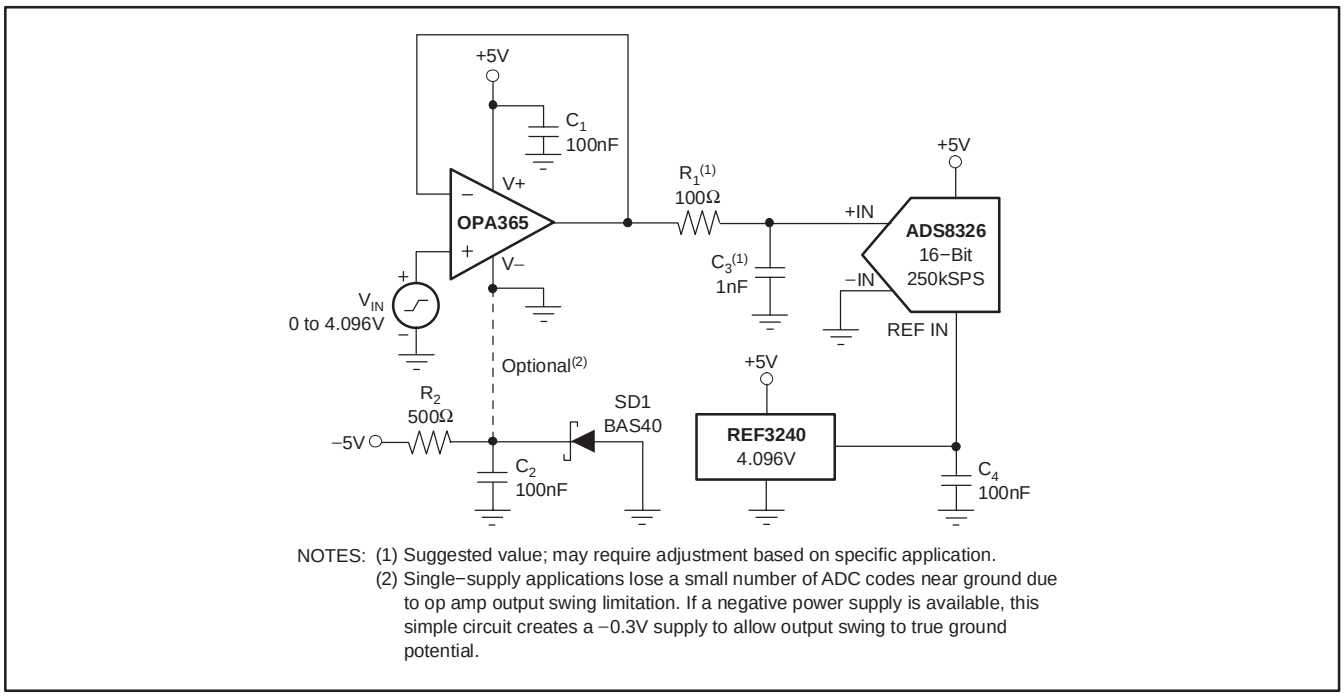


Figure 9. Configured as a 3-Pole, 20kHz, Sallen-Key Filter



NOTES: (1) Suggested value; may require adjustment based on specific application.
(2) Single−supply applications lose a small number of ADC codes near ground due to op amp output swing limitation. If a negative power supply is available, this simple circuit creates a −0.3V supply to allow output swing to true ground potential.

Figure 10. Driving the ADS8326

One method for driving an ADC that negates the need for an output swing down to 0V uses a slightly compressed ADC full-scale input range (FSR). For example, the 16-bit ADS8361 (shown in Figure 11) has a maximum FSR of 0V to 5V, when powered by a +5V supply and V_{REF} of 2.5V. The idea is to match the ADC input range with the op amp full linear output swing range; for example, an output range of +0.1 to +4.9V. The reference output from the ADS8361 ADC is divided down from 2.5V to 2.4V using a resistive divider. The ADC FSR then becomes $4.8V_{PP}$ centered on a common-mode voltage of +2.5V. Current from the ADS8361 reference pin is limited to about ±10µA. Here, 5µA was used to bias the divider. The resistors must be precise to maintain the ADC gain accuracy. An additional benefit of this method is the elimination of the negative supply voltage; it requires no additional power-supply current.

An RC network, consisting of R_1 and C_1, is included between the op amp and the ADS8361. It not only provides a high-frequency filter function, but more importantly serves as a charge reservoir used for charging the converter internal hold capacitance. This capability assures that the op amp output linearity is maintained as the ADC input characteristics change throughout the conversion cycle. Depending on the particular application and ADC, some optimization of the R_1 and C_1 values may be required for best transient performance.

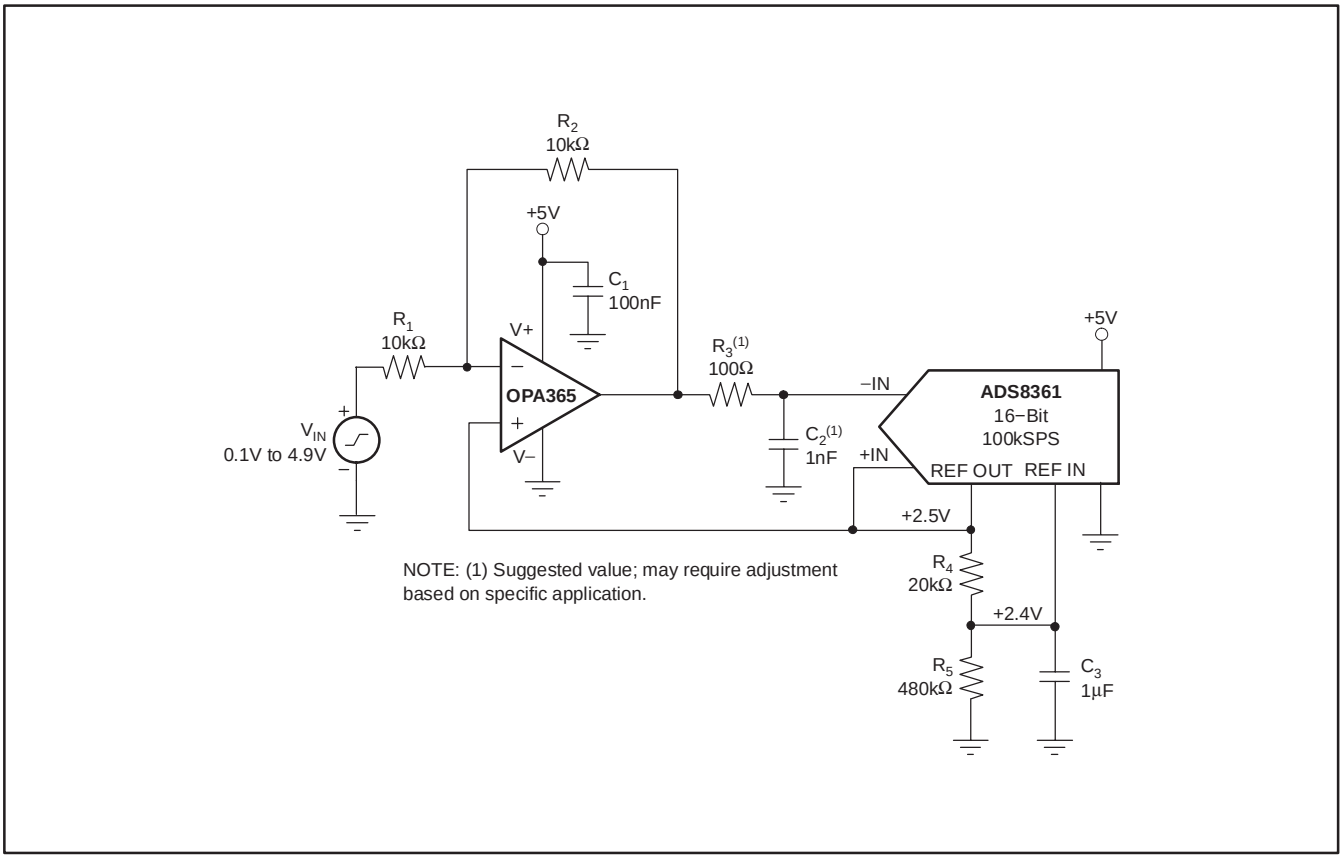


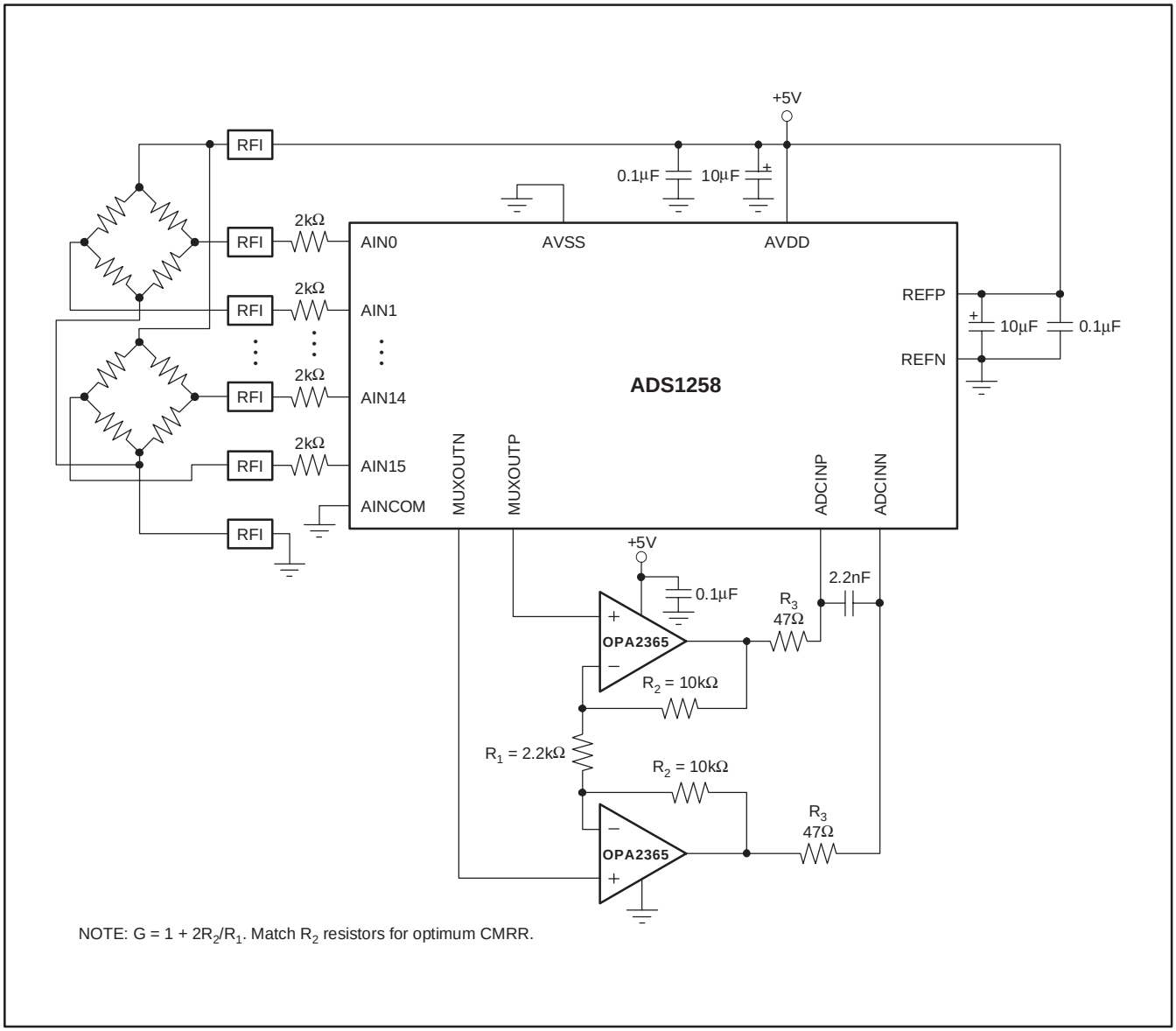
Figure 11. Driving the ADS8361

Figure 12 illustrates the OPA2365 dual op amp providing signal conditioning within an ADS1258 bridge sensor circuit. It follows the ADS1258 16:1 multiplexer and is connected as a differential in/differential out amplifier. The voltage gain for this stage is approximately 10V/V. Driving the ADS1258 internal ADC in differential mode, rather than in a single-ended, exploits the full linearity performance capability of the converter. For best common-mode rejection the two R_2 resistors should be closely matched.

Note that in Figure 12, the amplifiers, bridges, ADS1258 and internal reference are powered by the same single +5V supply. This ratiometric connection helps cancel excitation voltage drift effects and noise. For best performance, the +5V supply should be as free as possible of noise and transients.

When the ADS1258 data rate is set to maximum and the chop feature enabled, this circuit yields 12 bits of noise-free resolution with a 50mV full-scale input.

The chop feature is used to reduce the ADS1258 offset and offset drift to very low levels. A 2.2nF capacitor is required across the ADC inputs to bypass the sampling currents. The 47Ω resistors provide isolation for the OPA2365 outputs from the relatively large, 2.2nF capacitive load. For more information regarding the ADS1258, see the product data sheet available for down load at www.ti.com.



NOTE: G = 1 + $2R_2/R_1$. Match R_2 resistors for optimum CMRR.

Figure 12. Conditioning Input Signals to the ADS1258 on a Single-Supply

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA2365AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2365AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2365AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2365AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA365AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA365AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA365AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA365AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA365AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA365AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA365AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA365AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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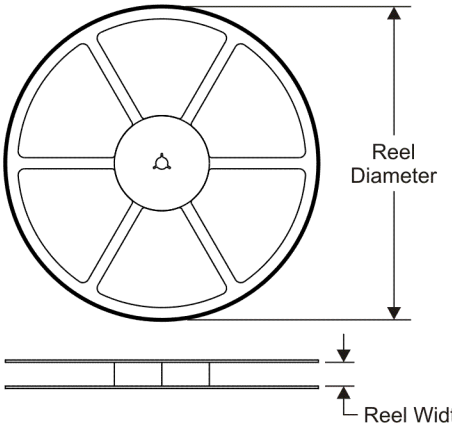
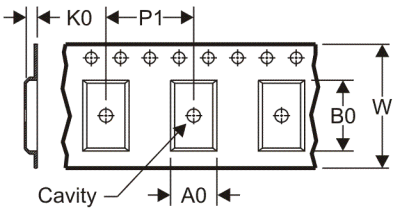
REEL DIMENSIONS

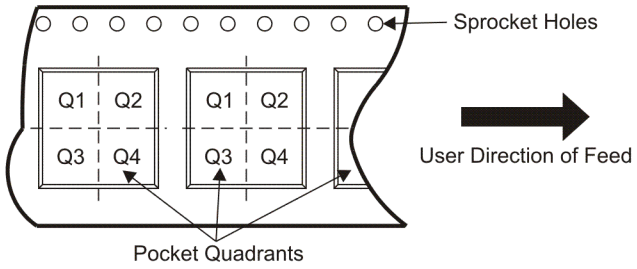


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

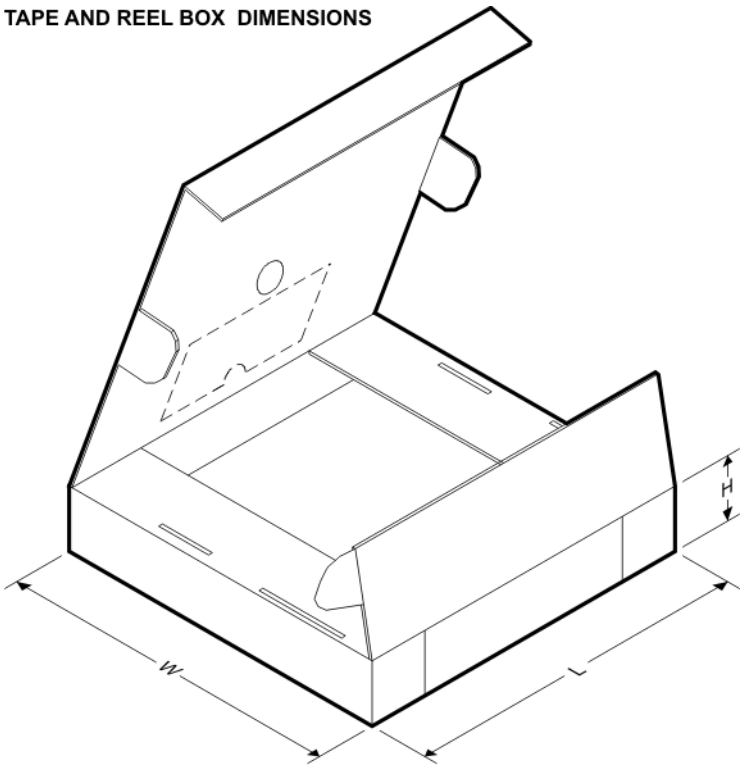
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2365AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA365AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA365AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA365AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

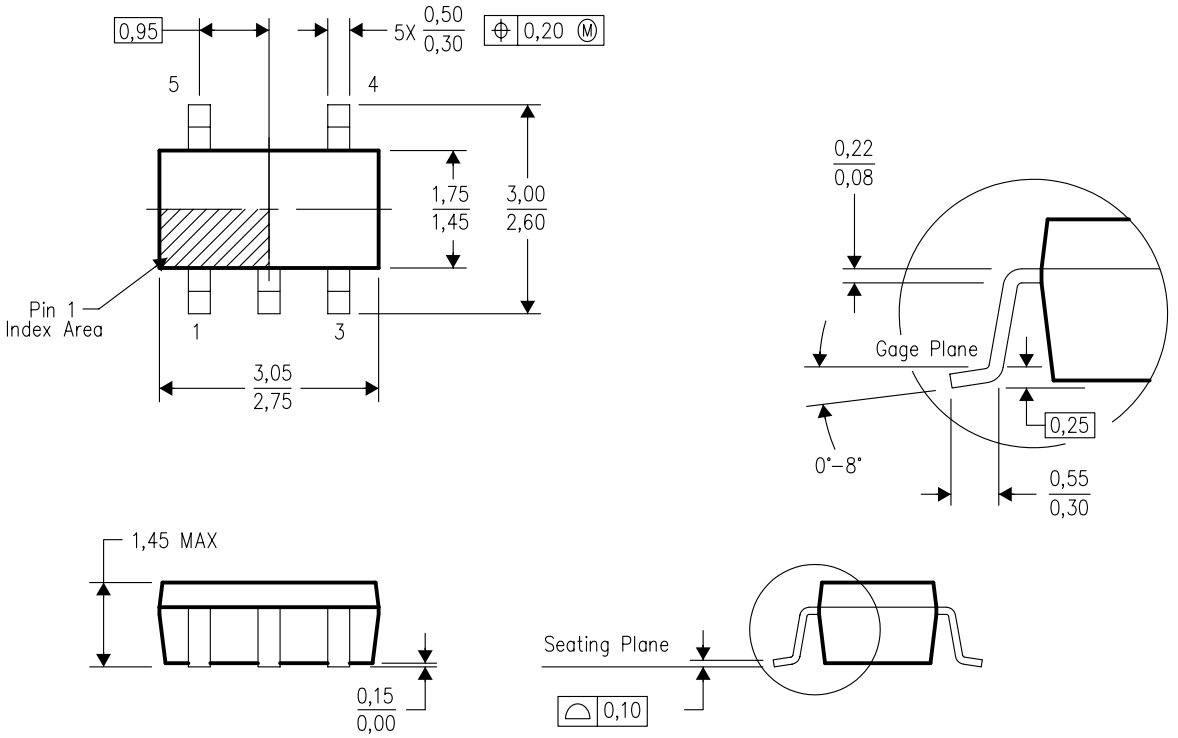
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2365AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA365AIDBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
OPA365AIDBVT	SOT-23	DBV	5	250	195.0	200.0	45.0
OPA365AIDR	SOIC	D	8	2500	346.0	346.0	29.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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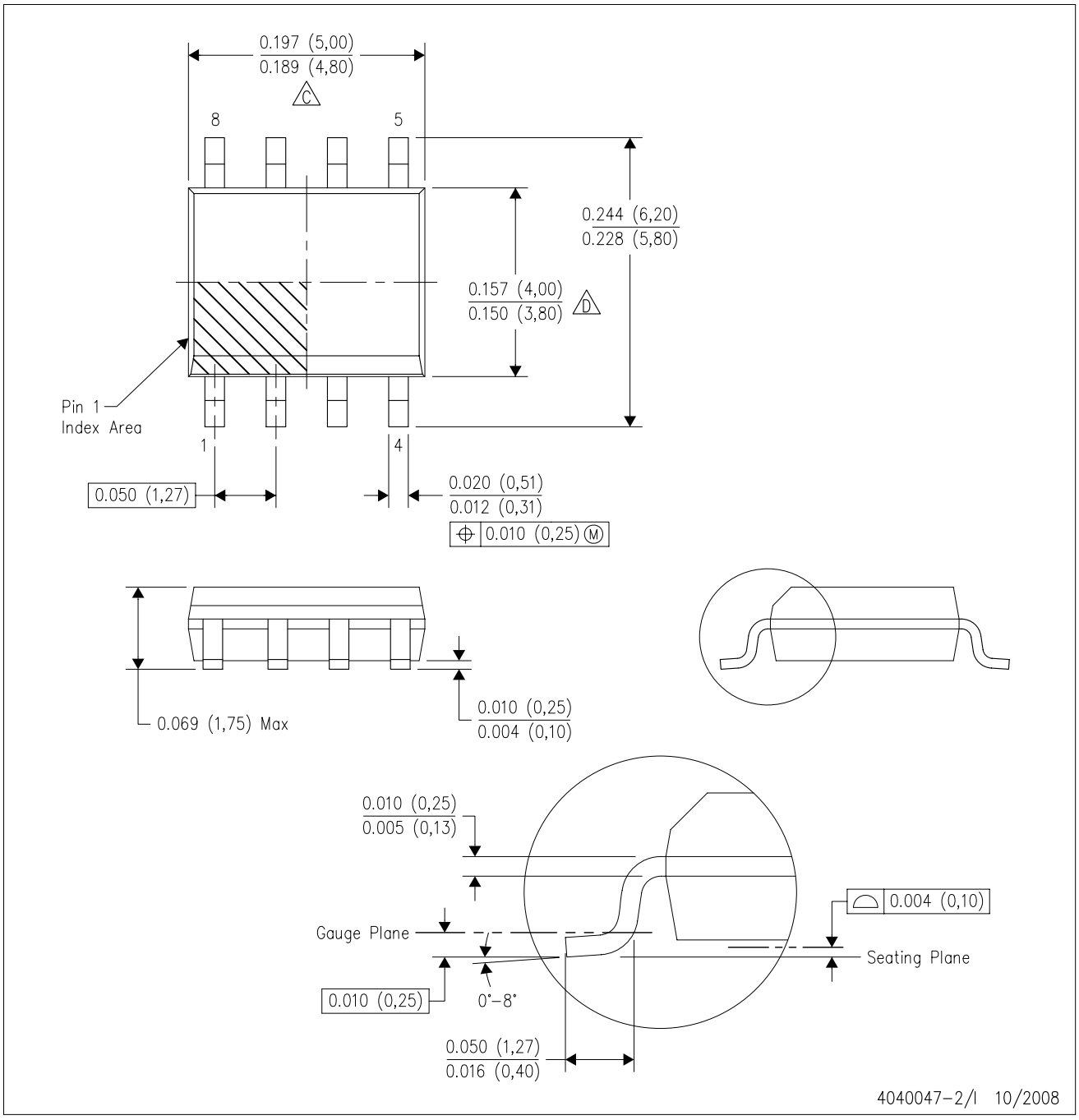
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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