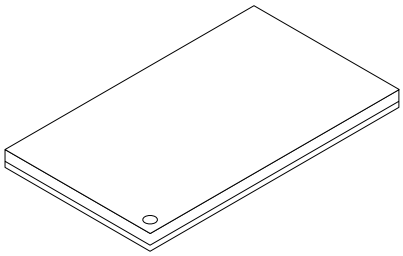
High Speed NAND Flash Memory

MT29H8G08ACAH1
MT29H16G08ECAH1
MT29H32G08GCAH2

Features

- Open NAND Flash Interface (ONFI) 2.0 compliant[1]
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 4,320 bytes (4,096 + 224 bytes)
  - Block size: 128 pages (512K + 28K bytes)
  - Plane size: 4 planes × 512 blocks per plane
  - Device size: 8Gb: 2,048 blocks; 16Gb: 4,096 blocks; 32Gb: 8,192 blocks
- I/O READ performance
  - Transfer rate: 6ns (DDR)
  - Read throughput per pin: 166 MT/s
  - SET FEATURES selects asynchronous/DDR mode for data output
- I/O WRITE performance
  - Transfer rate: 6ns (DDR)
  - Loading throughput per pin: 166 MT/s
  - SET FEATURES selects asynchronous/DDR mode for data input
  - Command/address entry on rising edge of CLK
- Array performance
  - Read single plane: 25µs (MAX)
  - Read multiplane: 30µs (MAX)
  - Program time: 160µs (TYP)
  - Erase time: 3ms (TYP)
- Operating voltage range
  - V_{CC}: 2.7–3.6V
  - $V_{CC}Q$: 1.7–1.95V
- Command set: ONFI NAND Flash protocol
- Advanced command set:
  - Program page cache
  - Sequential and random read page cache
  - One-time programmable (OTP) mode
  - Multiplane commands
  - Multi-LUN operations
  - Read unique ID
  - Copyback

Figure 1:100-Ball VBGA



- Operation status byte provides software method for detecting:
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data I/O in the synchronous interface
- Copyback operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: 10 years
  - Endurance: 100,000 PROGRAM/ERASE cycles
  - Operating temperature:
    Commercial: 0°C to +70°C
    Wireless: –25°C to +85°C
- First block (block address 00h) is valid with ECC
- Package: 100-ball VBGA
- RESET (FFh) required as first command following power-on

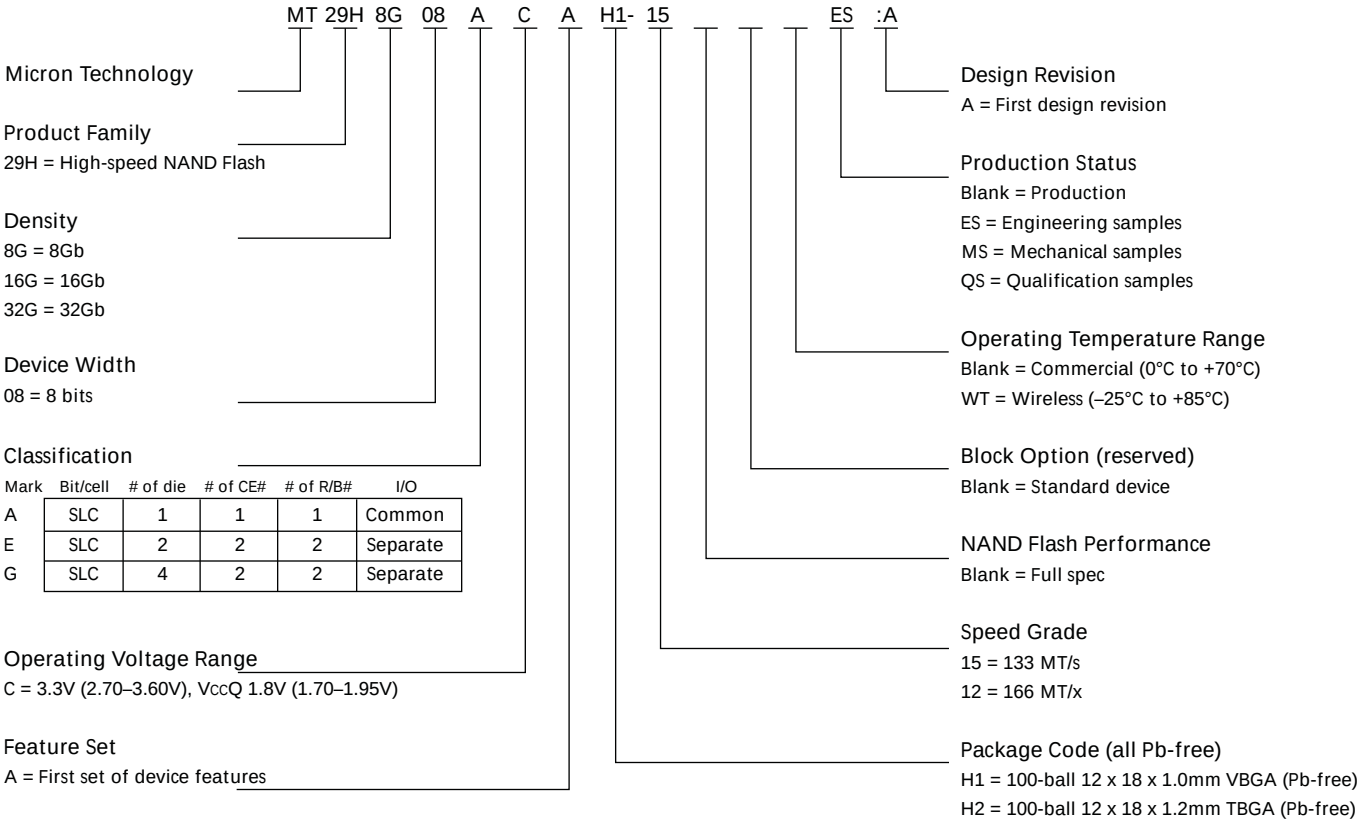
Notes: 1. The ONFI 2.0 specification will be published at www.onfi.org.

‡This data sheet contains the present description of a product in definition with no formal design in progress.

Part Numbering Information

Micron NAND Flash devices are available in several configurations and densities (see Figure 2).

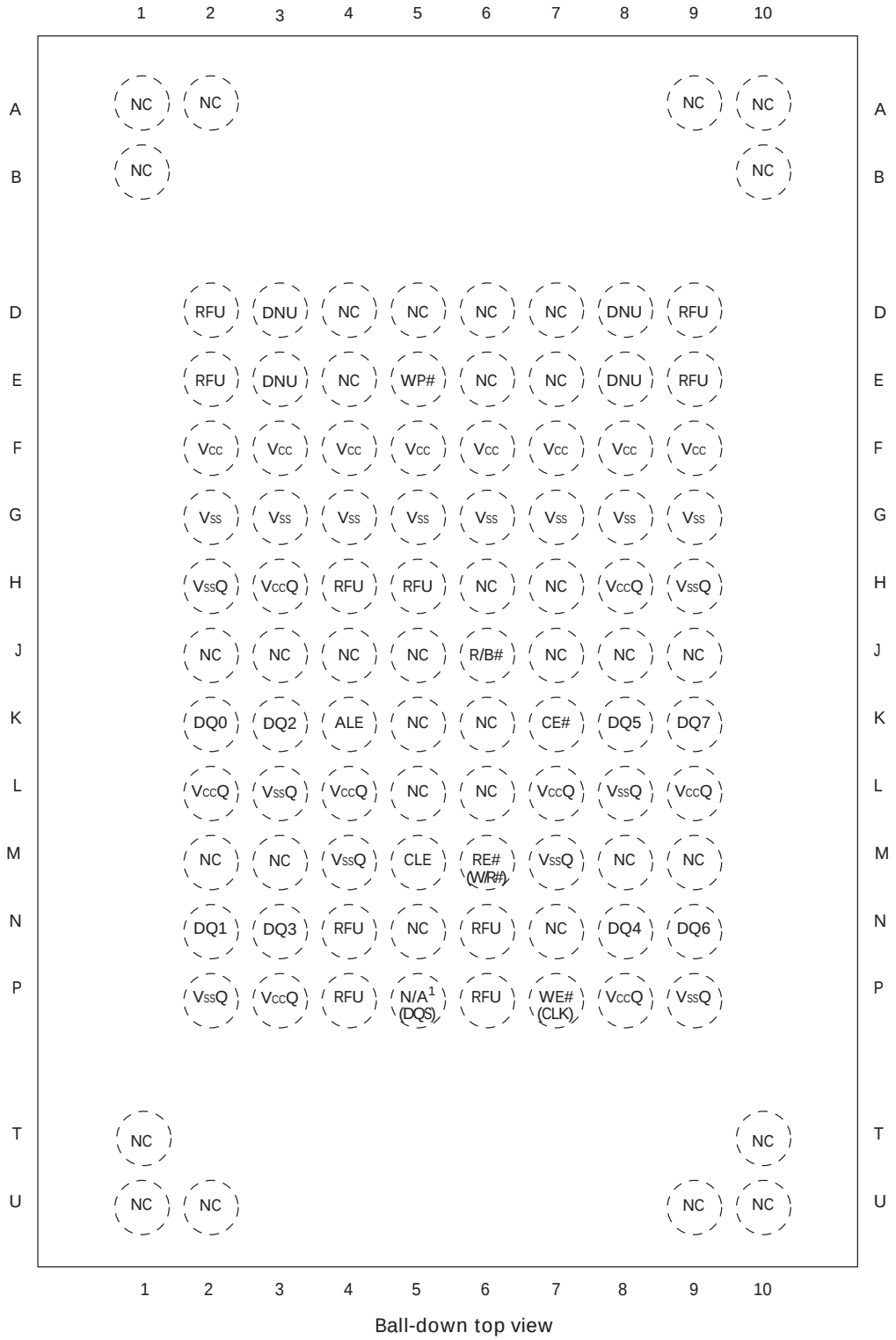
Figure 2: Part Number Chart



Valid Part Number Combinations

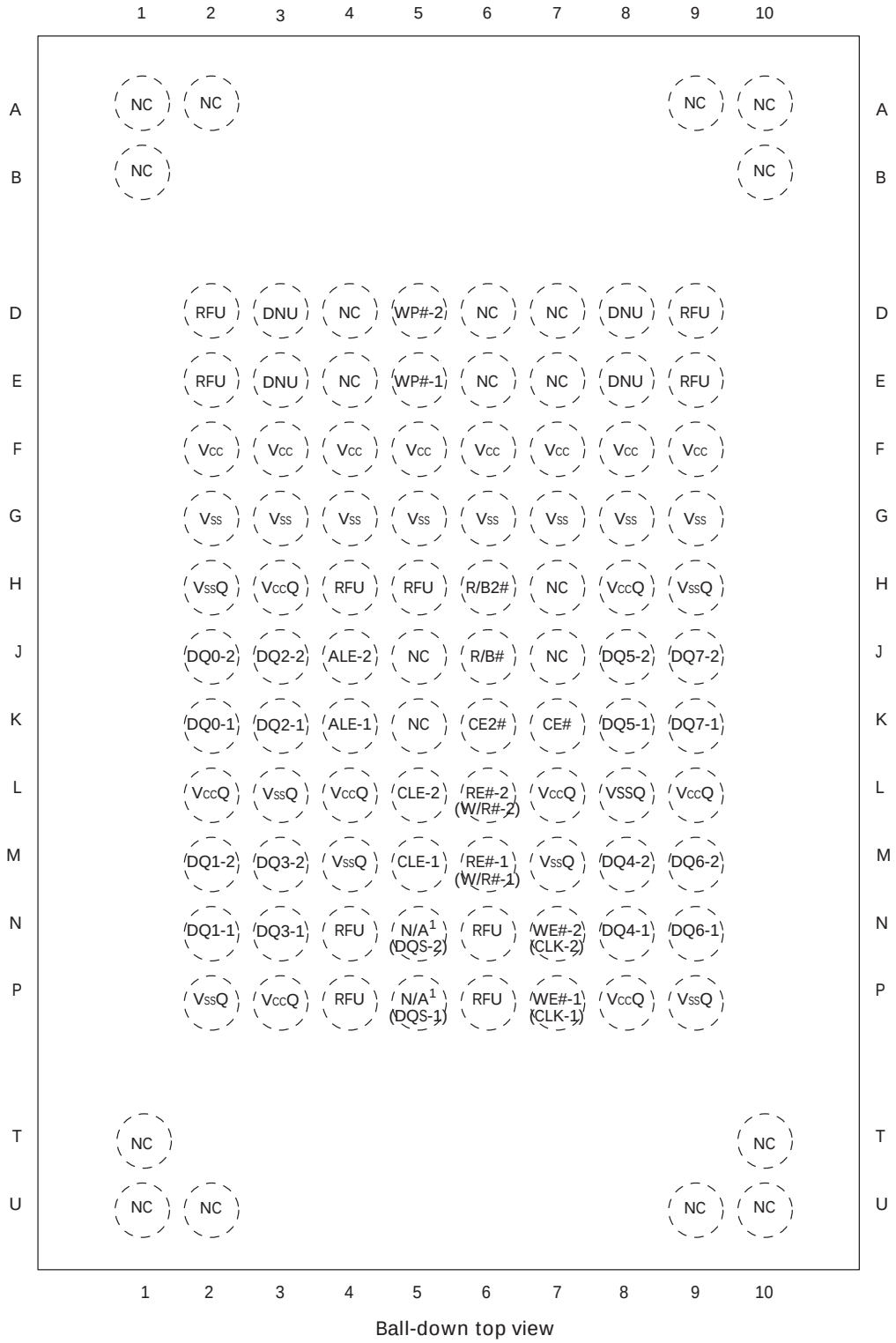
After building the part number from the part numbering chart, verify that the part is offered and valid by using the Micron Parametric Part Search Web site at: http://www.micron.com/products/parametric. If the device required is not on this list, contact the factory.

Figure 3: Ball Assignment: 100-Ball VBGA Single x8 Device (MT29H8G08ACAH1)



Notes: 1. N/A: This signal is tri-stated when the asynchronous interface is active. Signal names in parentheses are the signal names when the synchronous interface is active.

Figure 4: Ball Assignment: 100-Ball VBGA/TBGA Dual x8 (MT29H16G08ECAH1, MT29H32G08GCAH2)



Ball-down top view

Notes: 1. N/A: This signal is tri-stated when the asynchronous interface is active. Signal names in parentheses are the signal names when the synchronous interface is active.

Table 1: Signal Definitions

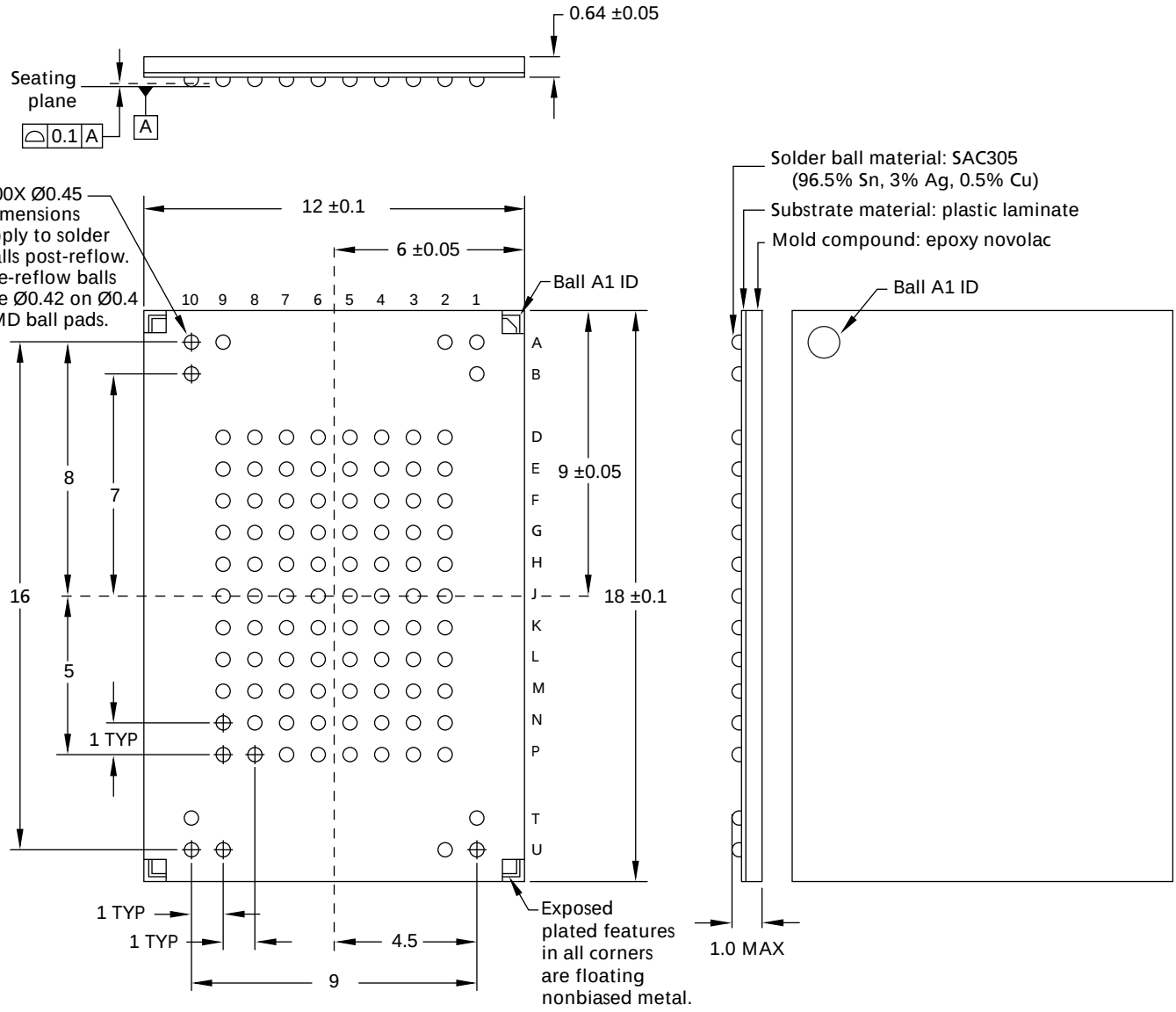
Symbol		Type	Description
Async	**Sync**		
ALE, ALE-1, ALE-2	ALE, ALE-1, ALE-2	Input	**Address latch enable:** Loads an address from DQ[7:0] into the address register. *Asynchronous interface:* When HIGH, the address on DQ[7:0] is latched on the rising edge of WE#. *Synchronous interface:* When HIGH, the address on DQ[7:0] is latched on the rising edge of CLK.
CE#, CE2#	CE#, CE2#	Input	**Chip enable:** An asynchronous-only signal that enables one or more logical units when driven LOW. When driven HIGH, other signals are disabled. When CE# is pulled LOW, ALE and CLE must remain LOW during ^{t}CS and ^{t}CAD. For the 16Gb device, CE# controls the first 8Gb of memory (-1); CE2# controls the second 8Gb of memory (-2). For the 32Gb device, CE# controls the first 16Gb of memory (-1); CE2# controls the second 16Gb of memory (-2).
CLE, CLE-1, CLE-2	CLE, CLE-1, CLE-2	Input	**Command latch enable:** Loads a command from DQ[7:0] into the command register. *Asynchronous interface:* When HIGH, the command on DQ[7:0] is latched on the rising edge of WE#. *Synchronous interface:* When HIGH, the command on DQ[7:0] is latched on the rising edge of CLK.
RE#, RE#-1, RE#-2	W/R#, W/R#-1, W/R#-2	Input	**Read enable/(Write/Read#)** *Asynchronous interface:* Read enable transfers serial data from the NAND Flash to the host system. *Synchronous interface:* Write/Read# is latched HIGH for command, address, and data input. When latched LOW, the NAND Flash device drives DQ[7:0] and DQS. This signal is latched on the rising edge of CLK.
WE#, WE#-1, WE#-2	CLK, CLK-1, CLK-2	Input	**Write enable/Clock** *Asynchronous interface:* Write enable transfers commands, addresses, and serial data from the host system to the NAND Flash. *Synchronous interface:* A free-running clock when CE# is LOW. When ALE is HIGH and CLE is LOW, addresses are latched in the address register. When ALE is LOW and CLE is HIGH, commands are latched in the command register. When CE# is HIGH, the host can disable CLK.
WP#, WP#-1, WP#-2	WP#, WP#-1, WP#-2	Input	**Write protect:** An asynchronous-only signal that disables array PROGRAM and ERASE operations when LOW.
DQ[7:0], DQ[7:0]-1, DQ[7:0]-2	DQ[7:0], DQ[7:0]-1, DQ[7:0]-2	Input/ output	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information. *Asynchronous interface:* Data is output only during READ operations when RE# is LOW; at other times, DQ[7:0] are inputs. *Synchronous interface:* Data is output only during READ operations when W/R# is LOW; at other times, DQ[7:0] are inputs.
N/A	DQS, DQS-1, DQS-2	Input/ output	**Data strobe** *Asynchronous interface:* This signal is tri-stated. *Synchronous interface:* When ALE, CLE, and W/R# are HIGH, the NAND Flash latches data input from DQ[7:0] on the rising and falling edges of DQS. When ALE and CLE are HIGH and W/R# is LOW, the NAND Flash outputs data on DQ[7:0], edge-aligned to the rising and falling edges of DQS.
R/B#, R/B2#	R/B#, R/B2#	Output	**Ready/Busy#:** An open-drain, active-low output that requires an external pull-up resistor.
V_{CC}	V_{CC}	Supply	Vcc: Core power supply.
V_{CCQ}	V_{CCQ}	Supply	VccQ: I/O power supply.

Table 1: Signal Definitions (continued)

Symbol		Type	Description
Async	Sync		
V_{SS}	V_{SS}	Supply	V_{SS}: Core ground connection.
$V_{SS}Q$	$V_{SS}Q$	Supply	$V_{SS}Q$: I/O ground connection.
NC	NC		No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	DNU		Do not use: DNUs must be left unconnected.
RFU	RFU		Reserved for future use: RFUs must be left unconnected.

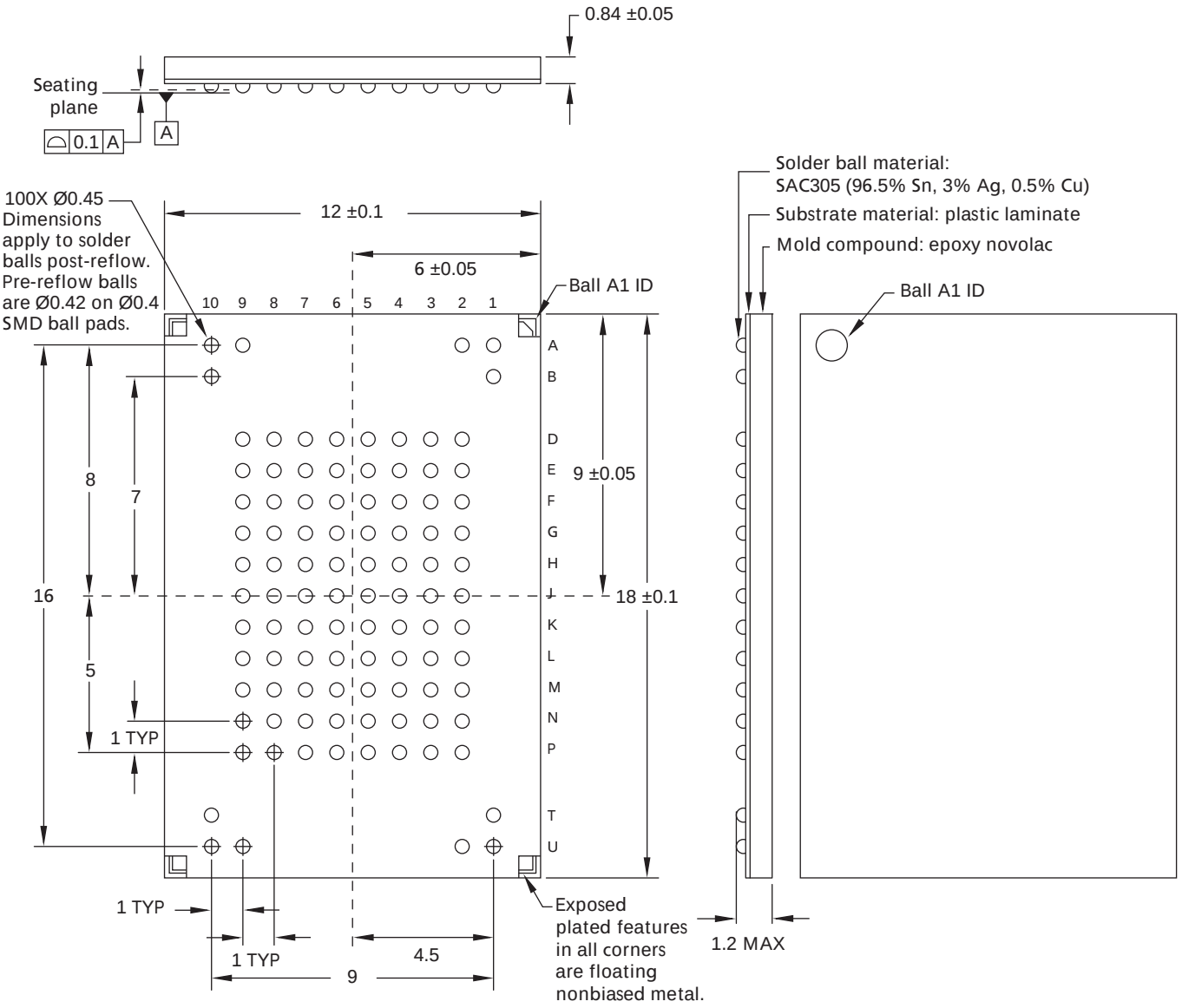
Package Dimensions

Figure 5: 100-Ball VBGA (Package Code H1), 12 × 18



Note: All dimensions are in millimeters.

Figure 6: 100-Ball TBGA (Package Code H2), 12 × 18



Note: All dimensions are in millimeters.

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