MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply-Voltage Range: 1.8 V to 3.6 V
- Ultralow Power Consumption
  - Active Mode (AM): 200 μA/MHz (Typ)
  - Standby Mode (LPM3 RTC Mode): 2.5 μA (Typ)
  - Off Mode (LPM4 RAM Retention): 1.5 μA (Typ)
  - Shutdown Mode (LPM5): 0.2 μA (Typ)
- Wake-Up From Standby Mode in Less Than 5 μs
- 16-Bit RISC Architecture, Extended Memory, up to 25-MHz System Clock
- Flexible Power Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low Power/Low Frequency Internal Clock Source (VLO)
  - Low Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Watch Crystals (XT1)
  - High-Frequency Crystals up to 32 MHz (XT2)
- 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
- 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TA2, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TB0, Timer_B With Seven Capture/Compare Shadow Registers
- Two Universal Serial Communication Interfaces
  - USCI_A0 and USCI_A1 Each Supporting
    - Enhanced UART supporting Auto-Baudrate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI_B0 and USCI_B1 Each Supporting
    - I^2C^{TM}
    - Synchronous SPI
- Full-Speed Universal Serial Bus (USB)
  - Integrated USB-PHY
  - Integrated 3.3 V/1.8 V USB Power System
  - Integrated USB-PLL
  - Eight Input, Eight Output Endpoints
- 12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature (MSP430F552x Only)
- Comparator
- Hardware Multiplier Supporting 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- Three Channel Internal DMA
- Basic Timer With Real-Time Clock Feature
- Family Members are Summarized in Table 1
- For Complete Module Descriptions, See the *MSP430x5xx Family User's Guide* (SLAU208)

PRODUCT PREVIEW

DESCRIPTION

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 5 μs.

The MSP430F5529, MSP430F5527, MSP430F5525, and MSP430F5521 are microcontroller configurations with integrated USB and PHY supporting USB 2.0, four 16-bit timers, a high-performance 12-bit analog-to-digital converter (ADC), two universal serial communication interfaces (USCI), hardware multiplier, DMA, real-time clock module with alarm capabilities, and 63 I/O pins. The MSP430F5528, MSP430F5526, MSP430F5524, and MSP430F5522 include all of these peripherals but have 47 I/O pins.

The MSP430F5519, MSP430F5517, and MSP430F5515 are microcontroller configurations with integrated USB and PHY supporting USB 2.0, four 16-bit timers, two universal serial communication interfaces (USCI), hardware multiplier, DMA, real time clock module with alarm capabilities, and 63 I/O pins. The MSP430F5514 and MSP430FF5513 include all of these peripherals but have 47 I/O pins.

Typical applications include analog and digital sensor systems, data loggers, etc. that require connectivity to various USB hosts.

Family members available are summarized in Table 1.

Table 1. Family Members

Device	Flash (KB)	SRAM (KB)(1)	Timer_A(2)	Timer_B(3)	USCI		ADC12_A (Ch)	Comp_B (Ch)	I/O	Package Type
					Channel A: UART/IrDA/ SPI	Channel B: SPI/I²C				
MSP430F5529	128	8 + 2	5, 3, 3	7	2	2	12 ext / 4 int	12	63	80 PN
MSP430F5528	128	8 + 2	5, 3, 3	7	2	2	8 ext / 4 int	8	47	64 RGC, 80 ZQE
MSP430F5527	96	6 + 2	5, 3, 3	7	2	2	12 ext / 4 int	12	63	80 PN
MSP430F5526	96	6 + 2	5, 3, 3	7	2	2	8 ext / 4 int	8	47	64 RGC, 80 ZQE
MSP430F5525	64	4 + 2	5, 3, 3	7	2	2	12 ext / 4 int	12	63	80 PN
MSP430F5524	64	4 + 2	5, 3, 3	7	2	2	8 ext / 4 int	8	47	64 RGC, 80 ZQE
MSP430F5522(4)	32	8 + 2	5, 3, 3	7	2	2	8 ext / 4 int	8	47	64 RGC, 80 ZQE
MSP430F5521(4)	32	6 + 2	5, 3, 3	7	2	2	12 ext/ 4 int	12	63	80 PN
MSP430F5519(4)	128	8 + 2	5, 3, 3	7	2	2	-	12	63	80 PN
MSP430F5517(4)	96	6 + 2	5, 3, 3	7	2	2	-	12	63	80 PN
MSP430F5515	64	4 + 2	5, 3, 3	7	2	2	-	12	63	80 PN
MSP430F5514	64	4 + 2	5, 3, 3	7	2	2	-	8	47	64 RGC, 80 ZQE
MSP430F5513(4)	32	4 + 2	5, 3, 3	7	2	2	-	8	47	64 RGC, 80 ZQE

(1) The additional 2 KB USB SRAM that is listed can be used as general purpose SRAM when USB is not in use.
(2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(3) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(4) Product Preview

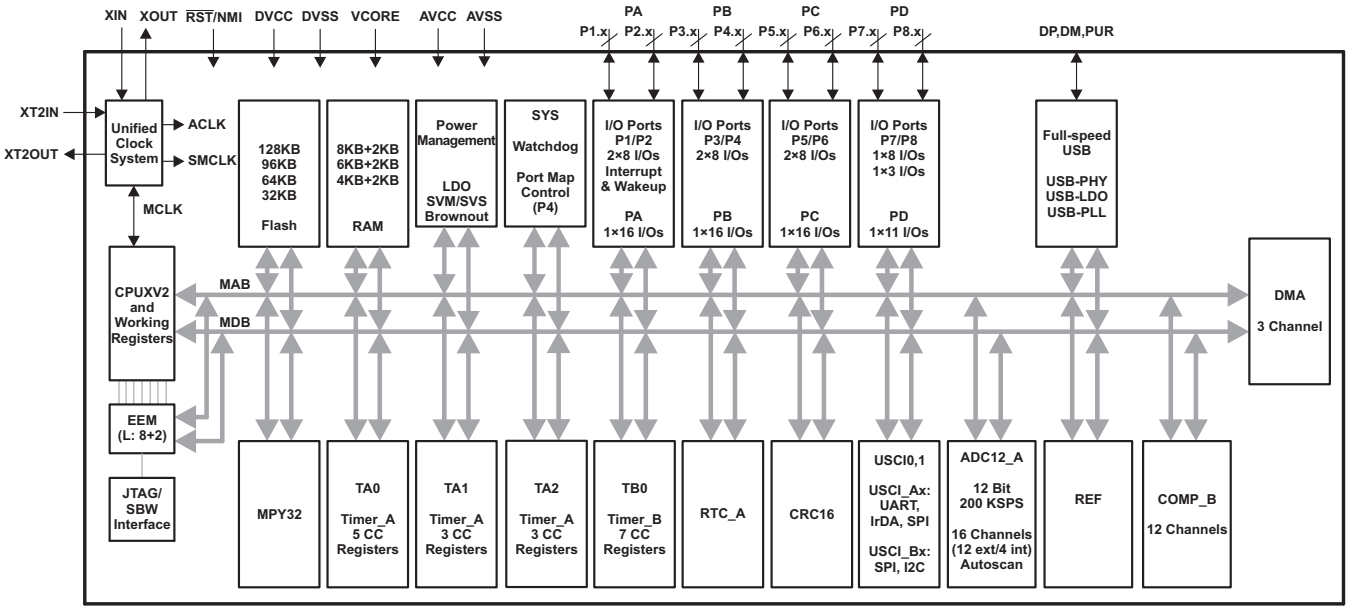
PRODUCT PREVIEW

ORDERING INFORMATION(1)

T_A	PACKAGED DEVICES(2)		
	PLASTIC 80-PIN TQFP (PN)	PLASTIC 64-PIN QFN (RGC)	PLASTIC 80-BALL BGA (ZQE)
–40°C to 85°C	MSP430F5529IPN	MSP430F5528IRGC	MSP430F5528IZQE(3)
	MSP430F5527IPN	MSP430F5526IRGC	MSP430F5526IZQE(3)
	MSP430F5525IPN	MSP430F5524IRGC	MSP430F5524IZQE(3)
	MSP430F5521IPN(3)	MSP430F5522IRGC(3)	MSP430F5522IZQE(3)
	MSP430F5519IPN(3)	MSP430F5514IRGC	MSP430F5514IZQE(3)
	MSP430F5517IPN(3)	MSP430F5513IRGC(3)	MSP430F5513IZQE(3)
	MSP430F5515IPN(3)		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.
(3) Product Preview

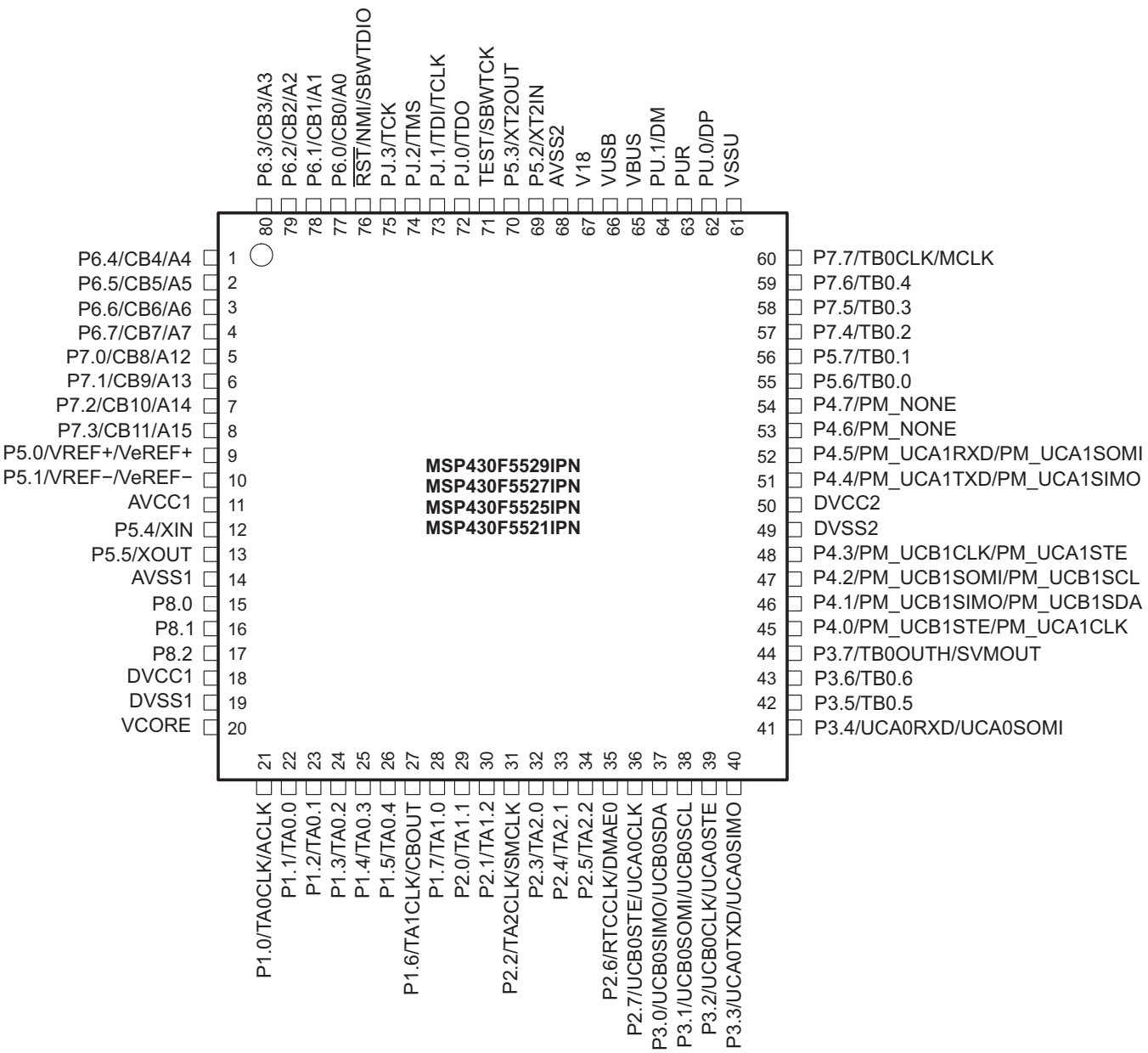
Functional Block Diagram – MSP430F5529IPN, MSP430F5527IPN, MSP430F5525IPN, MSP430F5521IPN



PRODUCT PREVIEW

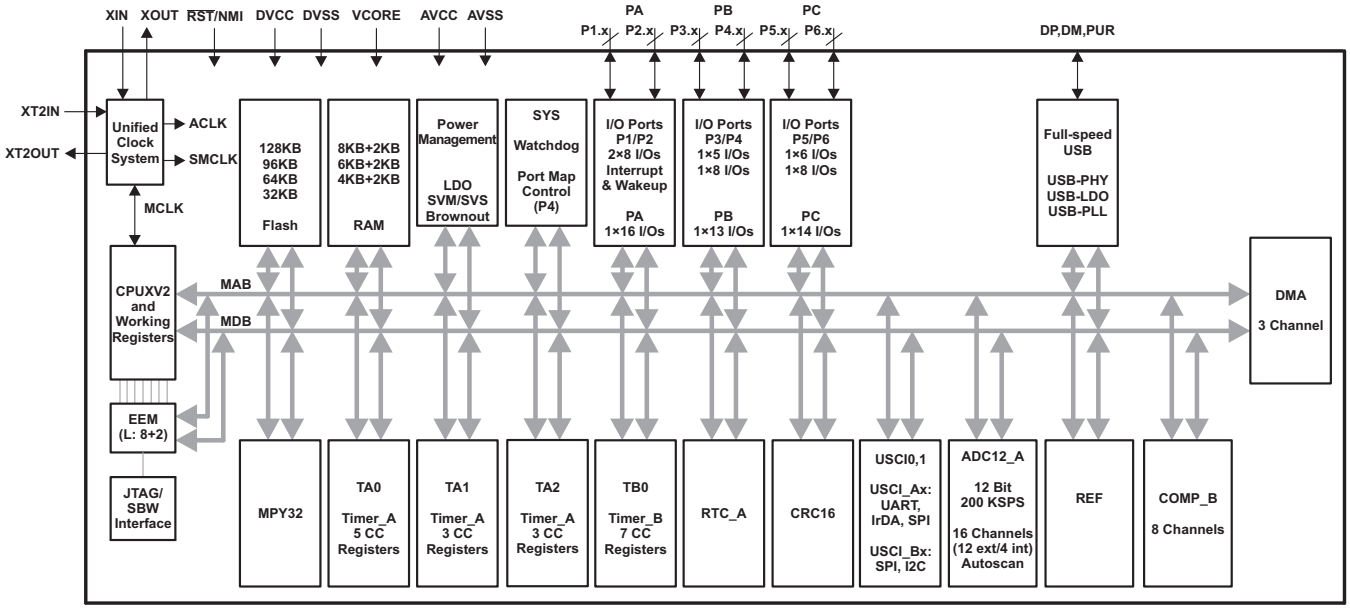
Pin Designation – MSP430F5529IPN, MSP430F5527IPN, MSP430F5525IPN, MSP430F5521IPN

PN PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

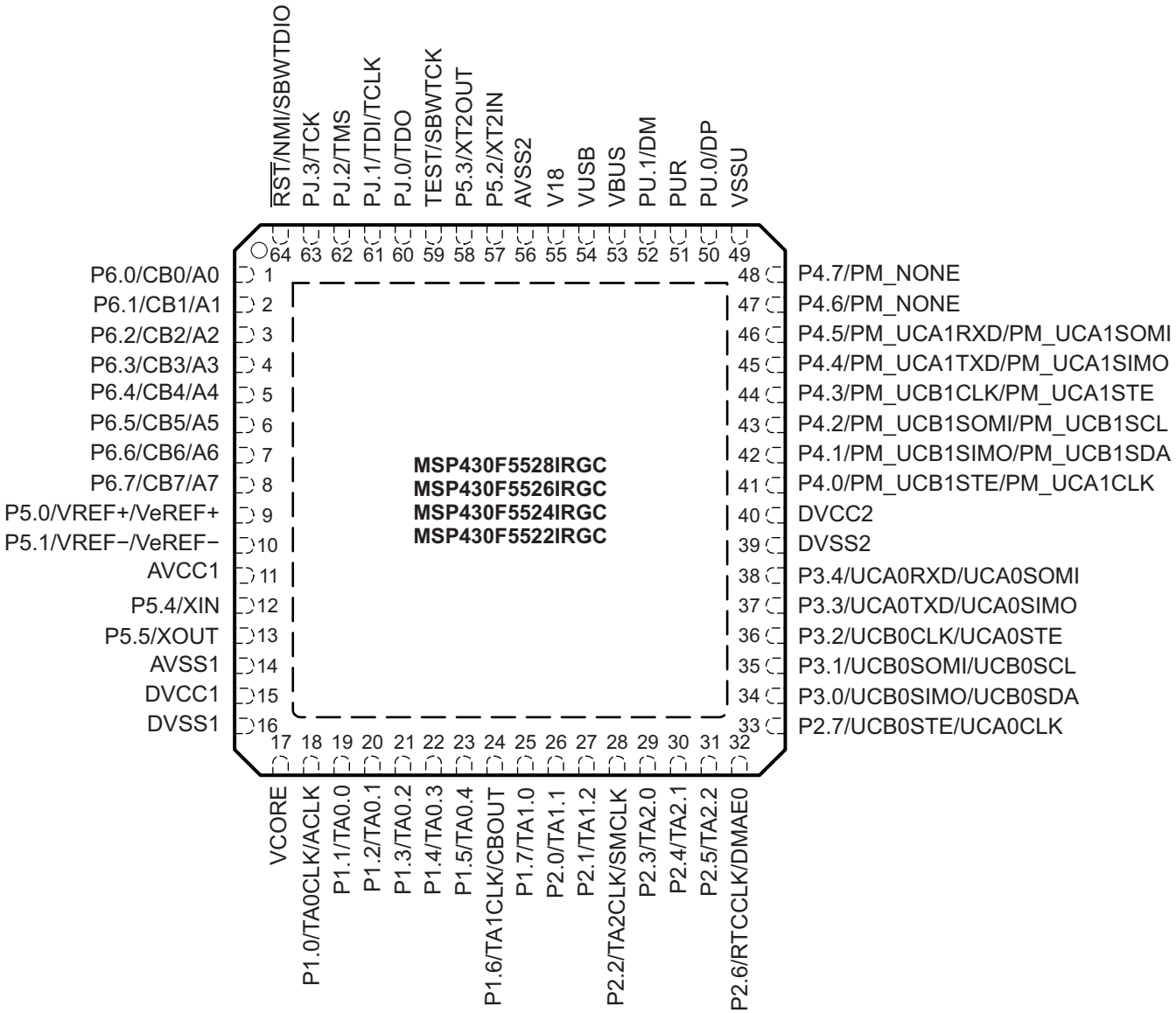
Functional Block Diagram – MSP430F5528IRGC, MSP430F5526IRGC, MSP430F5524IRGC, MSP430F5522IRGC, MSP430F5528IZQE, MSP430F5526IZQE, MSP430F5524IZQE, MSP430F5522IZQE



PRODUCT PREVIEW

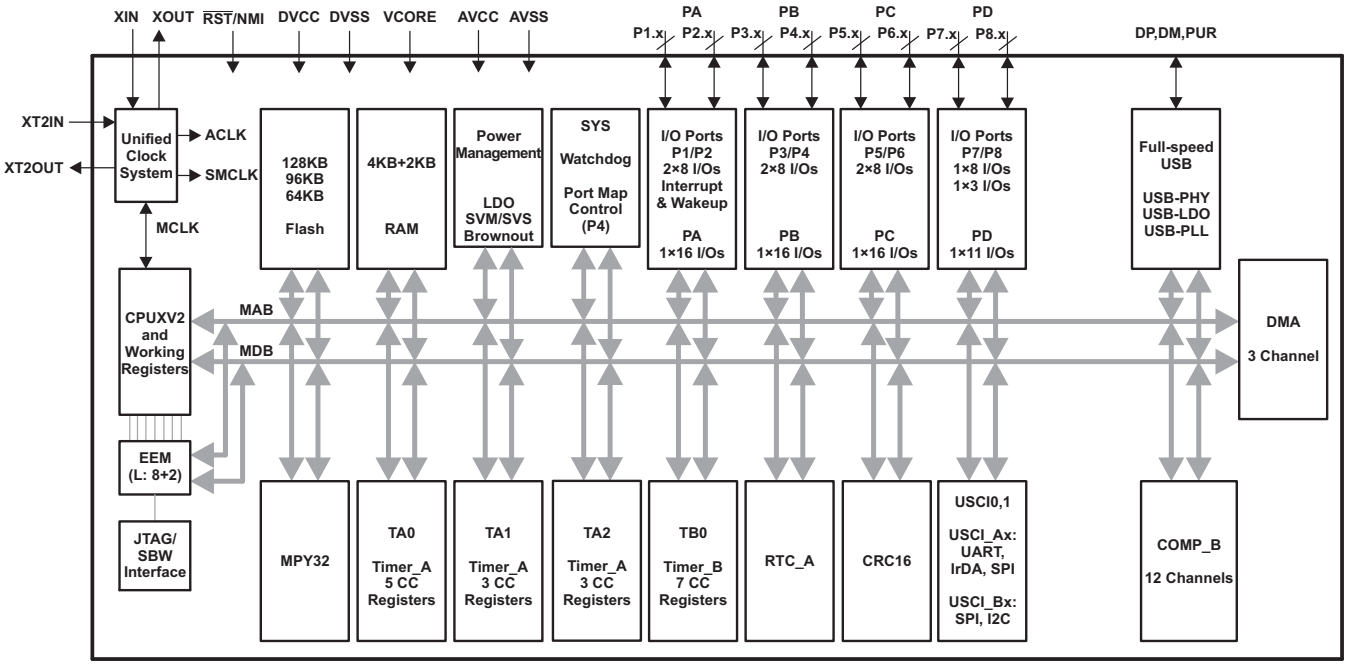
Pin Designation – MSP430F5528IRGC, MSP430F5526IRGC, MSP430F5524IRGC, MSP430F5522IRGC

RGC PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

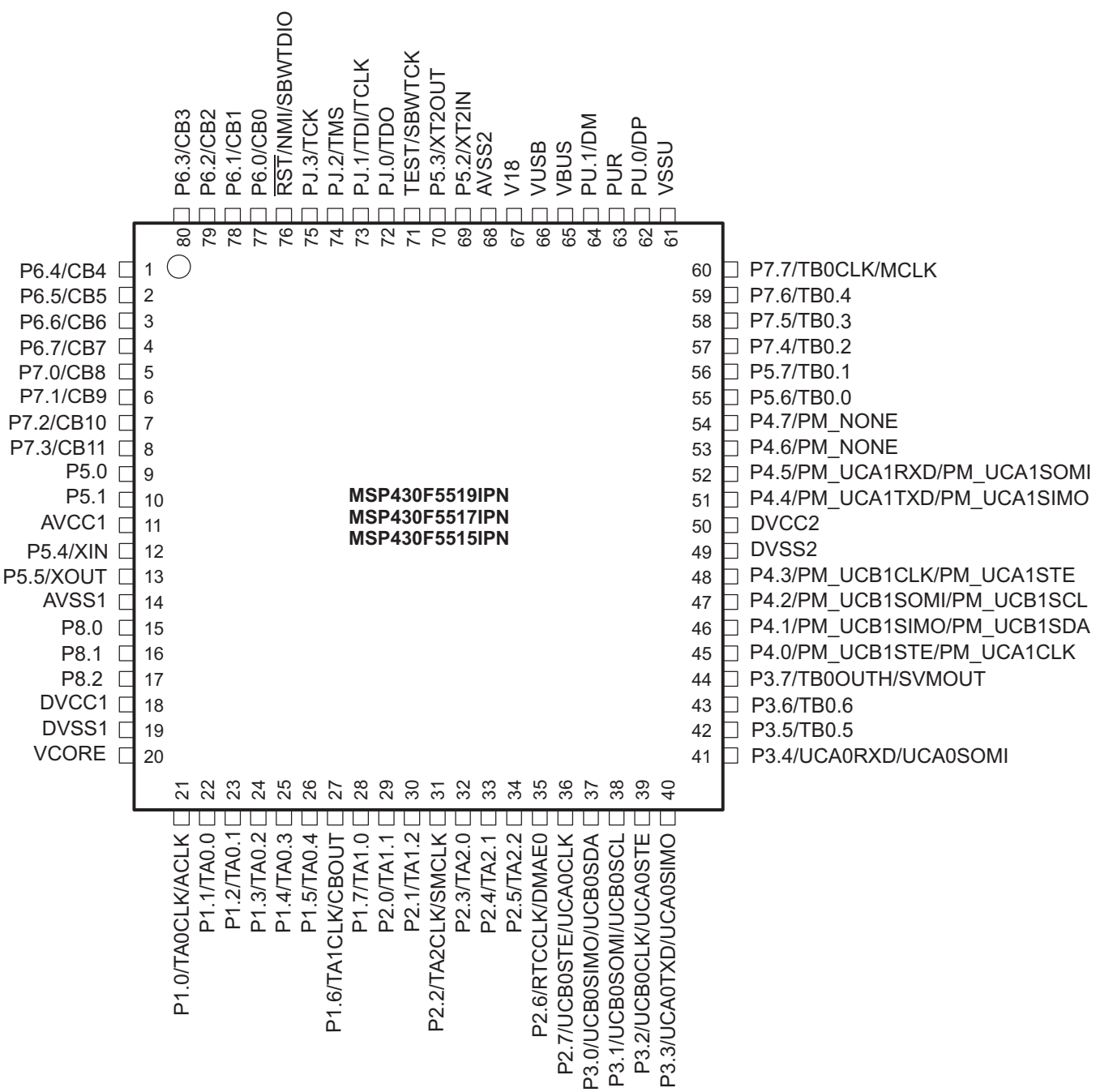
Functional Block Diagram – MSP430F5519IPN, MSP430F5517IPN, MSP430F5515IPN



PRODUCT PREVIEW

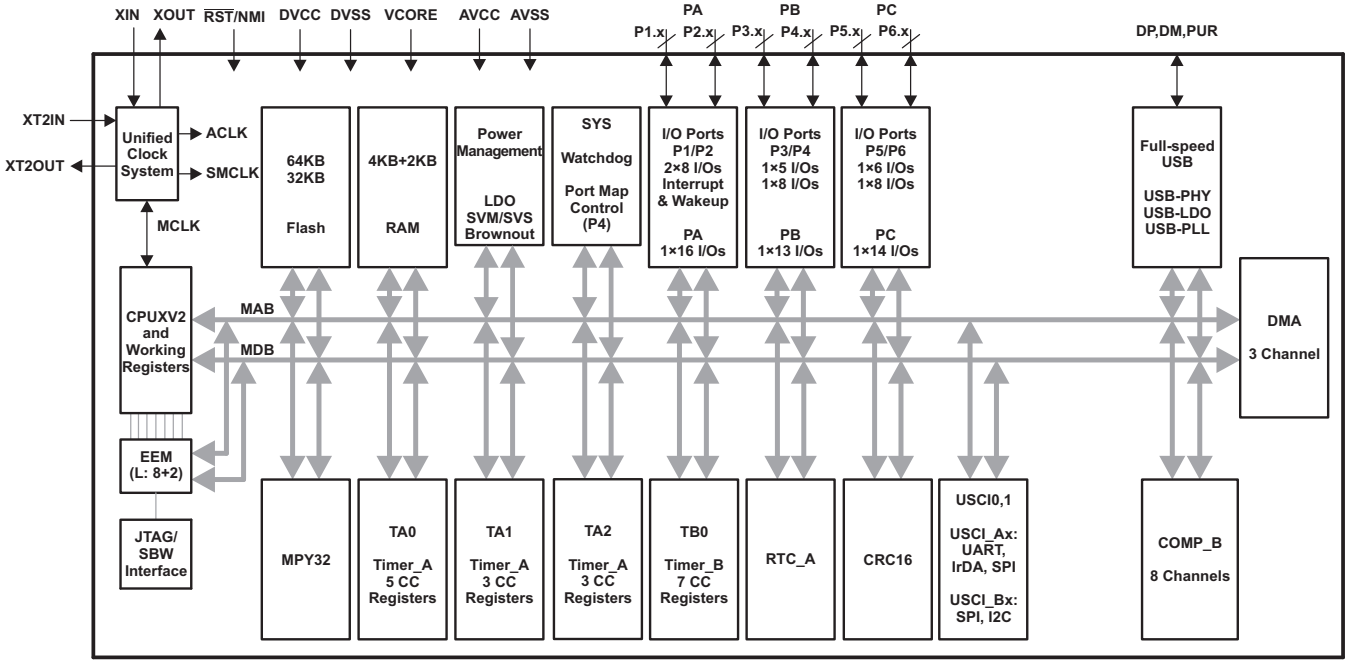
Pin Designation – MSP430F5519IPN, MSP430F5517IPN, MSP430F5515IPN

PN PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

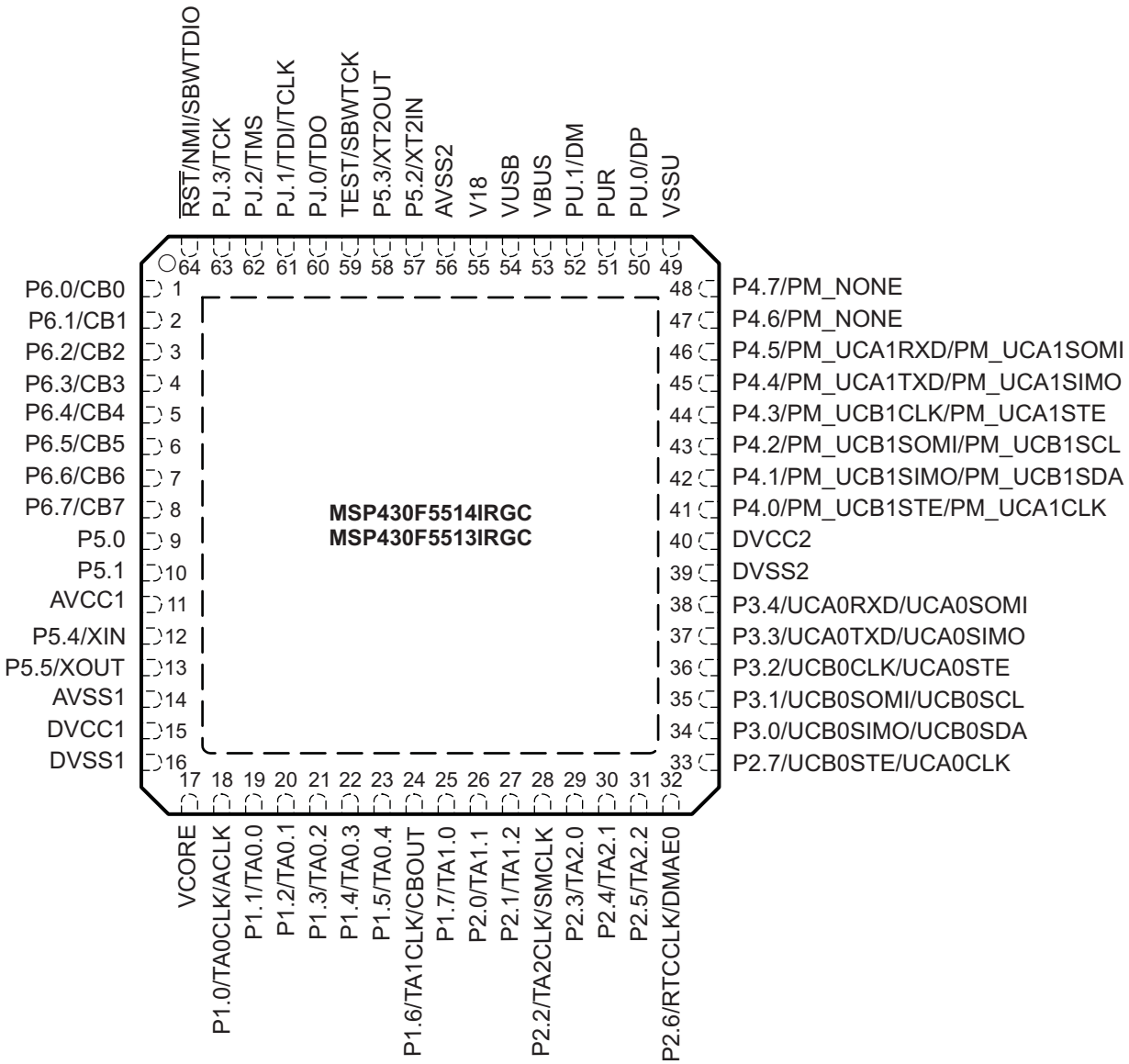
Functional Block Diagram – MSP430F5514IRGC, MSP430F5513IRGC, MSP430F5514IZQE, MSP430F5513IZQE



PRODUCT PREVIEW

Pin Designation – MSP430F5514IRGC, MSP430F5513IRGC

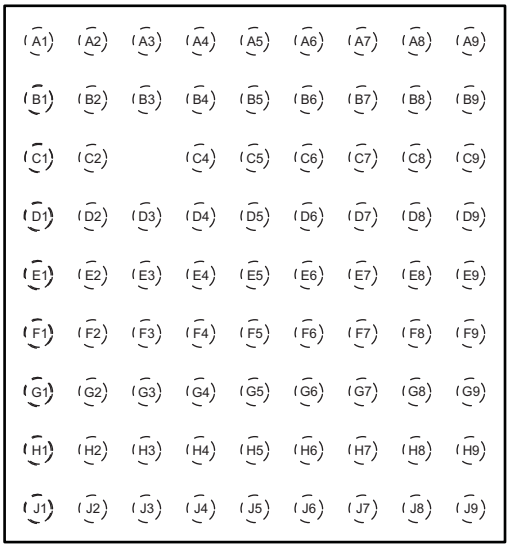
RGC PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

Pin Designation – MSP430F5528IZQE, MSP430F5526IZQE, MSP430F5524IZQE, MSP430F5522IZQE, MSP430F5514IZQE, MSP430F5513IZQE

ZQE PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

Table 2. TERMINAL FUNCTIONS

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.				
	PN	RGC	ZQE		
P6.4/CB4/A4	1	5	C1	I/O	General-purpose digital I/O Comparator_B input CB4 Analog input A4 – ADC (not available on '551x devices)
P6.5/CB5/A5	2	6	D2	I/O	General-purpose digital I/O Comparator_B input CB5 Analog input A5 – ADC (not available on '551x devices)
P6.6/CB6/A6	3	7	D1	I/O	General-purpose digital I/O Comparator_B input CB6 Analog input A6 – ADC (not available on '551x devices)
P6.7/CB7/A7	4	8	D3	I/O	General-purpose digital I/O Comparator_B input CB7 Analog input A7 – ADC (not available on '551x devices)
P7.0/CB8/A12	5	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) Comparator_B input CB8 (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) Analog input A12 – ADC (not available on '551x devices)
P7.1/CB9/A13	6	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) Comparator_B input CB9 (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) Analog input A13 – ADC (not available on '551x devices)
P7.2/CB10/A14	7	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) Comparator_B input CB10 (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) Analog input A14 – ADC (not available on '551x devices)
P7.3/CB11/A15	8	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) Comparator_B input CB11 (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) Analog input A15 – ADC (not available on '551x devices)
P5.0/VREF+/VeREF+	9	9	E1	I/O	General-purpose digital I/O Output of reference voltage to the ADC (not available on '551x devices) Input for an external reference voltage to the ADC (not available on '551x devices)
P5.1/VREF-/VeREF-	10	10	E2	I/O	General-purpose digital I/O Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage (not available on '551x devices)
AVCC1	11	11	F2		Analog power supply
P5.4/XIN	12	12	F1	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P5.5/XOUT	13	13	G1	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS1	14	14	G2		Analog ground supply
P8.0	15	N/A	N/A	I/O	General-purpose digital I/O
P8.1	16	N/A	N/A	I/O	General-purpose digital I/O
P8.2	17	N/A	N/A	I/O	General-purpose digital I/O
DVCC1	18	15	H1		Digital power supply
DVSS1	19	16	J1		Digital ground supply
VCORE[2]	20	17	J2		Regulated core power supply output (internal usage only, no external current loading)

(1) I = input, O = output, N/A = not available
(2) VCORE is for internal usage only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

Table 2. TERMINAL FUNCTIONS (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.				
	PN	RGC	ZQE		
P1.0/TA0CLK/ACLK	21	18	H2	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ; ACLK output (divided by 1, 2, 4, or 8)
P1.1/TA0.0	22	19	H3	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	23	20	J3	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	24	21	G4	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	25	22	H4	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	26	23	J4	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/TA1CLK/CBOUT	27	24	G5	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output
P1.7/TA1.0	28	25	H5	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output
P2.0/TA1.1	29	26	J5	I/O	General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output
P2.1/TA1.2	30	27	G6	I/O	General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output
P2.2/TA2CLK/SMCLK	31	28	J6	I/O	General-purpose digital I/O with port interrupt TA2 clock signal TA2CLK input ; SMCLK output
P2.3/TA2.0	32	29	H6	I/O	General-purpose digital I/O with port interrupt TA2 CCR0 capture: CCI0A input, compare: Out0 output
P2.4/TA2.1	33	30	J7	I/O	General-purpose digital I/O with port interrupt TA2 CCR1 capture: CCI1A input, compare: Out1 output
P2.5/TA2.2	34	31	J8	I/O	General-purpose digital I/O with port interrupt TA2 CCR2 capture: CCI2A input, compare: Out2 output
P2.6/RTCCLK/DMAE0	35	32	J9	I/O	General-purpose digital I/O with port interrupt RTC clock output for calibration DMA external trigger input
P2.7/UCB0STE/UCA0CLK	36	33	H7	I/O	General-purpose digital I/O Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.0/UCB0SIMO/UCB0SDA	37	34	H8	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C data – USCI_B0 I2C mode
P3.1/UCB0SOMI/UCB0SCL	38	35	H9	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I2C clock – USCI_B0 I2C mode
P3.2/UCB0CLK/UCA0STE	39	36	G8	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
P3.3/UCA0TXD/UCA0SIMO	40	37	G9	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode
P3.4/UCA0RXD/UCA0SOMI	41	38	G7	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode

PRODUCT PREVIEW

Table 2. TERMINAL FUNCTIONS (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.				
	PN	RGC	ZQE		
P3.5/TB0.5	42	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) TB0 CCR5 capture: CCI5A input, compare: Out5 output
P3.6/TB0.6	43	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) TB0 CCR6 capture: CCI6A input, compare: Out6 output
P3.7/TB0OUTH/SVMOUT	44	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) Switch all PWM outputs high impedance input – TB0 (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) SVM output (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices)
P4.0/PM_UCB1STE/ PM_UCA1CLK	45	41	E8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable – USCI_B1 SPI mode Default mapping: Clock signal input – USCI_A1 SPI slave mode Default mapping: Clock signal output – USCI_A1 SPI master mode
P4.1/PM_UCB1SIMO/ PM_UCB1SDA	46	42	E7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B1 SPI mode Default mapping: I2C data – USCI_B1 I2C mode
P4.2/PM_UCB1SOMI/ PM_UCB1SCL	47	43	D9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B1 SPI mode Default mapping: I2C clock – USCI_B1 I2C mode
P4.3/PM_UCB1CLK/ PM_UCA1STE	48	44	D8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B1 SPI slave mode Default mapping: Clock signal output – USCI_B1 SPI master mode Default mapping: Slave transmit enable – USCI_A1 SPI mode
DVSS2	49	39	F9		Digital ground supply
DVCC2	50	40	E9		Digital power supply
P4.4/PM_UCA1TXD/ PM_UCA1SIMO	51	45	D7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode
P4.5/PM_UCA1RXD/ PM_UCA1SOMI	52	46	C9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode
P4.6/PM_NONE	53	47	C8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P4.7/PM_NONE	54	48	C7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P5.6/TB0.0	55	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) TB0 CCR0 capture: CCI0A input, compare: Out0 output (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices)
P5.7/TB0.1	56	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) TB0 CCR1 capture: CCI1A input, compare: Out1 output (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices)
P7.4/TB0.2	57	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) TB0 CCR2 capture: CCI2A input, compare: Out2 output (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices)

Table 2. TERMINAL FUNCTIONS (continued)

TERMINAL				I/O[1]	DESCRIPTION
NAME	NO.				
	PN	RGC	ZQE		
P7.5/TB0.3	58	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) TB0 CCR3 capture: CCI3A input, compare: Out3 output (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices)
P7.6/TB0.4	59	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) TB0 CCR4 capture: CCI4A input, compare: Out4 output (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices)
P7.7/TB0CLK/MCLK	60	N/A	N/A	I/O	General-purpose digital I/O (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) TB0 clock signal TBCLK input (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices) MCLK output (not available on '5528, '5526, '5524, '5522, '5514, '5513 devices)
VSSU	61	49	B8, B9		USB PHY ground supply
PU.0/DP	62	50	A9	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DP
PUR	63	51	B7	O	USB pull-up resistor pin (open drain)
PU.1/DM	64	52	A8	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DM
VBUS	65	53	A7		USB LDO input (connect to USB power source)
VUSB	66	54	A6		USB LDO output
V18	67	55	B6		USB regulated power (internal usage only, no external current loading)
AVSS2	68	56	A5		Analog ground supply
P5.2/XT2IN	69	57	B5	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	70	58	B4	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK	71	59	A4	I	Test mode pin – select digital I/O on JTAG pins Spy-bi-wire input clock
PJ.0/TDO	72	60	C5	I/O	General-purpose digital I/O Test data output port
PJ.1/TDI/TCLK	73	61	C4	I/O	General-purpose digital I/O Test data input or test clock input
PJ.2/TMS	74	62	A3	I/O	General-purpose digital I/O Test mode select
PJ.3/TCK	75	63	B3	I/O	General-purpose digital I/O Test clock
$\overline{\text{RST}}$/NMI/SBWTDIO	76	64	A2	I/O	Reset input active low Non-maskable interrupt input Spy-bi-wire data input/output
P6.0/CB0/A0	77	1	A1	I/O	General-purpose digital I/O Comparator_B input CB0 Analog input A0 – ADC (not available on '551x devices)
P6.1/CB1/A1	78	2	B2	I/O	General-purpose digital I/O Comparator_B input CB1 Analog input A1 – ADC (not available on '551x devices)
P6.2/CB2/A2	79	3	B1	I/O	General-purpose digital I/O Comparator_B input CB2 Analog input A2 – ADC (not available on '551x devices)
P6.3/CB3/A3	80	4	C2	I/O	General-purpose digital I/O Comparator_B input CB3 Analog input A3 – ADC (not available on '551x devices)

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Table 2. TERMINAL FUNCTIONS (continued)

TERMINAL				I/O(1)	DESCRIPTION
NAME	NO.				
	PN	RGC	ZQE		
Reserved	N/A	N/A	(3)		

(3) C6, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6, F7, F8, G3 are reserved and should be connected to ground.

SHORT-FORM DESCRIPTION

CPU

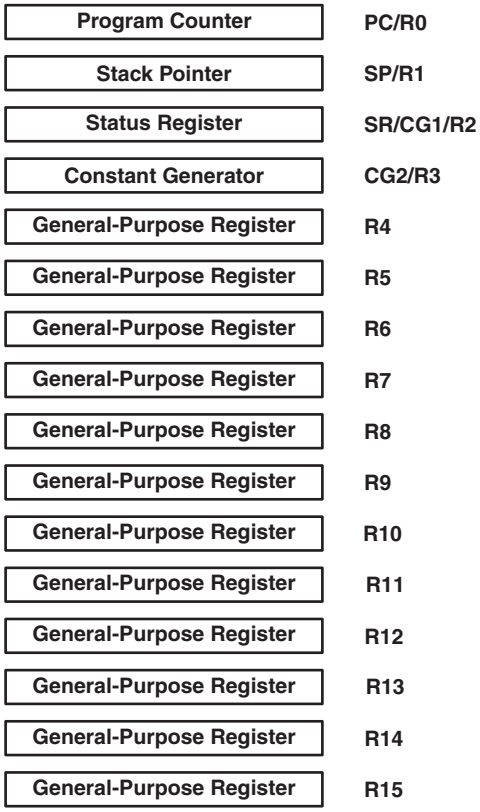
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.



Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; the address modes are listed in Table 4.

Table 3. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 → R5
Single operands, destination only	e.g., CALL R8	PC → (TOS), R8 → PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 4. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	+	+	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	+	+	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	+	+	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	+	+	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	+		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	+		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	+		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source, D = destination

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Operating Modes

The MSP430 has one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 5 (LPM5)
  - Internal regulator disabled
  - No data retention
  - Wakeup from $\overline{\text{RST}}$/NMI, P1, and P2.

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog Timeout, Key Violation Flash Memory Key Violation	WDTIFG, KEYV (SYSRSTIV)(1)(2)	Reset	0FFFEh	63, highest
System NMI PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator Fault Flash Memory Access Violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV)(1)(2)	(Non)maskable	0FFFAh	61
Comp_B	Comparator B interrupt flags (CBIV)(1)(3)	Maskable	0FFF8h	60
TB0	TB0CCR0 CCIFG0 (3)	Maskable	0FFF6h	59
TB0	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV)(1)(3)	Maskable	0FFF4h	58
Watchdog Timer_A Interval Timer Mode	WDTIFG	Maskable	0FFF2h	57
USCI_A0 Receive/Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1)(3)	Maskable	0FFF0h	56
USCI_B0 Receive/Transmit	UCB0RXIFG, UCB0TXIFG (UCAB0IV)(1)(3)	Maskable	0FFEEh	55
ADC12_A	ADC12IFG0 to ADC12IFG15 (ADC12IV)(1)(3)(4)	Maskable	0FFECh	54
TA0	TA0CCR0 CCIFG0(3)	Maskable	0FFEAh	53
TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1)(3)	Maskable	0FFE8h	52
USB_UBM	USB interrupts (USBIV)(1)(3)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1)(3)	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0(3)	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1)(3)	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1)(3)	Maskable	0FFDEh	47
USCI_A1 Receive/Transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV)(1)(3)	Maskable	0FFDCh	46
USCI_B1 Receive/Transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV)(1)(3)	Maskable	0FFDAh	45
TA2	TA2CCR0 CCIFG0(3)	Maskable	0FFD8h	44
TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV)(1)(3)	Maskable	0FFD6h	43
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV)(1)(3)	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1)(3)	Maskable	0FFD2h	41
Reserved	Reserved(5)		0FFD0h	40
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Only on devices with ADC, otherwise reserved.
(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

Memory Organization

Table 6. Memory Organization(1)

		MSP430F5522 MSP430F5521 MSP430F5513	MSP430F5525 MSP430F5524 MSP430F5515 MSP430F5514	MSP430F5527 MSP430F5526 MSP430F5517	MSP430F5529 MSP430F5528 MSP430F5519
Memory (flash) Main: interrupt vector	Total Size	32 KB 00FFFFh–00FF80h	64 KB 00FFFFh–00FF80h	96 KB 00FFFFh–00FF80h	128 KB 00FFFFh–00FF80h
Main: code memory	Bank 3	N/A	N/A	N/A	32 KB 0243FFh–01C400h
	Bank 2	N/A	N/A	32 KB 01C3FFh–014400h	32 KB 01C3FFh–014400h
	Bank 1	15 KB 00FFFFh–00C400h	32 KB 0143FFh–00C400h	32 KB 0143FFh–00C400h	32 KB 0143FFh–00C400h
	Bank 0	17 KB 00C3FFh–008000h	32 KB 00C3FFh–004400h	32 KB 00C3FFh–004400h	32 KB 00C3FFh–004400h
RAM	Sector 3	2 KB(2) 0043FFh–003C00h	N/A	N/A	2 KB 0043FFh–003C00h
	Sector 2	2 KB(3) 003BFFh–003400h	N/A	2 KB 003BFFh–003400h	2 KB 003BFFh–003400h
	Sector 1	2 KB 0033FFh–002C00h	2 KB 0033FFh–002C00h	2 KB 0033FFh–002C00h	2 KB 0033FFh–002C00h
	Sector 0	2 KB 002BFFh–002400h	2 KB 002BFFh–002400h	2 KB 002BFFh–002400h	2 KB 002BFFh–002400h
USB RAM(4)		2 KB 0023FFh–001C00h	2 KB 0023FFh–001C00h	2 KB 0023FFh–001C00h	2 KB 0023FFh–001C00h
Information memory (flash)	Info A	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h
	Info B	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h
	Info C	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h
	Info D	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h
Bootstrap loader (BSL) memory (flash)	BSL 3	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h
	BSL 2	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h
	BSL 1	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h
	BSL 0	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h
Peripherals	Size	4 KB 000FFFh–0h	4 KB 000FFFh–0h	4 KB 000FFFh–0h	4 KB 000FFFh–0h

(1) N/A = Not available.
(2) 'F5522 only.
(3) 'F5522, 'F5521 only.
(4) USB RAM can be used as general purpose RAM when not used for USB operation.

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Memory Programming User's Guide*, literature number SLAU265.

Table 7. BSL Functions

BSL FUNCTION	DEVICE OUTPUT SIGNAL
Data transmit	P1.1
Data receive	P1.2

Flash Memory

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

RAM Memory

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however all data is lost. Features of the RAM memory include:

- RAM memory has n sectors. The size of a sector can be found in the Memory Organization section.
- Each sector 0 to n can be complete disabled, however data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.
- For Devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx Family User's Guide*, literature number SLAU208.

Digital I/O

There are up to eight 8-bit I/O ports implemented: For 80 pin options, P1, P2, P3, P4, P5, P6, and P7 are complete. P8 is reduced to 3-bit I/O. For 64 pin options, P3 and P5 are reduced to 5-bit I/O and 6-bit I/O, respectively. P7 and P8 are completely removed. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM5 wakeup input capability is available for all bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P8) or word-wise in pairs (PA through PD).

Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4.

Table 8. Port Mapping, Mnemonics and Functions

Value	PxMAPy Mnemonic	Input Pin Function	Output Pin Function
0	PM_NONE	None	DVSS
1	PM_CBOUT0	-	Comparator_B output
	PM_TB0CLK	TB0 clock input	
2	PM_ADC12CLK	-	ADC12CLK
	PM_DMAE0	DMAE0 input	
3	PM_SVMOUT	-	SVM output
	PM_TB0OUTH	TB0 high impedance input TB0OUTH	
4	PM_TB0CCR0A	TB0 CCR0 capture input CCI0A	TB0 CCR0 compare output Out0
5	PM_TB0CCR1A	TB0 CCR1 capture input CCI1A	TB0 CCR1 compare output Out1
6	PM_TB0CCR2A	TB0 CCR2 capture input CCI2A	TB0 CCR2 compare output Out2
7	PM_TB0CCR3A	TB0 CCR3 capture input CCI3A	TB0 CCR3 compare output Out3
8	PM_TB0CCR4A	TB0 CCR4 capture input CCI4A	TB0 CCR4 compare output Out4
9	PM_TB0CCR5A	TB0 CCR5 capture input CCI5A	TB0 CCR5 compare output Out5
10	PM_TB0CCR6A	TB0 CCR6 capture input CCI6A	TB0 CCR6 compare output Out6
11	PM_UCA1RXD	USCI_A1 UART RXD (Direction controlled by USCI - input)	
	PM_UCA1SOMI	USCI_A1 SPI slave out master in (direction controlled by USCI)	
12	PM_UCA1TXD	USCI_A1 UART TXD (Direction controlled by USCI - output)	
	PM_UCA1SIMO	USCI_A1 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA1CLK	USCI_A1 clock input/output (direction controlled by USCI)	
	PM_UCB1STE	USCI_B1 SPI slave transmit enable (direction controlled by USCI)	
14	PM_UCB1SOMI	USCI_B1 SPI slave out master in (direction controlled by USCI)	
	PM_UCB1SCL	USCI_B1 I2C clock (open drain and direction controlled by USCI)	
15	PM_UCB1SIMO	USCI_B1 SPI slave in master out (direction controlled by USCI)	
	PM_UCB1SDA	USCI_B1 I2C data (open drain and direction controlled by USCI)	
16	PM_UCB1CLK	USCI_B1 clock input/output (direction controlled by USCI)	
	PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI)	
17	PM_CBOUT1	None	Comparator_B output
18	PM_MCLK	None	MCLK
19 - 30	Reserved	None	DVSS
31 (0FFh)(1)	PM_ANALOG	Disables the output driver as well as the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PMPAP_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored resulting in a read out value of 31.

Table 9. Default Mapping

Pin	PxMAPy Mnemonic	Input Pin Function	Output Pin Function
P4.0/P4MAP0	PM_UCB1STE/PM_UCA1CLK	USCI_B1 SPI slave transmit enable (direction controlled by USCI) USCI_A1 clock input/output (direction controlled by USCI)	
P4.1/P4MAP1	PM_UCB1SIMO/PM_UCB1SDA	USCI_B1 SPI slave in master out (direction controlled by USCI) USCI_B1 I2C data (open drain and direction controlled by USCI)	
P4.2/P4MAP2	PM_UCB1SOMI/PM_UCB1SCL	USCI_B1 SPI slave out master in (direction controlled by USCI) USCI_B1 I2C clock (open drain and direction controlled by USCI)	
P4.3/P4MAP3	PM_UCB1CLK/PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI) USCI_B1 clock input/output (direction controlled by USCI)	
P4.4/P4MAP4	PM_UCA1TXD/PM_UCA1SIMO	USCI_A1 UART TXD (Direction controlled by USCI - output) USCI_A1 SPI slave in master out (direction controlled by USCI)	
P4.5/P4MAP5	PM_UCA1RXD/PM_UCA1SOMI	USCI_A1 UART RXD (Direction controlled by USCI - input) USCI_A1 SPI slave out master in (direction controlled by USCI)	
P4.6/P4MAP6	PM_NONE	None	DVSS
P4.7/P4MAP7	PM_NONE	None	DVSS

Oscillator and System Clock

The clock system in the MSP430F552x and MSP430F551x family of devices is supported by the Unified Clock System (UCS) module that includes support for a 32 kHz watch crystal oscillator (XT1 LF mode - XT1 HF mode not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The UCS module is designed to meet the requirements of both low system cost and low-power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 5 µs. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32 kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

Real-Time Clock (RTC_A)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, boot strap loader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

Table 10. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV , System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		$\overline{\text{RST}}$/NMI (POR)	04h	
		PMMSWBOR (BOR)	06h	
		Wakeup from LPMx.5	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT timeout (PUC)	16h	
		WDT key violation (PUC)	18h	
		KEYV flash key violation (PUC)	1Ah	
		FLL unlock (PUC)	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM key violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
SYSSNIV , System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRIFG	12h	
		Reserved	14h to 1Eh	Lowest

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Table 10. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

The USB timestamp generator also utilizes the DMA trigger assignments described in Table 11.

Table 11. DMA Trigger Assignments(1)

Trigger	Channel		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA2CCR2 CCIFG	TA2CCR2 CCIFG	TA2CCR2 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC12IFGx(2)	ADC12IFGx(2)	ADC12IFGx(2)
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	USB FNRXD	USB FNRXD	USB FNRXD

(1) If a reserved trigger source is selected, no Trigger1 is generated.
(2) Only on devices with ADC. Reserved on devices without ADC.

Table 11. DMA Trigger Assignments (continued)

Trigger	Channel		
	0	1	2
28	USB ready	USB ready	USB ready
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3 pin or 4 pin) or I2C.

The MSP430F55xx series includes two complete USCI modules (n = 0, 1).

TA0

TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. TA0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC/ZQE	PN						RGC/ZQE	PN
18/H2-P1.0	21-P1.0	TA0CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
18/H2-P1.0	21-P1.0	TA0CLK	$\overline{\text{TACLK}}$					
19/H3-P1.1	22-P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	19/H3-P1.1	22-P1.1
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
20/J3-P1.2	23-P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	20/J3-P1.2	23-P1.2
		CBOUT (internal)	CCI1B				ADC12 (internal)(1) ADC12SHSx = {1}	ADC12 (internal)(1) ADC12SHSx = {1}
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
21/G4-P1.3	24-P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	21/G4-P1.3	24-P1.3
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
22/H4-P1.4	25-P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	22/H4-P1.4	25-P1.4
		DV_{SS}	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
23/J4-P1.5	26-P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	23/J4-P1.5	26-P1.5
		DV_{SS}	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

(1) Only on devices with ADC.

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TA1

TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 13. TA1 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC/ZQE	PN						RGC/ZQE	PN
24/G5-P1.6	27-P1.6	TA1CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
24/G5-P1.6	27-P1.6	TA1CLK	$\overline{\text{TACLK}}$					
25/H5-P1.7	28-P1.7	TA1.0	CCI0A	CCR0	TA0	TA1.0	25/H5-P1.7	28-P1.7
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
26/J5-P2.0	29-P2.0	TA1.1	CCI1A	CCR1	TA1	TA1.1	26/J5-P2.0	29-P2.0
		CBOUT (internal)	CCI1B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
27/G6-P2.1	30-P2.1	TA1.2	CCI2A	CCR2	TA2	TA1.2	27/G6-P2.1	30-P2.1
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

TA2

TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 14. TA2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC/ZQE	PN						RGC/ZQE	PN
28/J6-P2.2	31-P2.2	TA2CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
28/J6-P2.2	31-P2.2	TA2CLK	$\overline{\text{TACLK}}$					
29/H6-P2.3	32-P2.3	TA2.0	CCI0A	CCR0	TA0	TA2.0	29/H6-P2.3	32-P2.3
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
30/J7-P2.4	33-P2.4	TA2.1	CCI1A	CCR1	TA1	TA2.1	30/J7-P2.4	33-P2.4
		CBOUT (internal)	CCI1B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
31/J8-P2.5	34-P2.5	TA2.2	CCI2A	CCR2	TA2	TA2.2	31/J8-P2.5	34-P2.5
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

TB0

TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 15. TB0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC/ZQE[1]	PN						RGC/ZQE[1]	PN
	60-P7.7	TB0CLK	TBCLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
	60-P7.7	TB0CLK	$\overline{\text{TBCLK}}$					
	55-P5.6	TB0.0	CCI0A	CCR0	TB0	TB0.0		55-P5.6
	55-P5.6	TB0.0	CCI0B				ADC12 (internal)[2] ADC12SHSx = {2}	ADC12 (internal)[2] ADC12SHSx = {2}
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	56-P5.7	TB0.1	CCI1A	CCR1	TB1	TB0.1		56-P5.7
		CBOUT (internal)	CCI1B				ADC12 (internal) ADC12SHSx = {3}	ADC12 (internal) ADC12SHSx = {3}
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	57-P7.4	TB0.2	CCI2A	CCR2	TB2	TB0.2		57-P7.4
	57-P7.4	TB0.2	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	58-P7.5	TB0.3	CCI3A	CCR3	TB3	TB0.3		58-P7.5
	58-P7.5	TB0.3	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	59-P7.6	TB0.4	CCI4A	CCR4	TB4	TB0.4		59-P7.6
	59-P7.6	TB0.4	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	42-P3.5	TB0.5	CCI5A	CCR5	TB5	TB0.5		42-P3.5
	42-P3.5	TB0.5	CCI5B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	43-P3.6	TB0.6	CCI6A	CCR6	TB6	TB0.6		43-P3.6
		ACLK (internal)	CCI6B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

(1) Timer functions selectable via the port mapping controller.
(2) Only on devices with ADC.

Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

ADC12_A

The ADC12_A module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

REF Voltage Reference

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

USB Universal Serial Bus

The USB module is a fully integrated USB interface that is compliant with the USB 2.0 specification. The module supports full-speed operation of control, interrupt, and bulk transfers. The module includes an integrated LDO, PHY, and PLL. The PLL is highly-flexible and can support a wide range of input clock frequencies. USB RAM, when not used for USB communication, can be used by the system.

Embedded Emulation Module (EEM)

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The L version of the EEM implemented on all devices has the following features:

- Eight hardware triggers/breakpoints on memory access
- Two hardware trigger/breakpoint on CPU register write access
- Up to ten hardware triggers can be combined to form complex triggers/breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

Peripheral File Map

Table 16. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (refer to Table 17)	0100h	000h - 01Fh
PMM (refer to Table 18)	0120h	000h - 00Fh
Flash Control (refer to Table 19)	0140h	000h - 00Fh
CRC16 (refer to Table 20)	0150h	000h - 007h
RAM Control (refer to Table 21)	0158h	000h - 001h
Watchdog (refer to Table 22)	015Ch	000h - 001h
UCS (refer to Table 23)	0160h	000h - 01Fh
SYS (refer to Table 24)	0180h	000h - 01Fh
Shared Reference (refer to Table 25)	01B0h	000h - 001h
Port Mapping Control (refer to Table 26)	01C0h	000h - 002h
Port Mapping Port P4 (refer to Table 26)	01E0h	000h - 007h
Port P1/P2 (refer to Table 27)	0200h	000h - 01Fh
Port P3/P4 (refer to Table 28)	0220h	000h - 00Bh
Port P5/P6 (refer to Table 29)	0240h	000h - 00Bh
Port P7/P8 (refer to Table 30)	0260h	000h - 00Bh
Port PJ (refer to Table 31)	0320h	000h - 01Fh
TA0 (refer to Table 32)	0340h	000h - 02Eh
TA1 (refer to Table 33)	0380h	000h - 02Eh
TB0 (refer to Table 34)	03C0h	000h - 02Eh
TA2 (refer to Table 35)	0400h	000h - 02Eh
Real Timer Clock (RTC_A) (refer to Table 36)	04A0h	000h - 01Bh
32-bit Hardware Multiplier (refer to Table 37)	04C0h	000h - 02Fh
DMA General Control (refer to Table 38)	0500h	000h - 00Fh
DMA Channel 0 (refer to Table 38)	0510h	000h - 00Ah
DMA Channel 1 (refer to Table 38)	0520h	000h - 00Ah
DMA Channel 2 (refer to Table 38)	0530h	000h - 00Ah
USCI_A0 (refer to Table 39)	05C0h	000h - 01Fh
USCI_B0 (refer to Table 40)	05E0h	000h - 01Fh
USCI_A1 (refer to Table 41)	0600h	000h - 01Fh
USCI_B1 (refer to Table 42)	0620h	000h - 01Fh
ADC12_A (refer to Table 43)	0700h	000h - 03Eh
Comparator_B (refer to Table 44)	08C0h	000h - 00Fh
USB configuration (refer to Table 45)	0900h	000h - 014h
USB control (refer to Table 46)	0920h	000h - 01Fh

Table 17. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 18. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high side control	SVSMHCTL	04h
SVS low side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh

Table 19. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 20. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC result	CRC16INIRES	04h

Table 21. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 22. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 23. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 24. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootstrap loader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 25. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 26. Port Mapping Registers (Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping password register	PMAPPWD	00h
Port mapping control register	PMAPCTL	02h
Port P4.0 mapping register	P4MAP0	00h
Port P4.1 mapping register	P4MAP1	01h
Port P4.2 mapping register	P4MAP2	02h
Port P4.3 mapping register	P4MAP3	03h
Port P4.4 mapping register	P4MAP4	04h
Port P4.5 mapping register	P4MAP5	05h
Port P4.6 mapping register	P4MAP6	06h
Port P4.7 mapping register	P4MAP7	07h

Table 27. Port P1/P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h

Table 27. Port P1/P2 Registers (Base Address: 0200h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 28. Port P3/P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

Table 29. Port P5/P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup/pulldown enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pullup/pulldown enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 30. Port P7/P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 pullup/pulldown enable	P7REN	06h
Port P7 drive strength	P7DS	08h
Port P7 selection	P7SEL	0Ah
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h

Table 30. Port P7/P8 Registers (Base Address: 0260h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P8 direction	P8DIR	05h
Port P8 pullup/pulldown enable	P8REN	07h
Port P8 drive strength	P8DS	09h
Port P8 selection	P8SEL	0Bh

Table 31. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 32. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
Capture/compare register 3	TA0CCR3	18h
Capture/compare register 4	TA0CCR4	1Ah
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 33. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 34. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 register	TB0R	10h
Capture/compare register 0	TB0CCR0	12h
Capture/compare register 1	TB0CCR1	14h
Capture/compare register 2	TB0CCR2	16h
Capture/compare register 3	TB0CCR3	18h
Capture/compare register 4	TB0CCR4	1Ah
Capture/compare register 5	TB0CCR5	1Ch
Capture/compare register 6	TB0CCR6	1Eh
TB0 expansion register 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 35. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter register	TA2R	10h
Capture/compare register 0	TA2CCR0	12h
Capture/compare register 1	TA2CCR1	14h
Capture/compare register 2	TA2CCR2	16h
TA2 expansion register 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 36. Real Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds/counter register 1	RTCSEC/RTCNT1	10h
RTC minutes/counter register 2	RTCMIN/RTCNT2	11h
RTC hours/counter register 3	RTCHOUR/RTCNT3	12h
RTC day of week/counter register 4	RTCDOW/RTCNT4	13h

Table 36. Real Time Clock Registers (Base Address: 04A0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

Table 37. 32-bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

Table 38. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h

Table 38. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Ah

Table 39. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 0	UCA0CTL0	00h
USCI control 1	UCA0CTL1	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 40. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 0	UCB0CTL0	00h
USCI synchronous control 1	UCB0CTL1	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI I2C interrupt enable	UCB0I2CIE	08h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch

Table 40. USCI_B0 Registers (Base Address: 05E0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 41. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 0	UCA1CTL0	00h
USCI control 1	UCA1CTL1	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

Table 42. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 0	UCB1CTL0	00h
USCI synchronous control 1	UCB1CTL1	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI I2C interrupt enable	UCB1I2CIE	08h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

Table 43. ADC12_A Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Control register 0	ADC12CTL0	00h
Control register 1	ADC12CTL1	02h
Control register 2	ADC12CTL2	04h
Interrupt-flag register	ADC12IFG	0Ah
Interrupt-enable register	ADC12IE	0Ch
Interrupt-vector-word register	ADC12IV	0Eh
ADC memory-control register 0	ADC12MCTL0	10h
ADC memory-control register 1	ADC12MCTL1	11h
ADC memory-control register 2	ADC12MCTL2	12h

Table 43. ADC12_A Registers (Base Address: 0700h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC memory-control register 3	ADC12MCTL3	13h
ADC memory-control register 4	ADC12MCTL4	14h
ADC memory-control register 5	ADC12MCTL5	15h
ADC memory-control register 6	ADC12MCTL6	16h
ADC memory-control register 7	ADC12MCTL7	17h
ADC memory-control register 8	ADC12MCTL8	18h
ADC memory-control register 9	ADC12MCTL9	19h
ADC memory-control register 10	ADC12MCTL10	1Ah
ADC memory-control register 11	ADC12MCTL11	1Bh
ADC memory-control register 12	ADC12MCTL12	1Ch
ADC memory-control register 13	ADC12MCTL13	1Dh
ADC memory-control register 14	ADC12MCTL14	1Eh
ADC memory-control register 15	ADC12MCTL15	1Fh
Conversion memory 0	ADC12MEM0	20h
Conversion memory 1	ADC12MEM1	22h
Conversion memory 2	ADC12MEM2	24h
Conversion memory 3	ADC12MEM3	26h
Conversion memory 4	ADC12MEM4	28h
Conversion memory 5	ADC12MEM5	2Ah
Conversion memory 6	ADC12MEM6	2Ch
Conversion memory 7	ADC12MEM7	2Eh
Conversion memory 8	ADC12MEM8	30h
Conversion memory 9	ADC12MEM9	32h
Conversion memory 10	ADC12MEM10	34h
Conversion memory 11	ADC12MEM11	36h
Conversion memory 12	ADC12MEM12	38h
Conversion memory 13	ADC12MEM13	3Ah
Conversion memory 14	ADC12MEM14	3Ch
Conversion memory 15	ADC12MEM15	3Eh

Table 44. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control register 0	CBCTL0	00h
Comp_B control register 1	CBCTL1	02h
Comp_B control register 2	CBCTL2	04h
Comp_B control register 3	CBCTL3	06h
Comp_B interrupt register	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

Table 45. USB Configuration Registers (Base Address: 0900h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USB key/ID	USBKEYID	00h
USB module configuration	USBCNF	02h
USB PHY control	USBPHYCTL	04h
USB power control	USBPWRCTL	08h
USB power voltage setting	USBPWRVSR	0Ah
USB PLL control	USBPLLCTL	10h

Table 45. USB Configuration Registers (Base Address: 0900h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
USB PLL divider	USBPLLDIV	12h
USB PLL interrupts	USBPLLIR	14h

Table 46. USB Control Registers (Base Address: 0920h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Input endpoint#0 configuration	IEPCNF_0	00h
Input endpoint #0 byte count	IEPCNT_0	01h
Output endpoint#0 configuration	OEPCNF_0	02h
Output endpoint #0 byte count	OEPCNT_0	03h
Input endpoint interrupt enables	IEPIE	0Eh
Output endpoint interrupt enables	OEPIE	0Fh
Input endpoint interrupt flags	IEPIFG	10h
Output endpoint interrupt flags	OEPIFG	11h
USB interrupt vector	USBIV	12h
USB maintenance	MAINT	16h
Time stamp	TSREG	18h
USB frame number	USBFN	1Ah
USB control	USBCTL	1Ch
USB interrupt enables	USBIE	1Dh
USB interrupt flags	USBIFG	1Eh
Function address	FUNADR	1Fh

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

Voltage applied at V_{CC} to V_{SS}	–0.3 V to 4.1 V
Voltage applied to any pin (excluding VCORE, VBUS, V18)(2)	–0.3 V to V_{CC} + 0.3 V
Diode current at any device pin	±2 mA
Storage temperature range, T_{stg}(3)	–55°C to 105°C

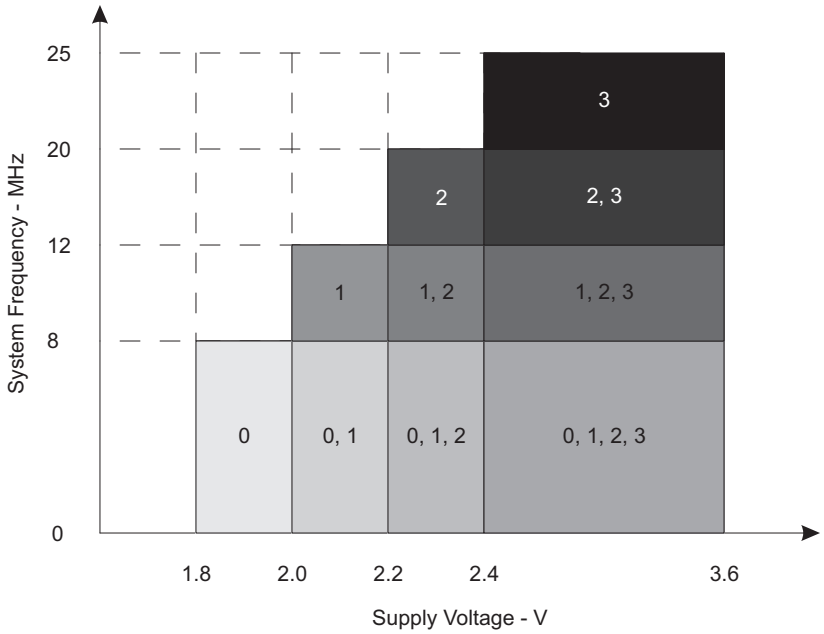
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. VCORE is for internal device usage only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming(AV_{CC} = $DV_{CC1/2/3/4}$ = DV_{CC})(1)	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	V
		PMMCOREVx = 0, 1, 2	2.2		3.6	V
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	V
AV_{CC}	(AV_{CC} = $DV_{CC1/2/3/4}$ = DV_{CC})(1)	Reduced analog performance	1.8		3.6	V
		Full analog performance	2.2		3.6	V
V_{SS}	Supply voltage (AV_{SS} = $DV_{SS1/2/3/4}$ = DV_{SS})			0		V
T_A	Operating free-air temperature	I version	–40		85	°C
T_J	Maximum junction temperature				95	°C
θ_{JA}	Thermal resistance of package	PN package		TBD		°C/W
		RGC package		TBD		
		ZQE package		TBD		
C_{VCORE}	Capacitor at VCORE			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(2) (see Figure 1)	PMMCOREVx = 0 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition)	0		8.0	MHz
		PMMCOREVx = 1 2.0 V ≤ V_{CC} ≤ 3.6 V	0		12.0	
		PMMCOREVx = 2 2.2 V ≤ V_{CC} ≤ 3.6 V	0		20.0	
		PMMCOREVx = 3 2.4 V ≤ V_{CC} ≤ 3.6 V	0		25.0	
f_{SYSTEM_USB}	Minimum processor frequency for USB operation		1.5			MHz
USB_wait	Wait state cycles during USB operation			16		cycles

(1) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
(2) Modules may have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.

PRODUCT PREVIEW



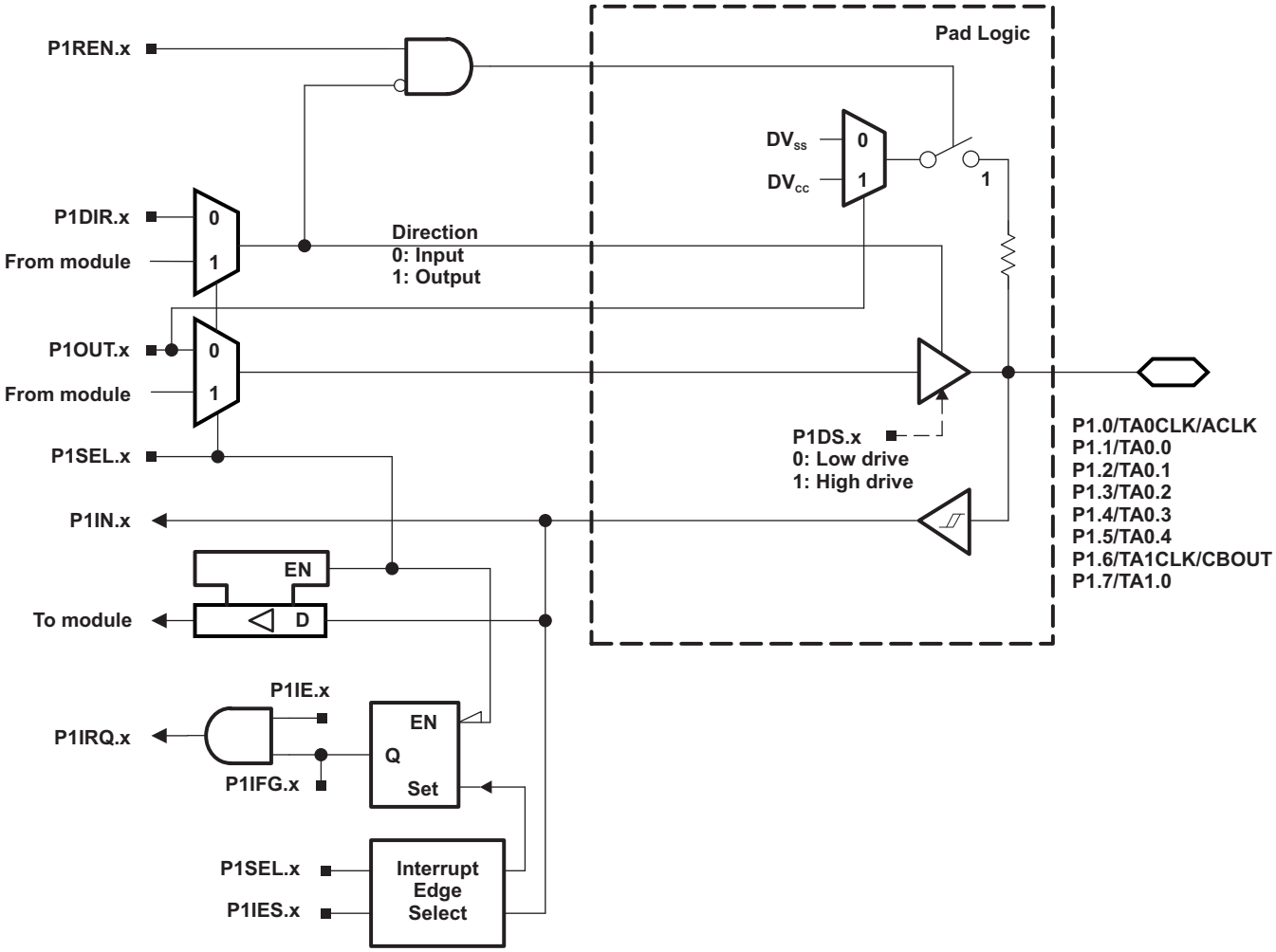
The numbers within the fields denote the supported PMMCOREVx settings.

Figure 1. Maximum System Frequency

PRODUCT PREVIEW

INPUT/OUTPUT SCHEMATICS

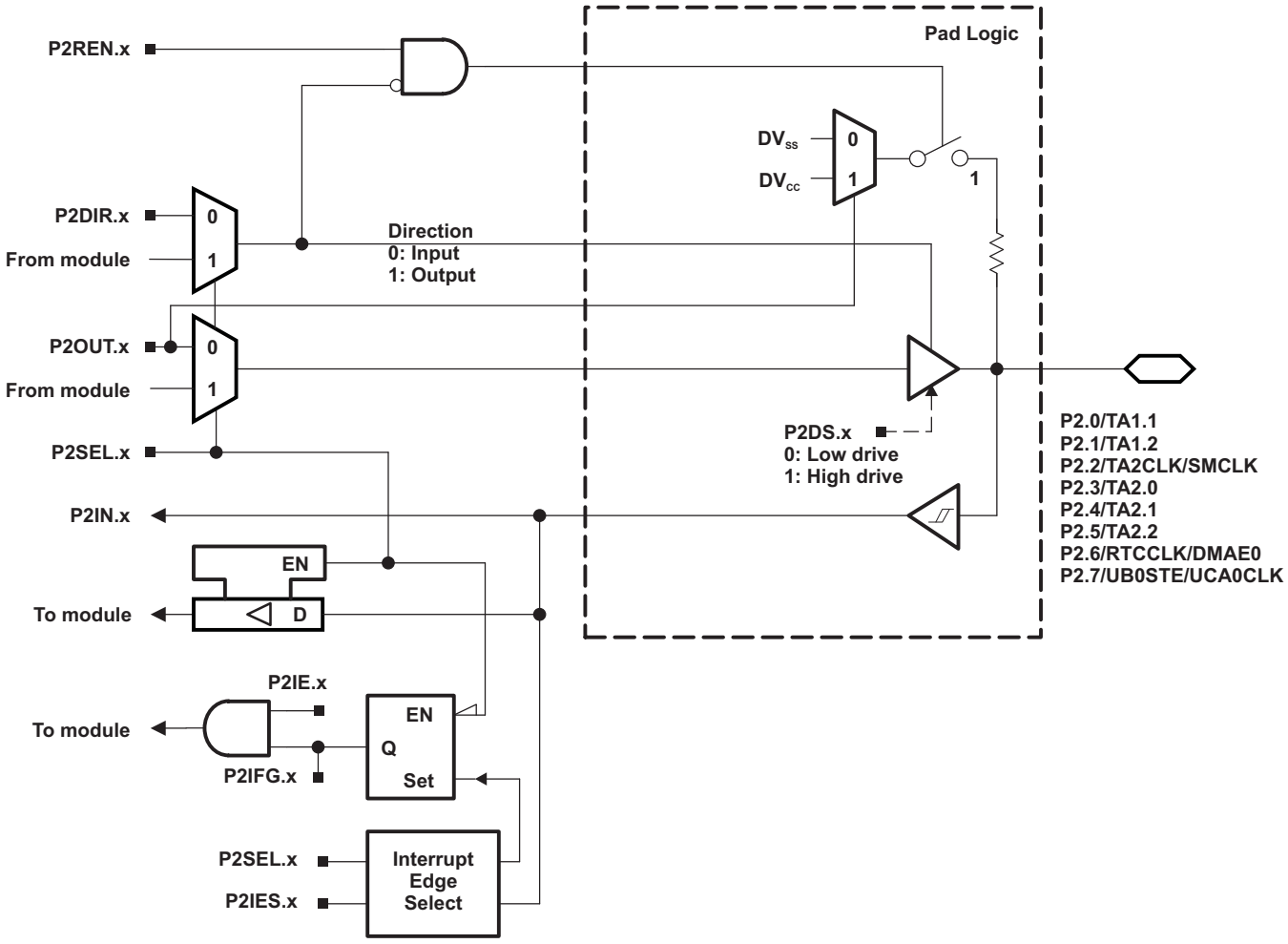
Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger



Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/TA1CLK/CBOUT	6	P1.6 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		CBOUT comparator B	1	1
P1.7/TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1

Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger



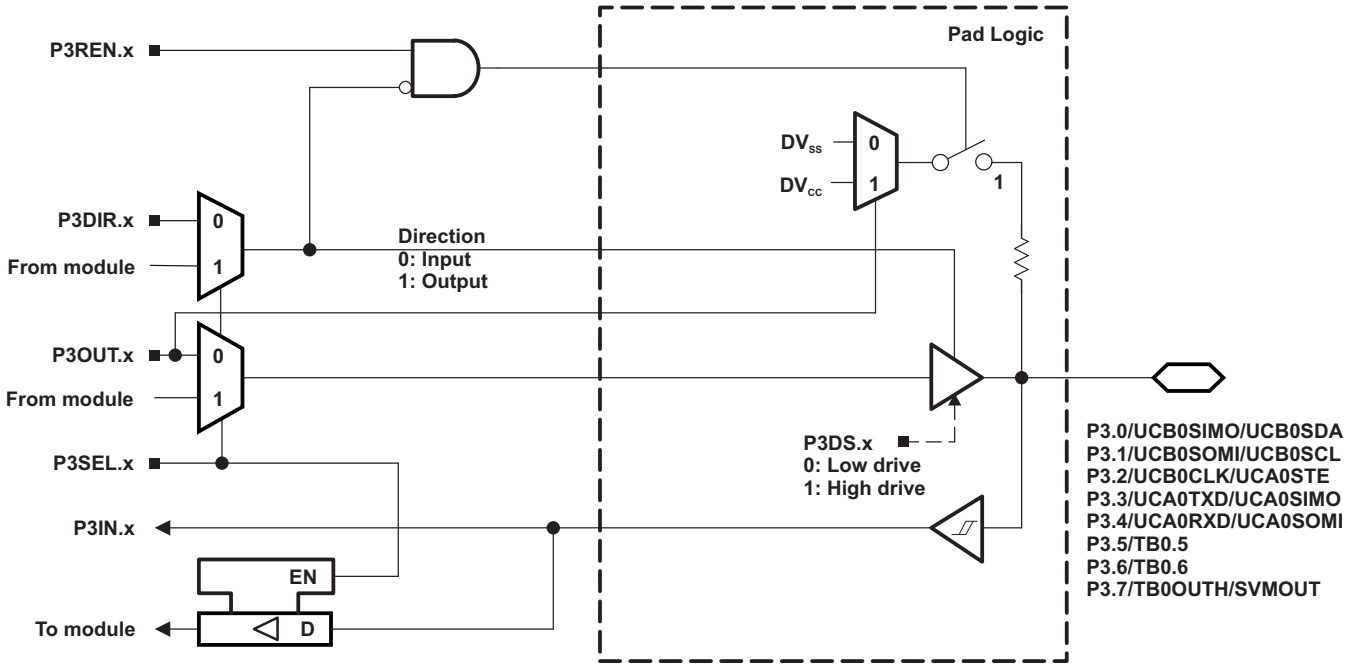
PRODUCT PREVIEW

Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)	
			P2DIR.x	P2SEL.x
P2.0/TA1.1	0	P2.0 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	1
P2.1/TA1.2	1	P2.1 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	1
P2.2/TA2CLK/SMCLK	2	P2.2 (I/O)	I: 0; O: 1	0
		TA2CLK	0	1
		SMCLK	1	1
P2.3/TA2.0	3	P2.3 (I/O)	I: 0; O: 1	0
		TA2.CCI0A	0	1
		TA2.0	1	1
P2.4/TA2.1	4	P2.4 (I/O)	I: 0; O: 1	0
		TA2.CCI1A	0	1
		TA2.1	1	1
P2.5/TA2.2	5	P2.5 (I/O)	I: 0; O: 1	0
		TA2.CCI2A	0	1
		TA2.2	1	1
P2.6/RTCCLK/DMAE0	6	P2.6 (I/O)	I: 0; O: 1	0
		DMAE0	0	1
		RTCCLK	1	1
P2.7/UCB0STE/UCA0CLK	7	P2.7 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK(2)(3)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI A0/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger

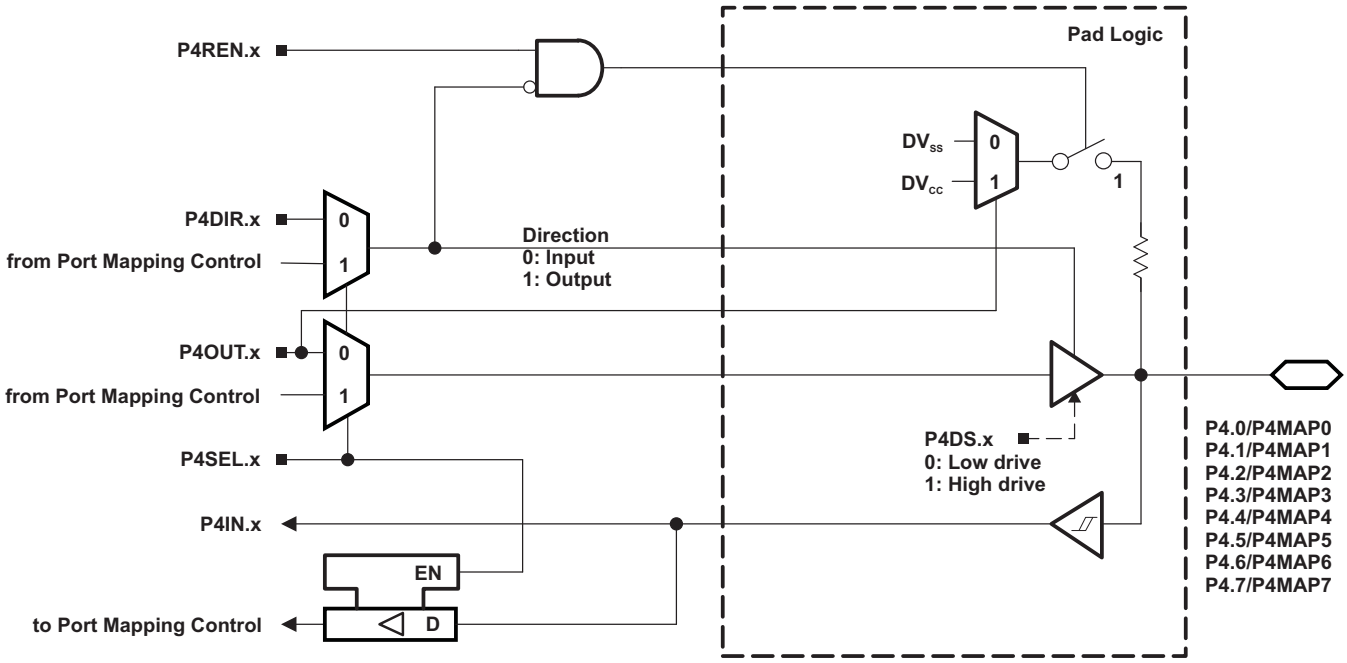


Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]	
			P3DIR.x	P3SEL.x
P3.0/UCB0SIMO/UCB0SDA	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA[2][3]	X	1
P3.1/UCB0SOMI/UCB0SCL	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL[2][3]	X	1
P3.2/UCB0CLK/UCA0STE	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE[2][4]	X	1
P3.3/UCA0TXD/UCA0SIMO	3	P3.3 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO[2]	X	1
P3.4/UCA0RXD/UCA0SOMI	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI[2]	X	1
P3.5/TB0.5[5]	5	P3.5 (I/O)	I: 0; O: 1	0
		TB0.CCI5A	0	1
		TB0.5	1	1
P3.6/TB0.6[5]	6	P3.6 (I/O)	I: 0; O: 1	0
		TB0.CCI6A	0	1
		TB0.6	1	1
P3.7/TB0OUTH/SVMOUT[5]	7	P3.7 (I/O)	I: 0; O: 1	0
		TB0OUTH	0	1
		SVMOUT	1	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI A0/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(5) 'F5529, 'F5527, 'F5525, 'F5521, 'F5519, 'F5517, 'F5515 devices only.

Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger

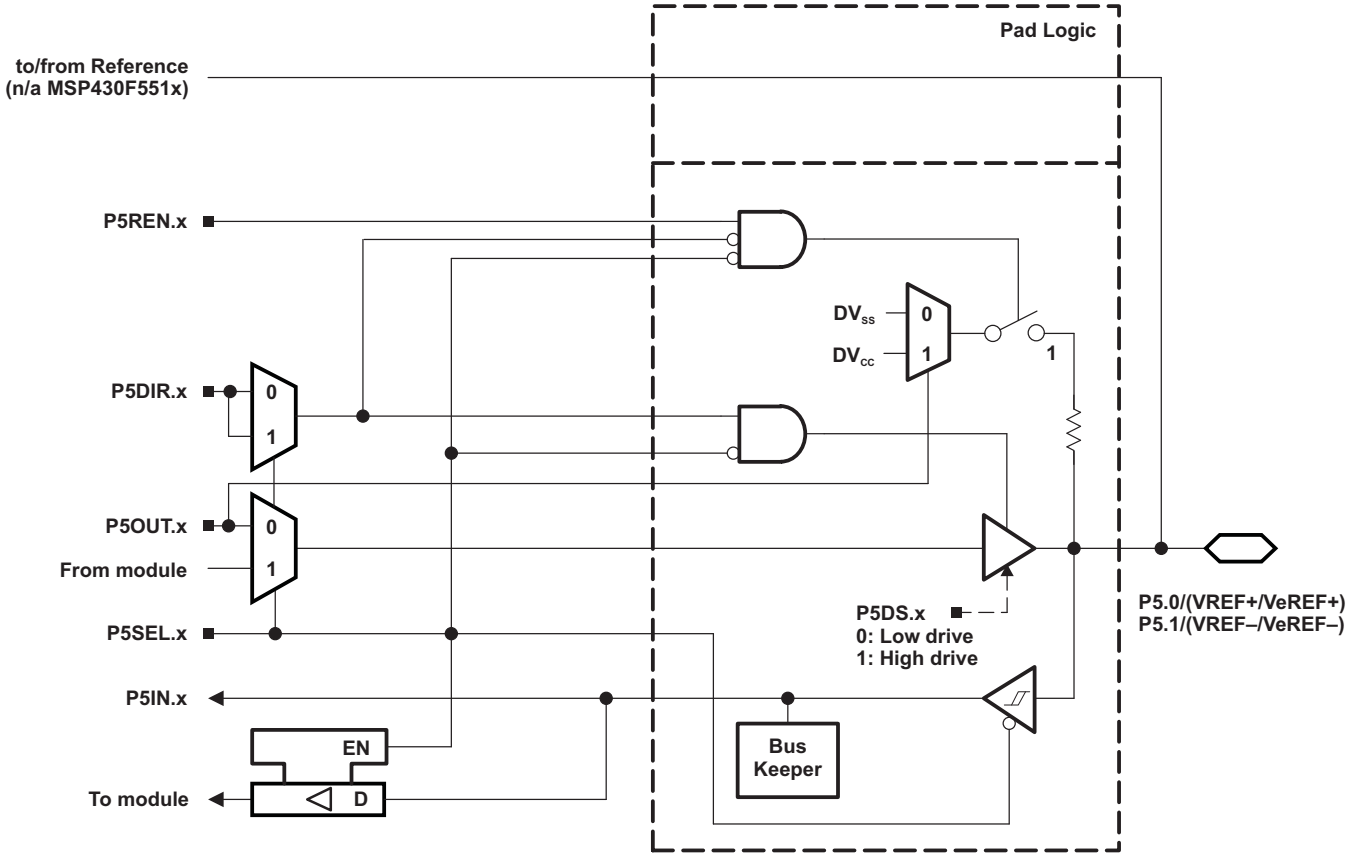


Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS		
			P4DIR.x(1)	P4SEL.x	P4MAPx
P4.0/P4MAP0	0	P4.0 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.1/P4MAP1	1	P4.1 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.2/P4MAP2	2	P4.2 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.3/P4MAP3	3	P4.3 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.4/P4MAP4	4	P4.4 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.5/P4MAP5	5	P4.5 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.6/P4MAP6	6	P4.6 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.7/P4MAP7	7	P4.7 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30

(1) The direction of some mapped secondary functions are controlled directly by the module. Please refer to Table 8 for specific direction control information of mapped secondary functions.

Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger

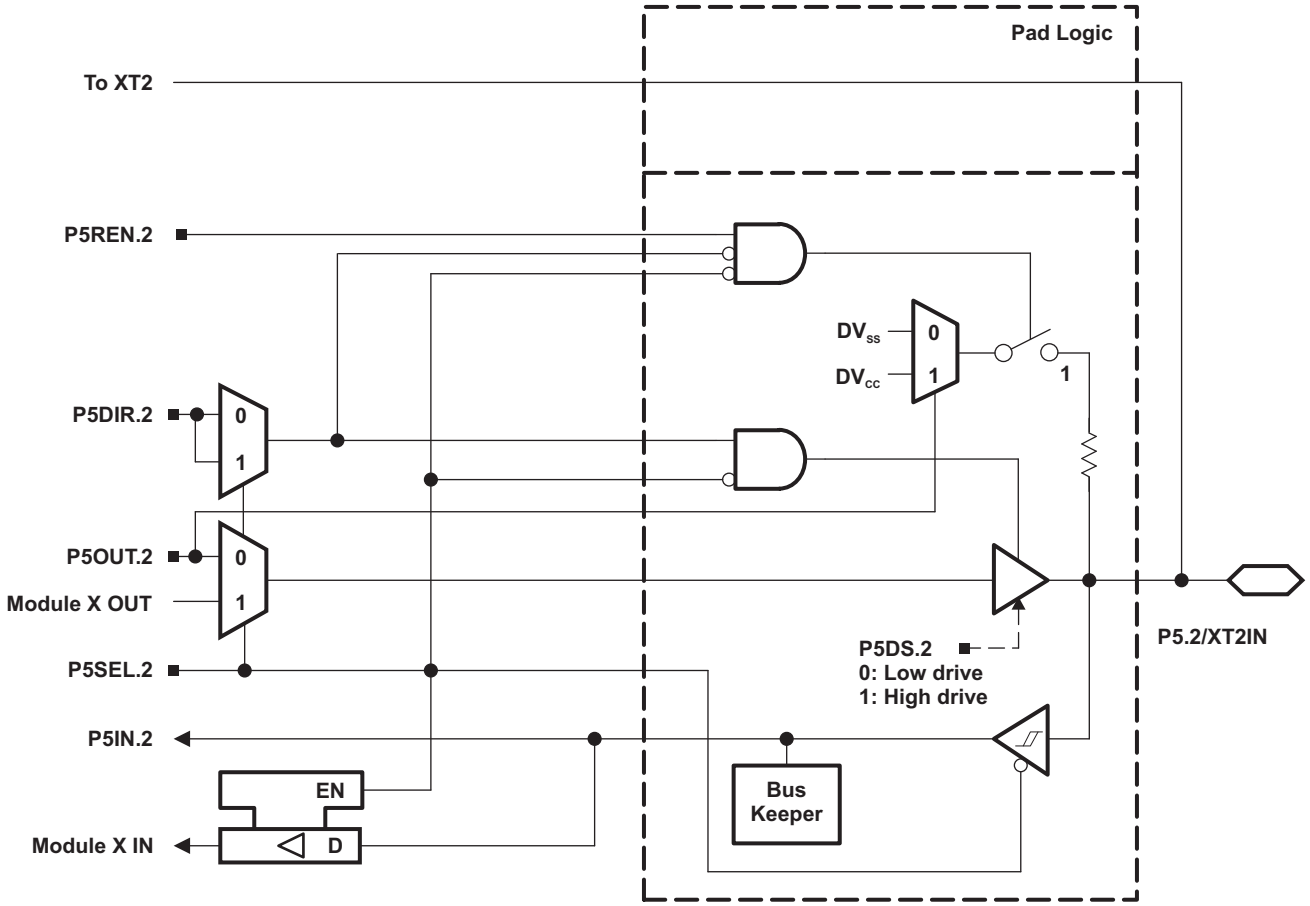


Port P5 (P5.0 and P5.1) Pin Functions

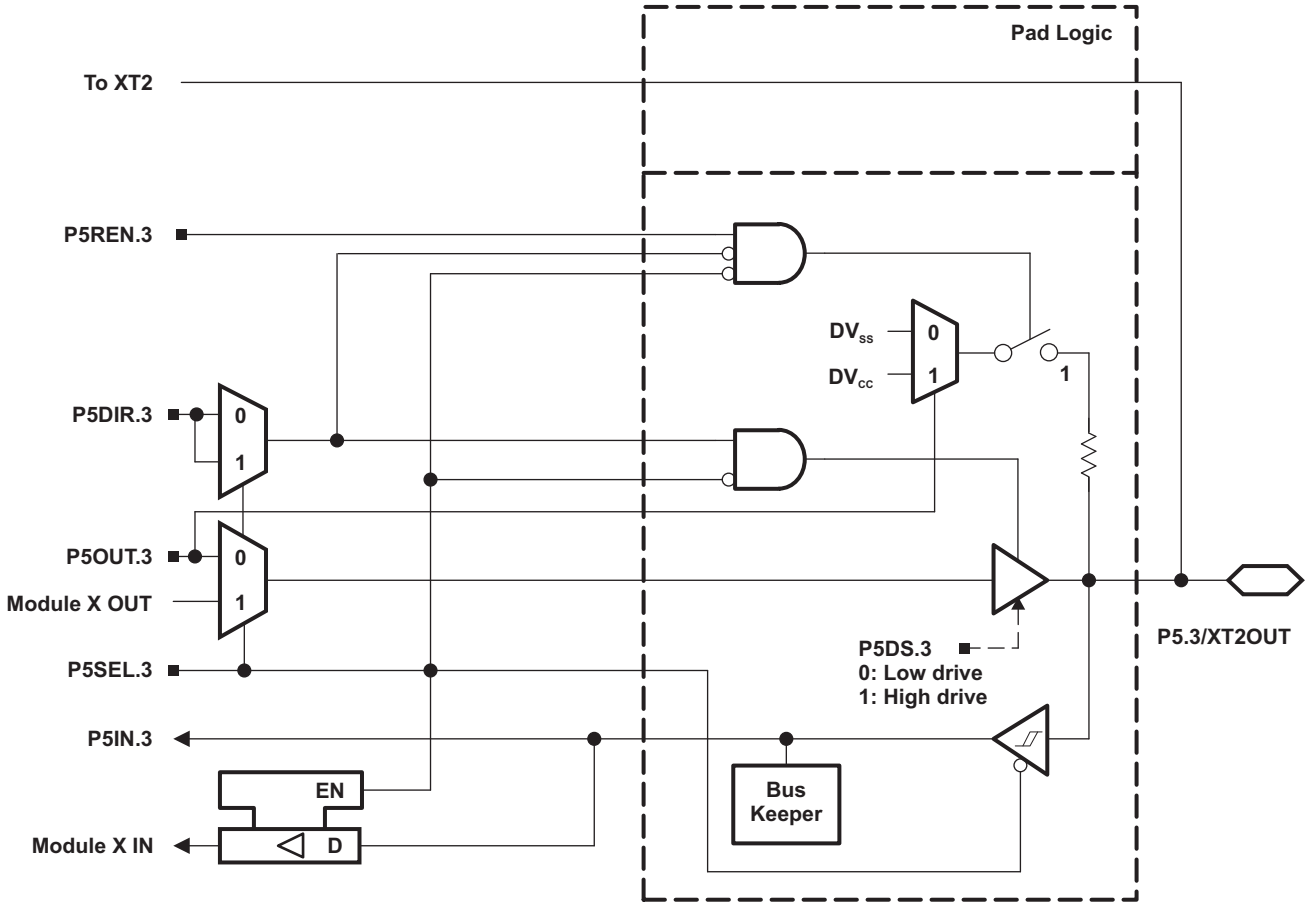
PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P5DIR.x	P5SEL.x	REFOUT
P5.0/VREF+/VeREF+(2)	0	P5.0 (I/O)(3)	I: 0; O: 1	0	X
		VeREF+(4)	X	1	0
		VREF+(5)	X	1	1
P5.1/VREF–/VeREF–(6)	1	P5.1 (I/O)(3)	I: 0; O: 1	0	X
		VeREF–(7)	X	1	0
		VREF–(8)	X	1	1

(1) X = Don't care
(2) VREF+/VeREF+ available on MSP430F552x devices only.
(3) Default condition
(4) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A when available.
(5) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The VREF+ reference is available at the pin.
(6) VREF-/VeREF- available on MSP430F552x devices only.
(7) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A when available.
(8) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The VREF– reference is available at the pin.

Port P5, P5.2, Input/Output With Schmitt Trigger



Port P5, P5.3, Input/Output With Schmitt Trigger

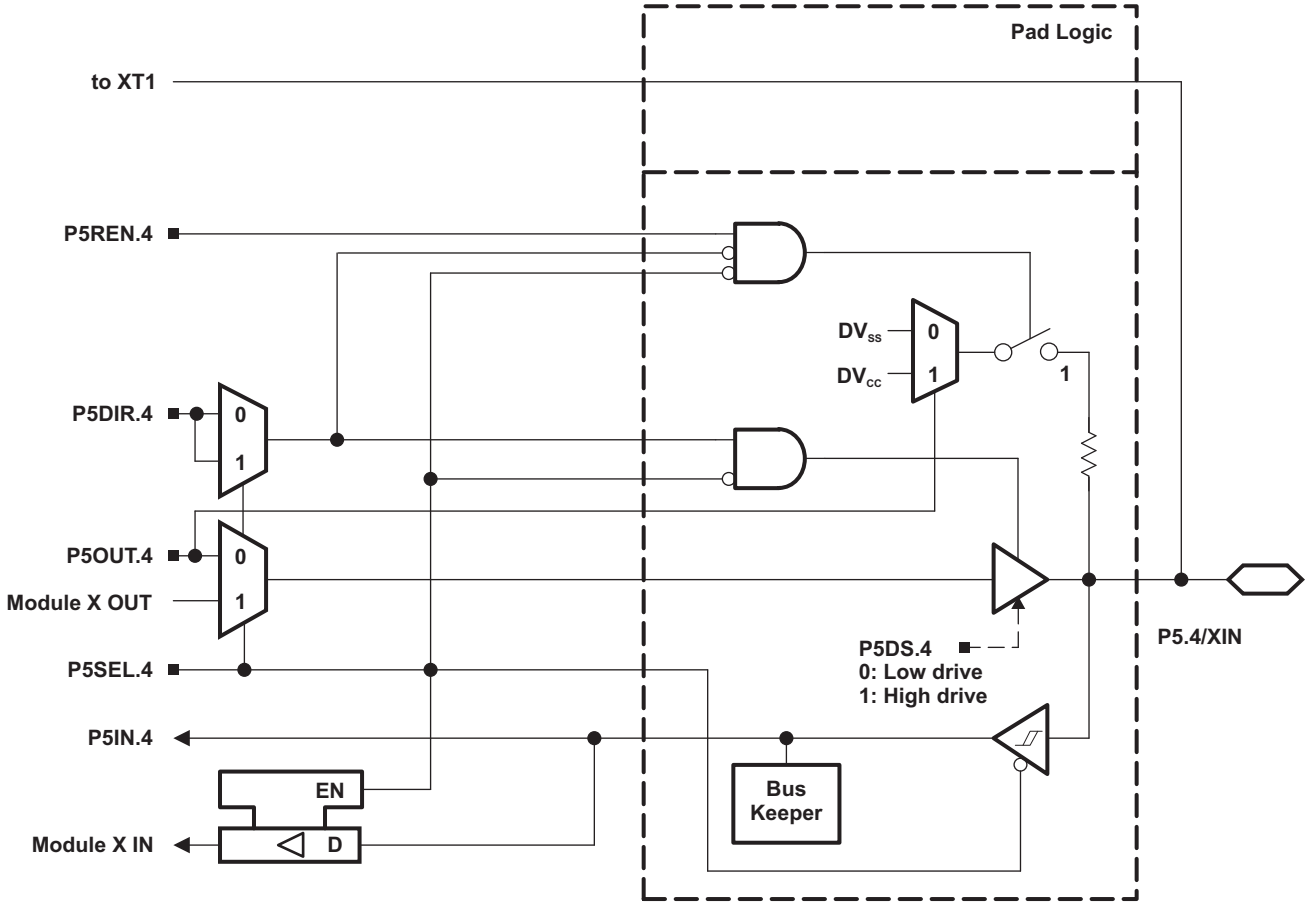


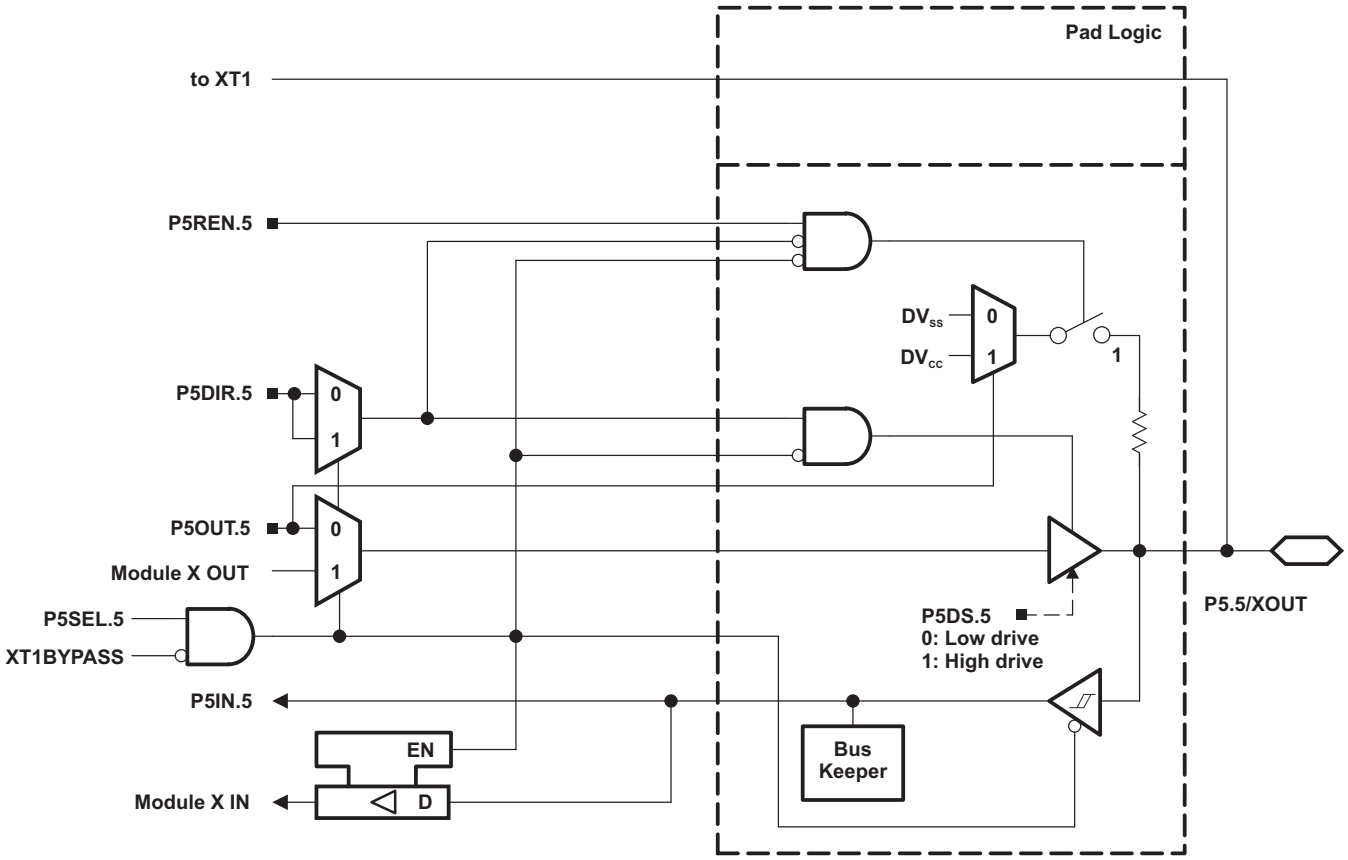
Port P5 (P5.2, P5.3) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode(2)	X	1	X	0
		XT2IN bypass mode(2)	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	X	X
		XT2OUT crystal mode(3)	X	1	X	0
		P5.3 (I/O)(3)	X	1	X	1

(1) X = Don't care
(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

Port P5, P5.4 and P5.5 Input/Output With Schmitt Trigger





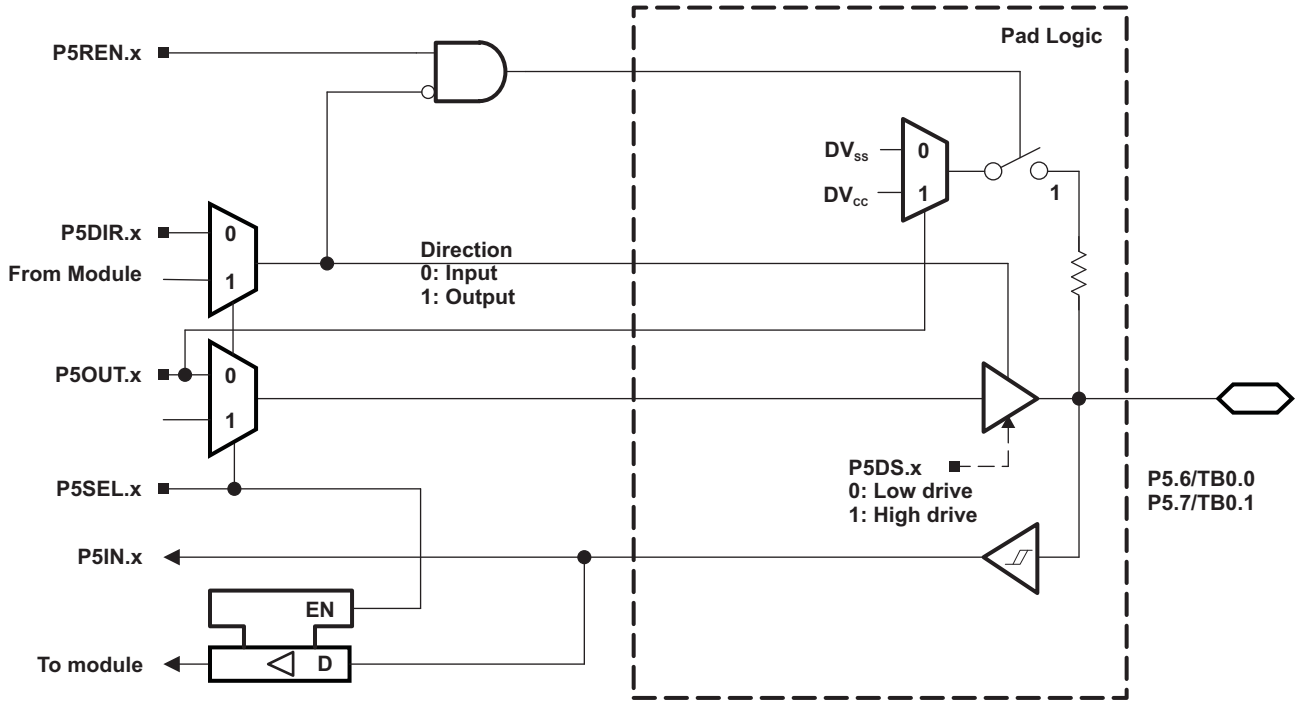
Port P5 (P5.4 and P5.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)			
			P5DIR.x	P5SEL.4	P5SEL.5	XT1BYPASS
P5.4/XIN	4	P5.4 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode(2)	X	1	X	0
		XIN bypass mode(2)	X	1	X	1
P5.5/XOUT	5	P5.5 (I/O)	I: 0; O: 1	0	X	X
		XOUT crystal mode(3)	X	1	X	0
		P5.5 (I/O)(3)	X	1	X	1

(1) X = Don't care
(2) Setting P5SEL.4 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.4 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as general-purpose I/O.

PRODUCT PREVIEW

Port P5, P5.6 to P5.7, Input/Output With Schmitt Trigger



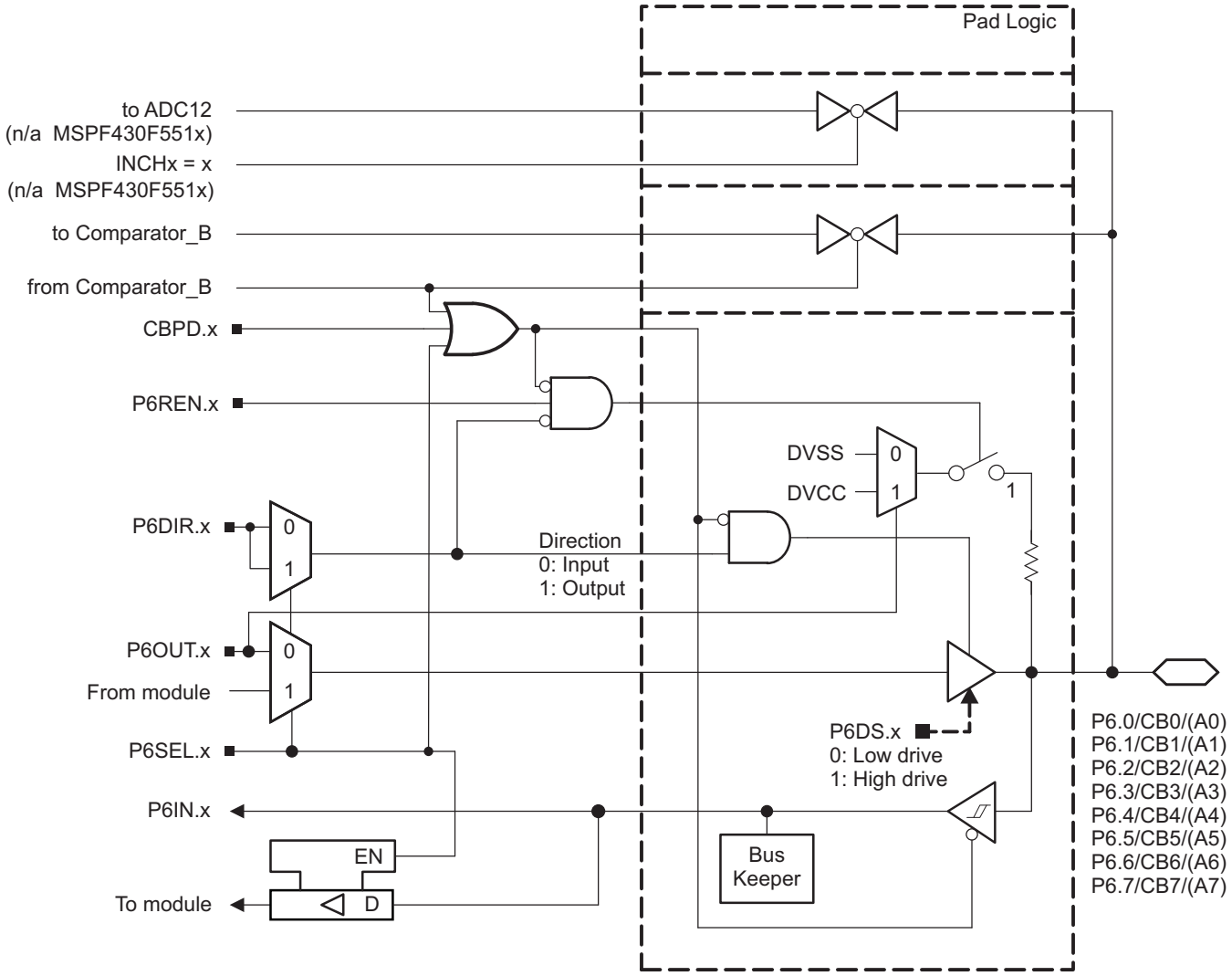
Port P5 (P5.6 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P5DIR.x	P5SEL.x
P5.6/TB0.0 (1)	6	P5.6 (I/O)	I: 0; O: 1	0
		TB0.CCI0A	0	1
		TB0.0	1	1
P5.7/TB0.1 (1)	7	TB0.CCI1A	0	1
		TB0.1	1	1

(1) 'F5529, 'F5527, 'F5525, 'F5521, 'F5519, 'F5517, 'F5515 devices only.

PRODUCT PREVIEW

Port P6, P6.0 to P6.7, Input/Output With Schmitt Trigger

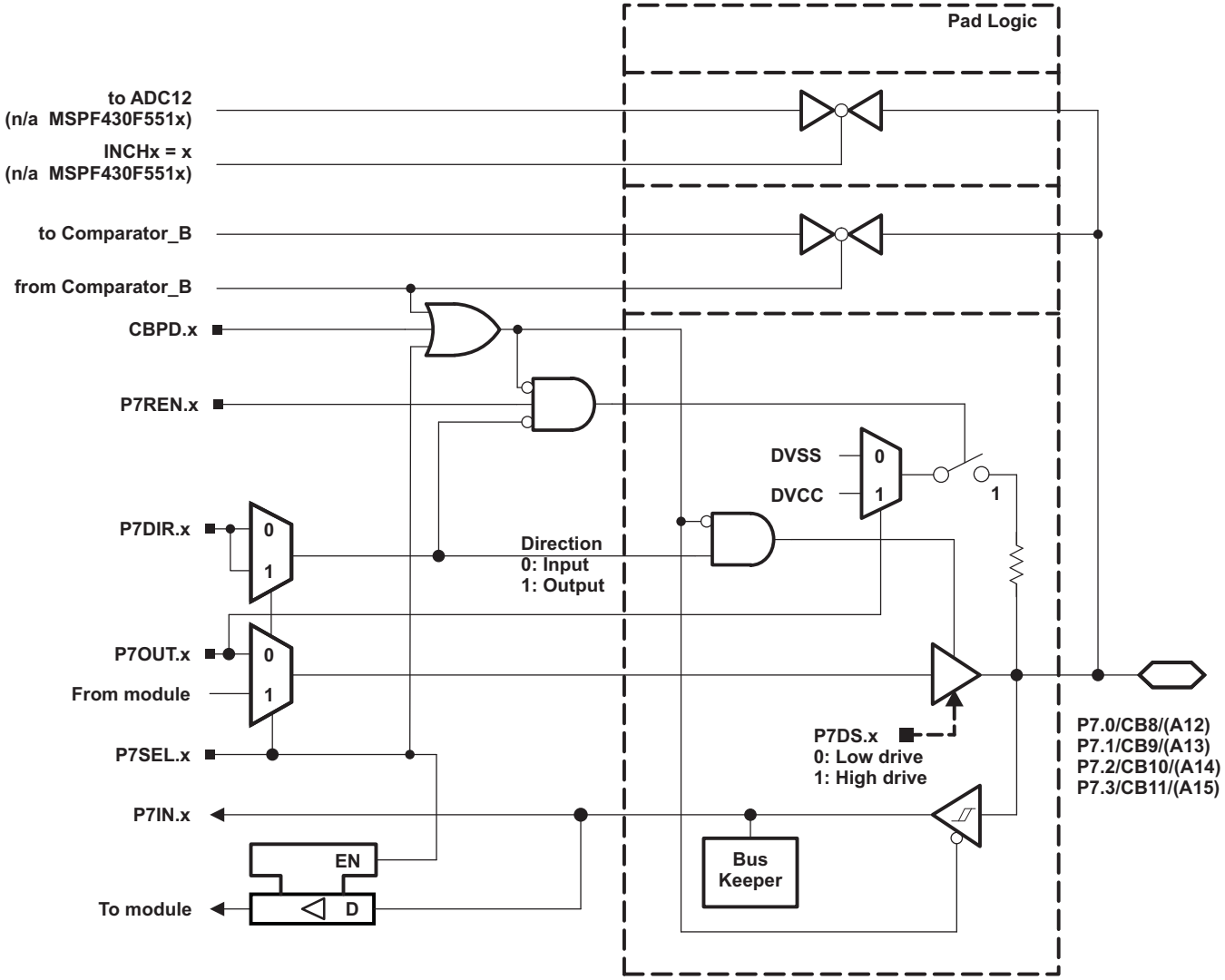


Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS/SIGNALS		
			P6DIR.x	P6SEL.x	CBPD
P6.0/CB0/(A0)	0	P6.0 (I/O)	I: 0; O: 1	0	0
		A0 (only MSP430F552x)	X	1	X
		CB0(1)	X	X	1
P6.1/CB1/(A1)	1	P6.1 (I/O)	I: 0; O: 1	0	0
		A1 (only MSP430F552x)	X	1	X
		CB1(1)	X	X	1
P6.2/CB2/(A2)	2	P6.2 (I/O)	I: 0; O: 1	0	0
		A2 (only MSP430F552x)	X	1	X
		CB2(1)	X	X	1
P6.3/CB3/(A3)	3	P6.3 (I/O)	I: 0; O: 1	0	0
		A3 (only MSP430F552x)	X	1	X
		CB3(1)	X	X	1
P6.4/CB4/(A4)	4	P6.4 (I/O)	I: 0; O: 1	0	0
		A4 (only MSP430F552x)	X	1	X
		CB4(1)	X	X	1
P6.5/CB5/(A5)	5	P6.5 (I/O)	I: 0; O: 1	0	0
		A5 (only MSP430F552x)	X	1	X
		CB5(1)	X	X	1
P6.6/CB6/(A6)	6	P6.6 (I/O)	I: 0; O: 1	0	0
		A6 (only MSP430F552x)	X	1	X
		CB6(1)	X	X	1
P6.7/CB7/(A7)	7	P6.7 (I/O)	I: 0; O: 1	0	0
		A7 (only MSP430F552x)	X	1	X
		CB7(1)	X	X	1

(1) Setting the CBPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

Port P7, P7.0 to P7.3, Input/Output With Schmitt Trigger

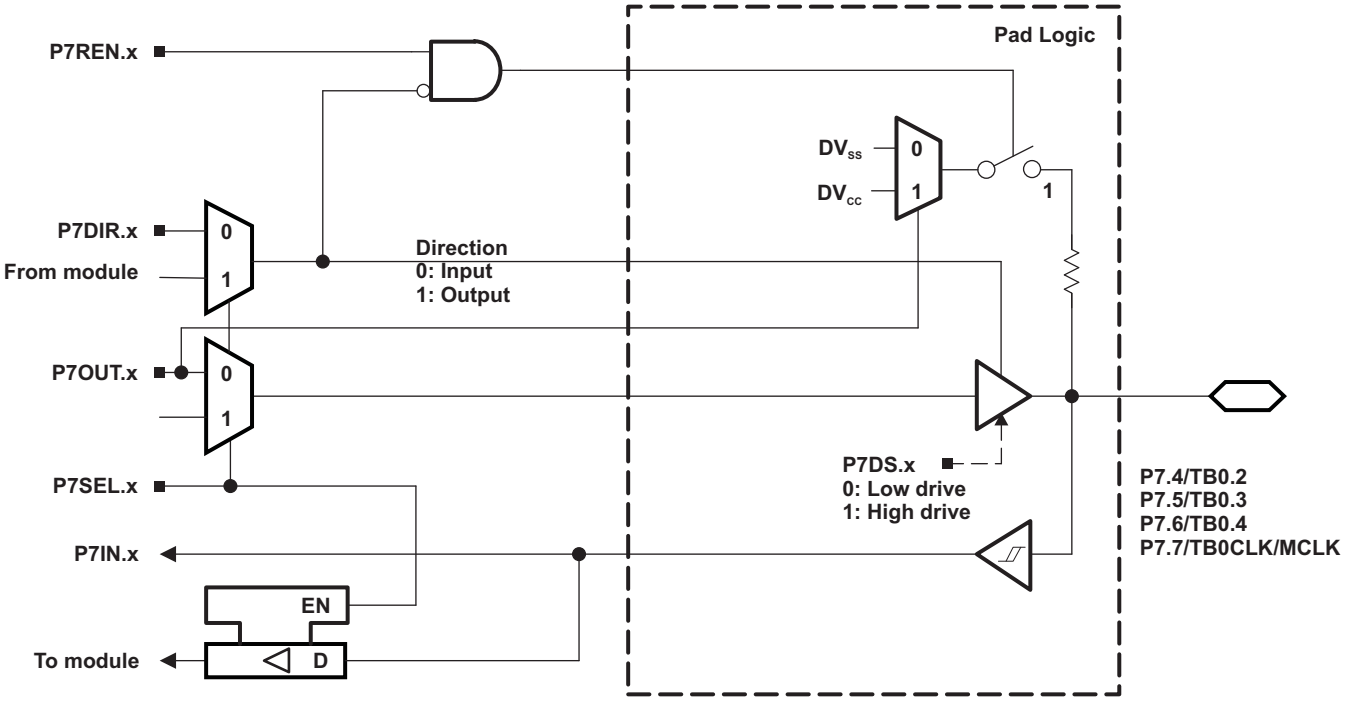


Port P7 (P7.0 to P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS		
			P7DIR.x	P7SEL.x	CBPD
P7.0/CB8/(A12)	0	P7.0 (I/O) (1)	I: 0; O: 1	0	0
		A12 (2)	X	1	X
		CB8(3) (1)	X	X	1
P7.1/CB9/(A13)	1	P7.1 (I/O)(1)	I: 0; O: 1	0	0
		A13 (2)	X	1	X
		CB9(3)(1)	X	X	1
P7.2/CB10/(A14)	2	P7.2 (I/O)(1)	I: 0; O: 1	0	0
		A14(2)	X	1	X
		CB10(3)(1)	X	X	1
P7.3/CB11/(A15)	3	P7.3 (I/O)(1)	I: 0; O: 1	0	0
		A15(2)	X	1	X
		CB11(3)(1)	X	X	1

(1) 'F5529, 'F5527, 'F5525, 'F5521, 'F5519, 'F5517, 'F5515 devices only.
(2) 'F5529, 'F5527, 'F5525, 'F5521 devices only.
(3) Setting the CBPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

Port P7, P7.4 to P7.7, Input/Output With Schmitt Trigger



Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P7DIR.x	P7SEL.x
P7.4/TB0.2(1)	4	P7.4 (I/O)	I: 0; O: 1	0
		TB0.CCI2A	0	1
		TB0.2	1	1
P7.5/TB0.3(1)	5	P7.5 (I/O)	I: 0; O: 1	0
		TB0.CCI3A	0	1
		TB0.3	1	1
P7.6/TB0.4(1)	6	P7.6 (I/O)	I: 0; O: 1	0
		TB0.CCI4A	0	1
		TB0.4	1	1
P7.7/TB0CLK/MCLK(1)	7	P7.7 (I/O)	I: 0; O: 1	0
		TB0CLK	0	1
		MCLK	1	1

(1) 'F5529, 'F5527, 'F5525, 'F5521, 'F5519, 'F5517, 'F5515 devices only.

PRODUCT PREVIEW

Port P8, P8.0 to P8.2, Input/Output With Schmitt Trigger

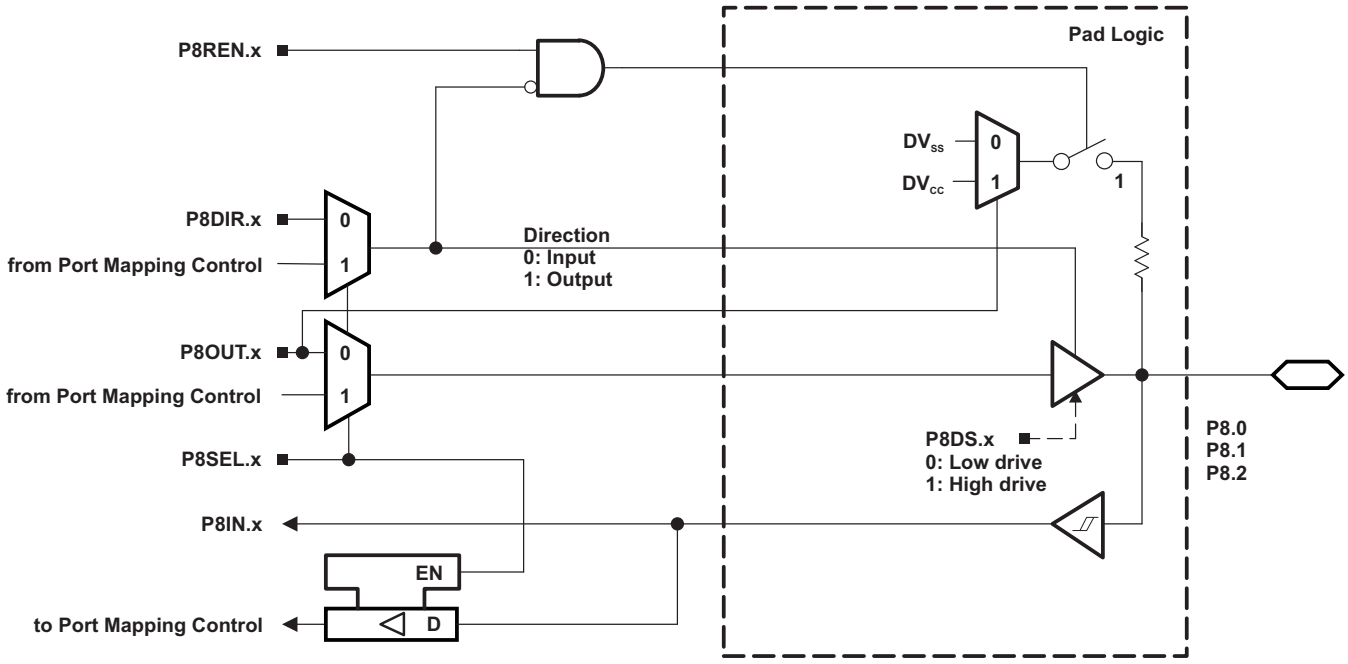


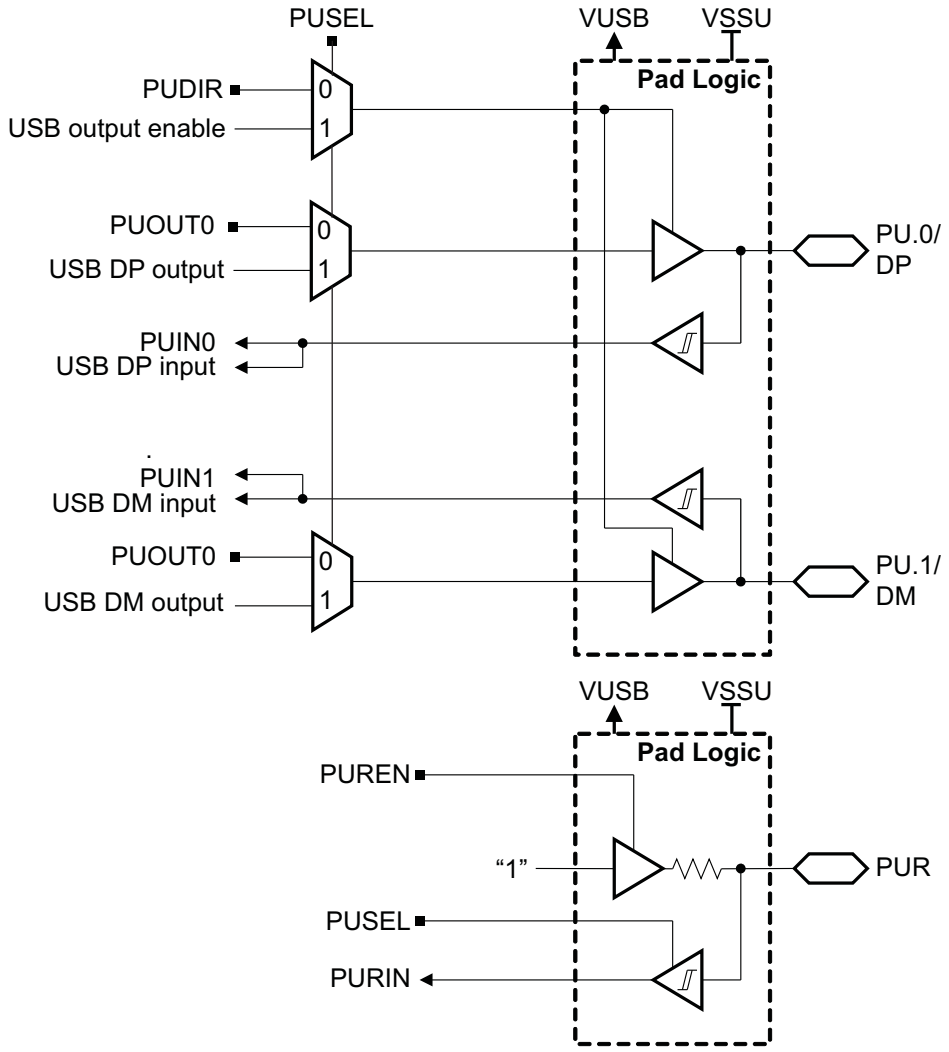
Table 47. Port P8 (P8.0 to P8.2) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P8DIR.x	P8SEL.x
P8.0(1)	0	P8.0(I/O)	I: 0; O: 1	0
P8.1(1)	1	P8.1(I/O)	I: 0; O: 1	0
P8.2(1)	2	P8.2(I/O)	I: 0; O: 1	0

(1) 'F5529, 'F5527, 'F5525, 'F5521, 'F5519, 'F5517, 'F5515 devices only.

PRODUCT PREVIEW

Port PU.0/DP, PU.1/DM, PUR USB Ports



Port PU.0/DP, PU.1/DM Output Functions

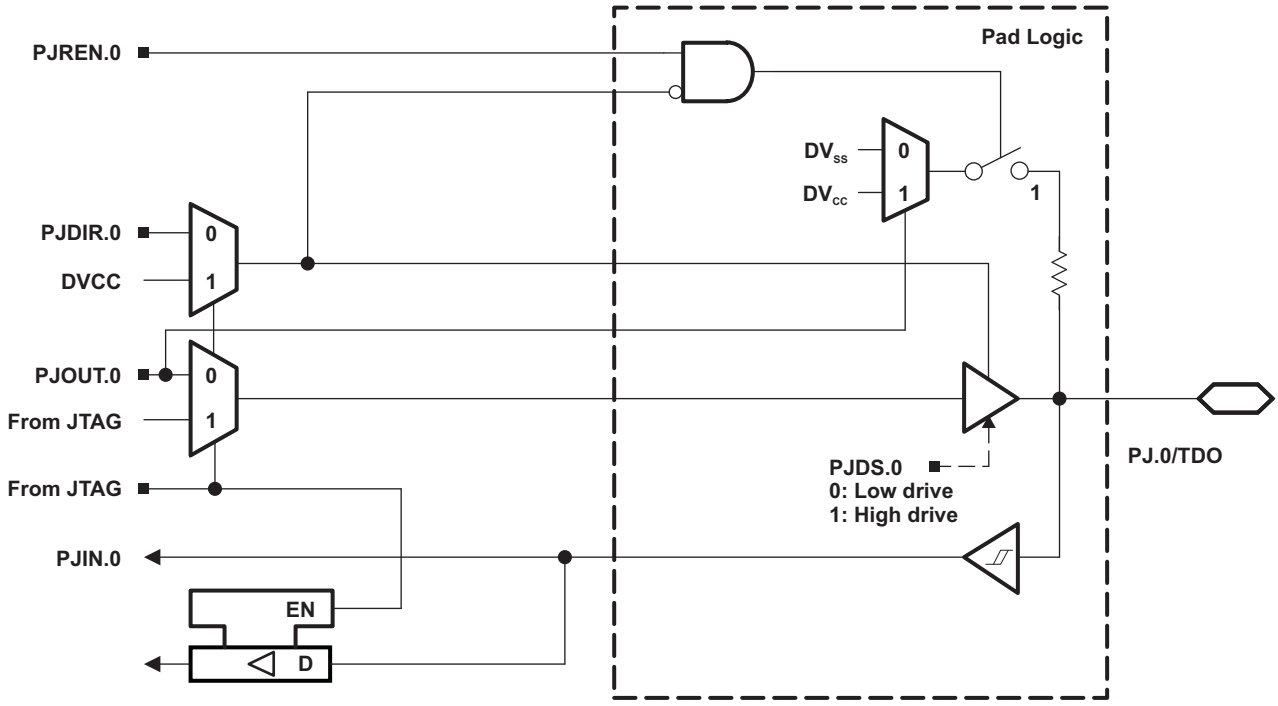
CONTROL BITS				PIN NAME		FUNCTION
PUSEL	PUDIR	PUOUT1	PUOUT0	PU.1/DM	PU.0/DP	
0	0	X	X	Hi-Z	Hi-Z	Outputs off
0	1	0	0	0	0	Outputs enabled
0	1	0	1	0	1	Outputs enabled
0	1	1	0	1	0	Outputs enabled
0	1	1	1	1	1	Outputs enabled
1	X	X	X	DM	DP	Direction set by USB module

PRODUCT PREVIEW

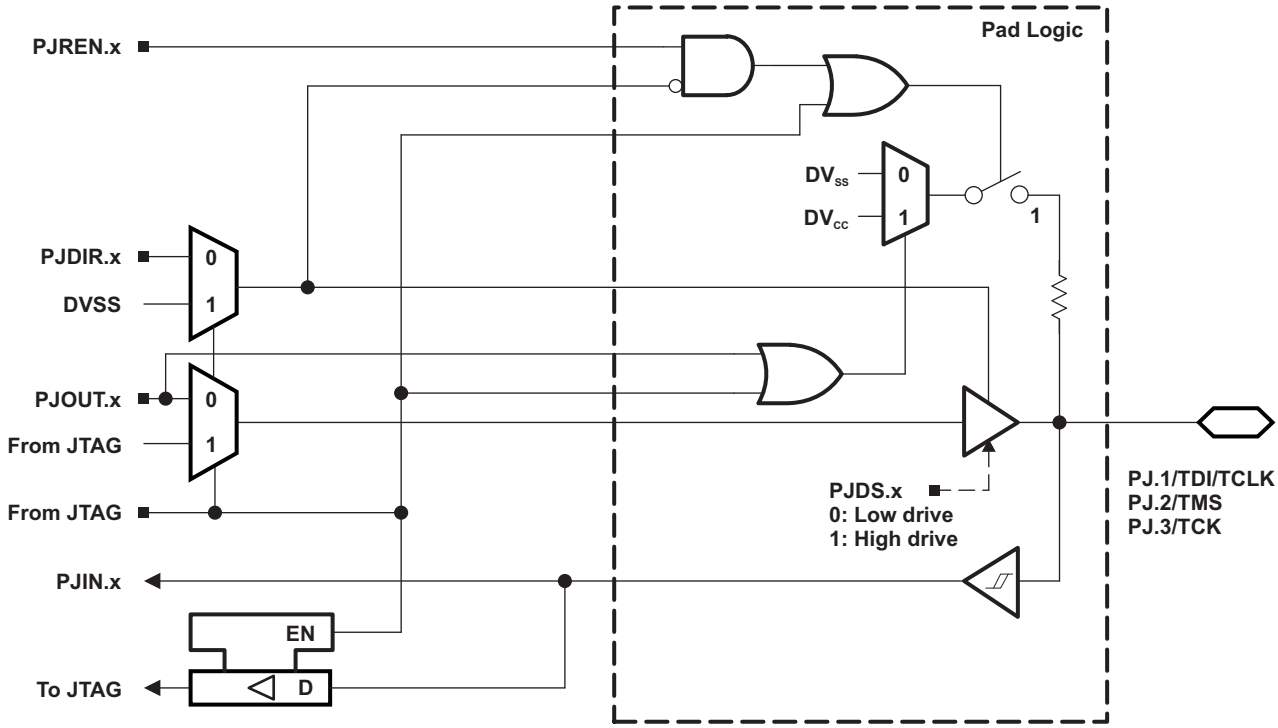
Port PUR Input Functions

CONTROL BITS		FUNCTION
PUSEL	PUREN	
0	0	Input disabled Pull up disabled
0	1	Input disabled Pull up enabled
1	0	Input enabled Pull up disabled
1	1	Input enabled Pull up enabled

Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output



PRODUCT PREVIEW

Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS(1)
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O)(2)	I: 0; O: 1
		TDO(3)	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O)(2)	I: 0; O: 1
		TDI/TCLK(3)(4)	X
PJ.2/TMS	2	PJ.2 (I/O)(2)	I: 0; O: 1
		TMS(3)(4)	X
PJ.3/TCK	3	PJ.3 (I/O)(2)	I: 0; O: 1
		TCK(3)(4)	X

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

DEVICE DESCRIPTORS

Table 48 and Table 49 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 48. 'F552x Device Descriptor Table(1)

	Description	Address	Size bytes	'F5529	'F5528	'F5527	'F5526	'F5525	'F5524	'F5522	'F5521
				Value	Value	Value	Value	Value	Value	Value	Value
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	1	55h	55h	55h	55h	55h	55h	55h	55h
	Device ID	01A05h	1	29h	28h	27h	26h	25h	24h	22h	21h
	Hardware revision	01A06h	1	10h	10h	10h	10h	10h	10h	10h	10h
	Firmware revision	01A07h	1	10h	10h	10h	10h	10h	10h	10h	10h
Die Record	Die Record Tag	01A08h	1	08h	08h	08h	08h	08h	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
ADC12 Calibration	ADC12 Calibration Tag	01A14h	1	11h	11h	11h	11h	11h	11h	11h	11h
	ADC12 Calibration length	01A15h	1	10h	10h	10h	10h	10h	10h	10h	10h
	ADC Gain Factor		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC Offset		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 30°C		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 85°C		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 30°C		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 85°C		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 30°C		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 85°C		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
REF Calibration	REF Calibration Tag	01A26h	1	12h	12h	12h	12h	12h	12h	12h	12h
	REF Calibration length	01A27h	1	06h	06h	06h	06h	06h	06h	06h	06h
	REF 1.5-V Reference Factor		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	REF 2.0-V Reference Factor		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	REF 2.5-V Reference Factor		2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
Peripheral Descriptor	Peripheral Descriptor Tag	01A2Eh	1	02h	02h	02h	02h	02h	02h	02h	02h
	Peripheral Descriptor Length	01A2Fh	1	63h	61h	65h	63h	63h	61h	61h	64h

(1) NA = Not applicable, blank = unused and reads FFh.

PRODUCT PREVIEW

Table 48. 'F552x Device Descriptor Table (continued)

	Description	Address	Size bytes	'F5529	'F5528	'F5527	'F5526	'F5525	'F5524	'F5522	'F5521
				Value	Value	Value	Value	Value	Value	Value	Value
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah
	Memory 4		2	12h 2Eh	12h 2Eh	12h 2Dh	12h 2Dh	12h 2Ch	12h 2Ch	12h 2Eh	12h 2Dh
	Memory 5		2	22h 96h	22h 96h	2Ah 22h	2Ah 22h	22h 94h	22h 94h	40h 92h	2Ah 40h
	Memory 6		1/2	N/A	N/A	95h 92h	95h 92h	N/A	N/A	N/A	92h
	delimiter		1	00h	00h	00h	00h	00h	00h	00h	00h
	Peripheral count		1	21h	20h	21h	20h	21h	20h	20h	21h
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h
	JTAG		2	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-L		2	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h
	CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch
	CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h
	REF		2	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h
	Port Mapping		2	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h
	Port 1/2		2	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h
	Port 3/4		2	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5/6		2	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h
	Port 7/8		2	02h 54h	N/A	02h 54h	N/A	02h 54h	N/A	N/A	02h 54h

Table 48. 'F552x Device Descriptor Table (continued)

	Description	Address	Size bytes	'F5529	'F5528	'F5527	'F5526	'F5525	'F5524	'F5522	'F5521
				Value	Value	Value	Value	Value	Value	Value	Value
	JTAG		2	0Ch 5Fh	0Eh 5Fh	0Ch 5Fh	0Eh 5Fh	0Ch 5Fh	0Eh 5Fh	0Eh 5Fh	0Ch 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A/B		2	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h
	USCI_A/B		2	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h
	ADC12_A		2	10h D1h	10h D1h	10h D1h	10h D1h	10h D1h	10h D1h	10h D1h	10h D1h
	COMP_B		2	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h
	USB		2	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h
Interrupts	COMP_B		1	A8h	A8h	A8h	A8h	A8h	A8h	A8h	A8h
	TB0.CCIFG0		1	64h	64h	64h	64h	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h	40h	40h	40h	40h
	USCI_A0		1	90h	90h	90h	90h	90h	90h	90h	90h
	USCI_B0		1	91h	91h	91h	91h	91h	91h	91h	91h
	ADC12_A		1	D0h	D0h	D0h	D0h	D0h	D0h	D0h	D0h
	TA0.CCIFG0		1	60h	60h	60h	60h	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h	61h	61h	61h	61h
	USB		1	98h	98h	98h	98h	98h	98h	98h	98h
	DMA		1	46h	46h	46h	46h	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h	63h	63h	63h	63h
	P1		1	50h	50h	50h	50h	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h	93h	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h	66h	66h	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h	67h	67h	67h	67h	67h
	P2		1	51h	51h	51h	51h	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h	68h	68h	68h	68h
	delimiter		1	00h	00h	00h	00h	00h	00h	00h	00h

PRODUCT PREVIEW

Table 49. 'F551x Device Descriptor Table(1)

	Description	Address	Size bytes	'F5519	'F5517	'F5515	'F5514	'F5513
				Value	Value	Value	Value	Value
Info Block	Info length	01A00h	1	55h	55h	55h	55h	55h
	CRC length	01A01h	1	19h	17h	15h	14h	13h
	CRC value	01A02h	2	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	1	22h	21h	55h	55h	20h
	Device ID	01A05h	1	80h	80h	15h	14h	80h
	Hardware revision	01A06h	1	10h	10h	10h	10h	10h
	Firmware revision	01A07h	1	10h	10h	10h	10h	10h
Die Record	Die Record Tag	01A08h	1	08h	08h	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit	per unit	per unit
ADC12 Calibration	ADC12 Calibration Tag	01A14h	1	05h	05h	11h	11h	05h
	ADC12 Calibration length	01A15h	1	10h	10h	10h	10h	10h
	ADC Gain Factor		2	blank	blank	blank	blank	blank
	ADC Offset		2	blank	blank	blank	blank	blank
	ADC 1.5-V Reference Temp. Sensor 30°C		2	blank	blank	blank	blank	blank
	ADC 1.5-V Reference Temp. Sensor 85°C		2	blank	blank	blank	blank	blank
	ADC 2.0-V Reference Temp. Sensor 30°C		2	blank	blank	blank	blank	blank
	ADC 2.0-V Reference Temp. Sensor 85°C		2	blank	blank	blank	blank	blank
	ADC 2.5-V Reference Temp. Sensor 30°C		2	blank	blank	blank	blank	blank
	ADC 2.5-V Reference Temp. Sensor 85°C		2	blank	blank	blank	blank	blank
REF Calibration	REF Calibration Tag	01A26h	1	12h	12h	12h	12h	12h
	REF Calibration length	01A27h	1	06h	06h	06h	06h	06h
	REF 1.5-V Reference Factor		2	per unit	per unit	per unit	per unit	per unit
	REF 2.0-V Reference Factor		2	per unit	per unit	per unit	per unit	per unit

(1) NA = Not applicable, blank = unused and reads FFh.

Table 49. 'F551x Device Descriptor Table (continued)

	Description	Address	Size bytes	'F5519	'F5517	'F5515	'F5514	'F5513
				Value	Value	Value	Value	Value
	REF 2.5-V Reference Factor		2	per unit	per unit	per unit	per unit	per unit
Peripheral Descriptor	Peripheral Descriptor Tag	01A2Eh	1	02h	02h	02h	02h	02h
	Peripheral Descriptor Length	01A2Fh	1	61h	63h	61h	5Fh	5Fh
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah
	Memory 4		2	12h 2Eh	12h 2Dh	12h 2Ch	12h 2Ch	12h 2Ch
	Memory 5		2	22h 96h	2Ah 22h	22h 94h	22h 94h	40h 92h
	Memory 6		1/2	N/A	95h 92h	N/A	N/A	N/A
	delimiter		1	00h	00h	00h	00h	00h
	Peripheral count		1	20h	20h	20h	1Fh	1Fh
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h
	JTAG		2	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-L		2	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h
	CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch
	CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h
	REF		2	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h
	Port Mapping		2	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h
	Port 1/2		2	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h

PRODUCT PREVIEW

Table 49. 'F551x Device Descriptor Table (continued)

	Description	Address	Size bytes	'F5519	'F5517	'F5515	'F5514	'F5513
				Value	Value	Value	Value	Value
	Port 3/4		2	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5/6		2	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h
	Port 7/8		2	02h 54h	02h 54h	02h 54h	N/A	N/A
	JTAG		2	0Ch 5Fh	0Ch 5Fh	0Ch 5Fh	0Eh 5Fh	0Eh 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A/B		2	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h
	USCI_A/B		2	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h
	ADC12_A		2	N/A	N/A	N/A	N/A	N/A
	COMP_B		2	2Ch A8h	2Ch A8h	2Ch A8h	2Ch A8h	2Ch A8h
	USB		2	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h
Interrupts	COMP_B		1	A8h	A8h	A8h	A8h	A8h
	TB0.CCIFG0		1	64h	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h	40h
	USCI_A0		1	90h	90h	90h	90h	90h
	USCI_B0		1	91h	91h	91h	91h	91h
	ADC12_A		1	01h	01h	01h	01h	01h
	TA0.CCIFG0		1	60h	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h	61h
	USB		1	98h	98h	98h	98h	98h
	DMA		1	46h	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h	63h
	P1		1	50h	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h	67h	67h
	P2		1	51h	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h	68h

Table 49. 'F551x Device Descriptor Table (continued)

	Description	Address	Size bytes	'F5519	'F5517	'F5515	'F5514	'F5513
				Value	Value	Value	Value	Value
	delimiter		1	00h	00h	00h	00h	00h

Revision History

REVISION	DESCRIPTION
SLAS590	Limited product preview release
SLAS590A	Changes throughout for XMS430F5529 sampling
SLAS590B	Changes throughout for updated preview

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430F5514IRGC	PREVIEW	VQFN	RGC	64	250	TBD	Call TI	Call TI
MSP430F5514IRGCR	PREVIEW	VQFN	RGC	64	2000	TBD	Call TI	Call TI
MSP430F5515IPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F5515IPNR	PREVIEW	LQFP	PN	80	1000	TBD	Call TI	Call TI
MSP430F5524IRGCR	PREVIEW	VQFN	RGC	64	2000	TBD	Call TI	Call TI
MSP430F5525IPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F5525IPNR	PREVIEW	LQFP	PN	80	1000	TBD	Call TI	Call TI
MSP430F5526IRGC	PREVIEW	VQFN	RGC	64	250	TBD	Call TI	Call TI
MSP430F5526IRGCR	PREVIEW	VQFN	RGC	64	2000	TBD	Call TI	Call TI
MSP430F5527IPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F5527IPNR	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F5528IRGC	PREVIEW	VQFN	RGC	64	250	TBD	Call TI	Call TI
MSP430F5528IRGCR	PREVIEW	VQFN	RGC	64	2000	TBD	Call TI	Call TI
MSP430F5529IPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F5529IPNR	PREVIEW	LQFP	PN	80	1000	TBD	Call TI	Call TI
XMS430F5529IPN	ACTIVE	LQFP	PN	80	50	TBD	Call TI	Call TI
XMS430F5529IPNR	PREVIEW	LQFP	PN	80	1000	TBD	Call TI	Call TI

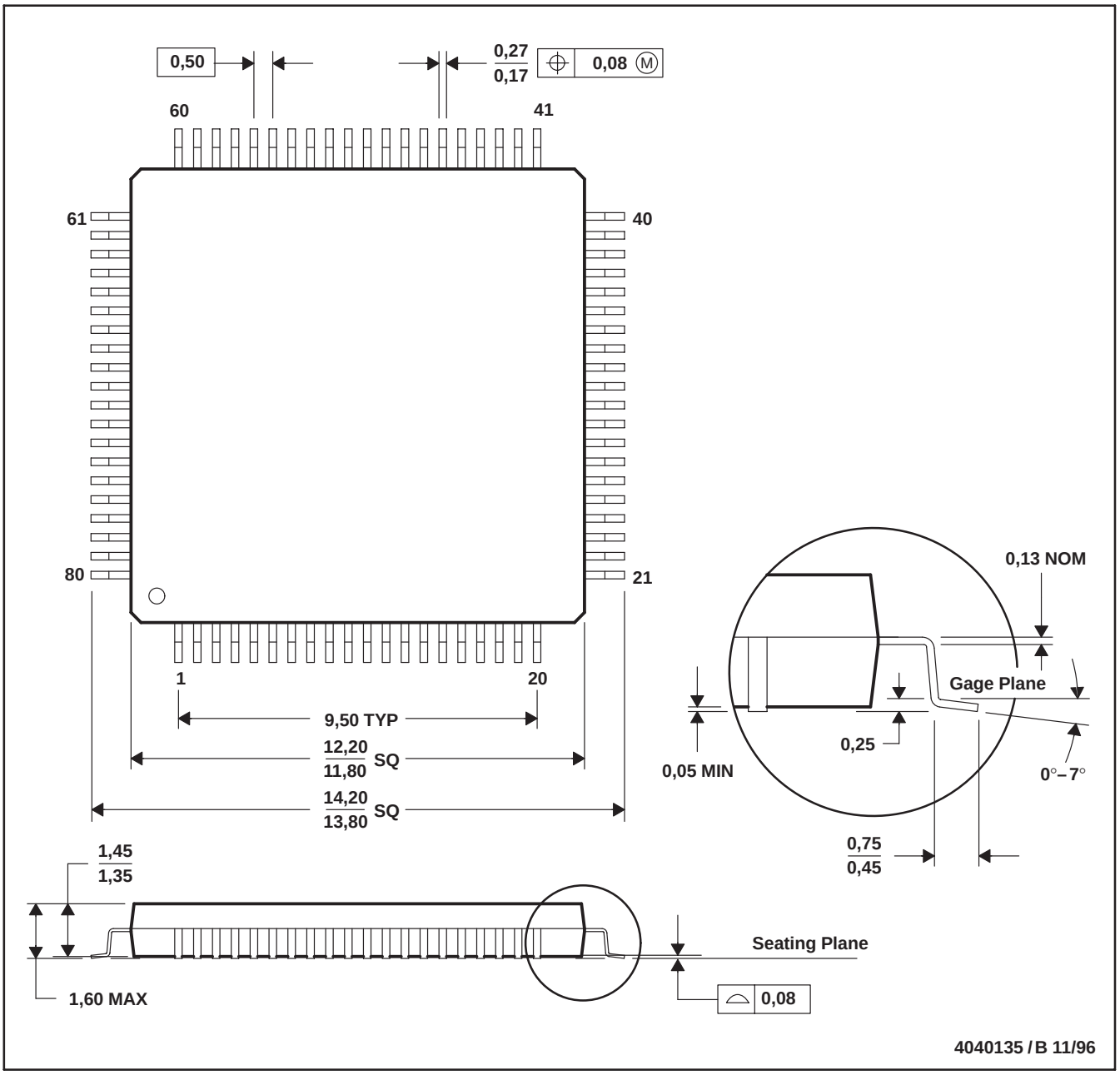
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

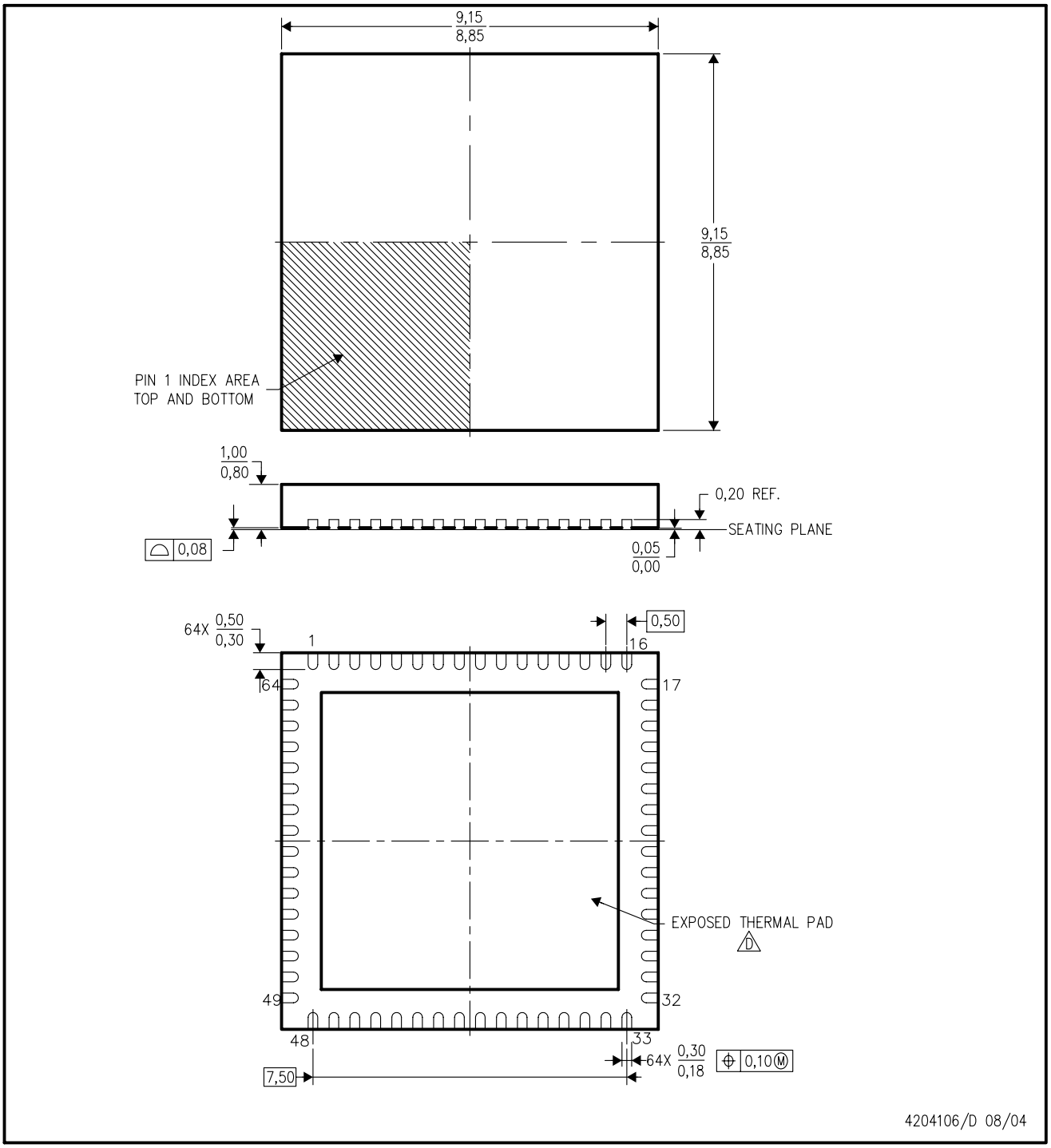
MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

RGC (S–PQFP–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration .
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

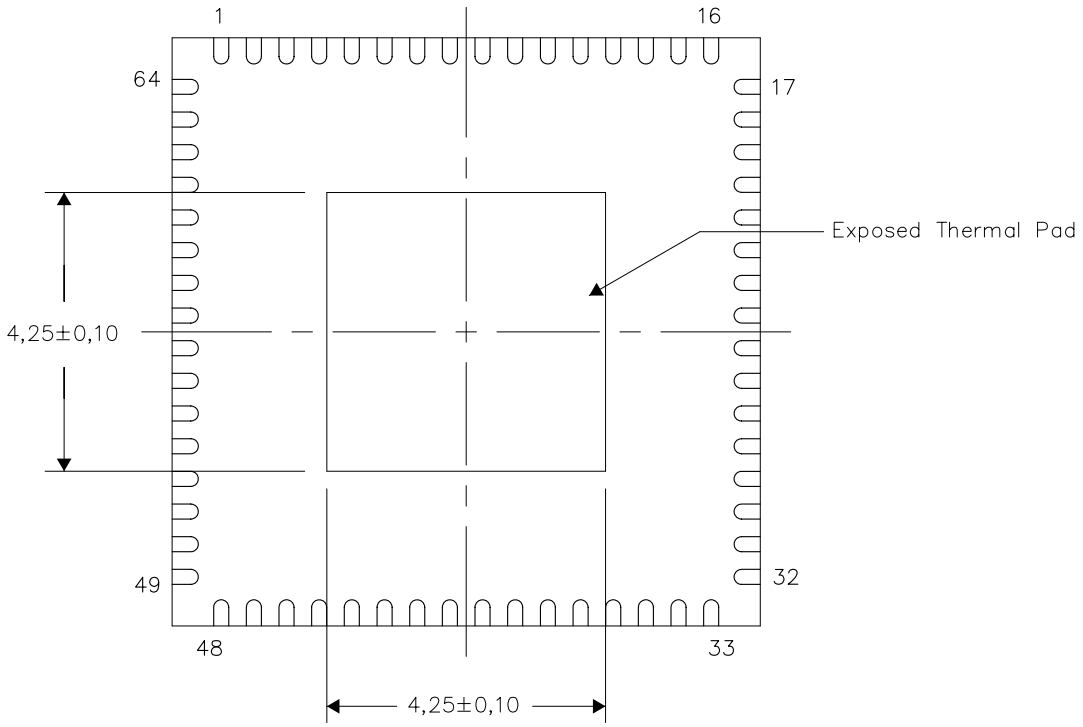
RGC (S–PVQFN–N64)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

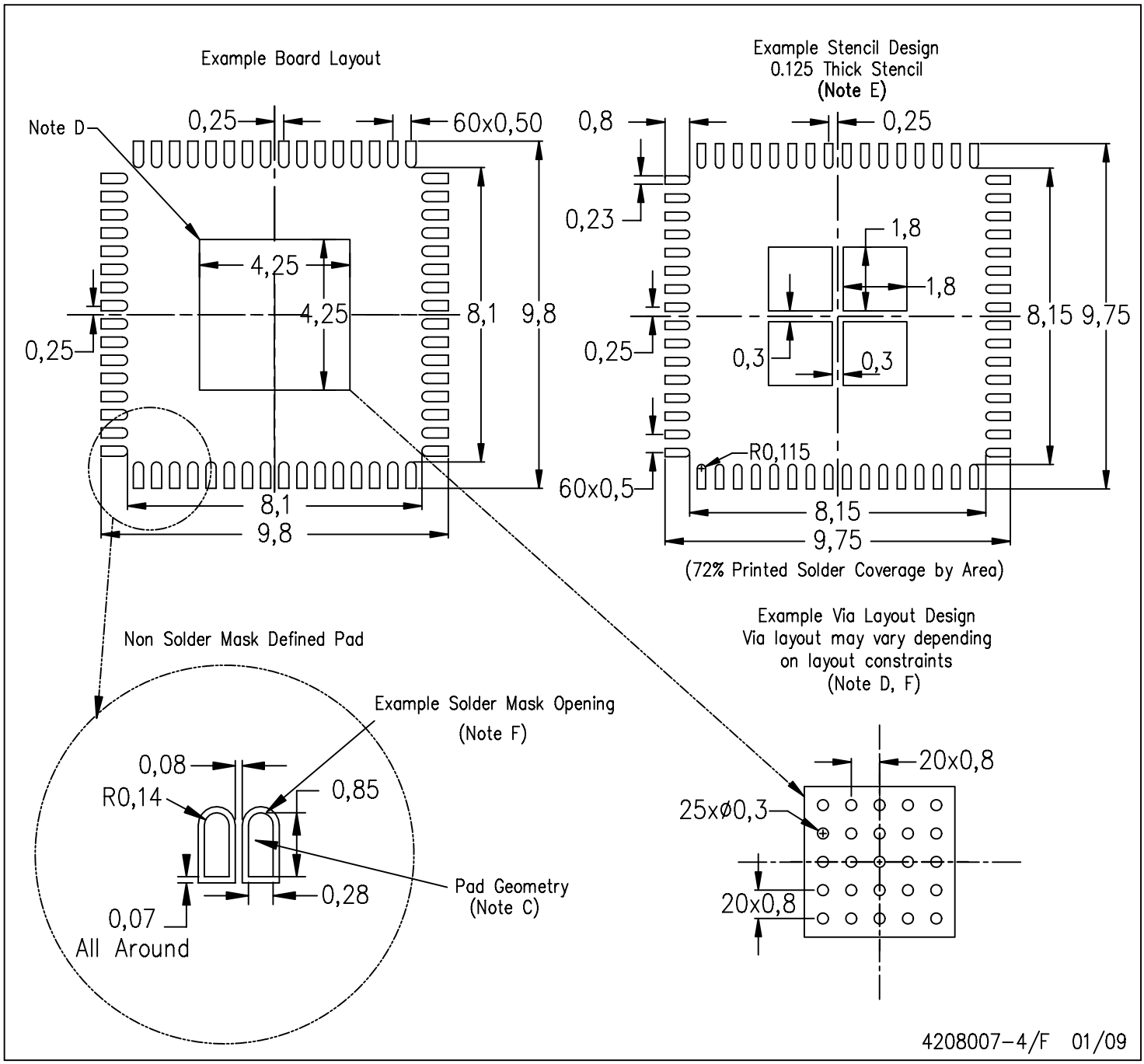


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGC (S–PVQFN–N64)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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