Freescale Semiconductor
Technical Data

MPXAZ6115A
Rev 4, 01/2007

Media Resistant and High Temperature Accuracy Integrated Silicon Pressure Sensor for Measuring Absolute Pressure, On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPXAZ6115A series sensor integrates on-chip, bipolar op amp circuitry and thin film resistor networks to provide a high output signal and temperature compensation. The sensor's packaging has been designed to provide resistance to high humidity conditions as well as common automotive media. The small form factor and high reliability of on-chip integration make the Freescale Semiconductor, Inc. pressure sensor a logical and economical choice for the system designer.

The MPXAZ6115A series piezoresistive transducer is a state-of-the-art, monolithic, signal conditioned, silicon pressure sensor. This sensor combines advanced micromachining techniques, thin film metallization, and bipolar semiconductor processing to provide an accurate, high level analog output signal that is proportional to applied pressure.

Figure 1 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

Features

- Resistant to High Humidity and Common Automotive Media
- Improved Accuracy at High Temperature
- 1.5% Maximum Error over 0° to 85°C
- Ideally suited for Microprocessor or Microcontroller-Based Systems
- Temperature Compensated from -40° to +125°C
- Durable Thermoplastic (PPS) Surface Mount Package

Typical Applications

- Aviation Altimeters
- Industrial Controls
- Engine Control/Manifold Absolute Pressure (MAP)
- Weather Station and Weather Reporting Devices

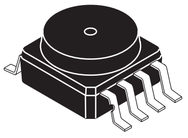
ORDERING INFORMATION

Device Type	Options	Case No.	MPX Series Order No.	Packing Options	Device Marking
SMALL OUTLINE PACKAGE					
Basic Element	Absolute, Element Only	482	MPXAZ6115A6U	Rails	MPXAZ6115A
	Absolute, Element Only	482	MPXAZ6115A6T1	Tape & Reel	MPXAZ6115A
Ported Element	Absolute, Axial Port	482A	MPXAZ6115AC6U	Rails	MPXAZ6115A
	Absolute, Axial Port	482A	MPXAZ6115AC6T1	Tape & Reel	MPXAZ6115A
	Absolute, Side Port	1369	MPXAZ6115AP	Tray	MPXAZ6115A
	Absolute, Side Port	1369	MPXAZ6115APT1	Tape & Reel	MPXAZ6115A
SUPER SMALL OUTLINE PACKAGE					
Basic Element	Absolute, Element Only	1317	MPXHZ6115A6U	Rails	MPXHZ6115A
	Absolute, Element Only	1317	MPXHZ6115A6T1	Tape & Reel	MPXHZ6115A
Ported Element	Absolute, Axial Port	1317A	MPXHZ6115AC6U	Rails	MPXHZ6115A
	Absolute, Axial Port	1317A	MPXHZ6115AC6T1	Tape & Reel	MPXHZ6115A

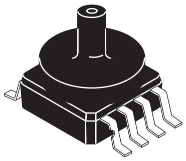
MPXAZ6115A
MPXHZ6115A
SERIES

INTEGRATED
PRESSURE SENSOR
15 TO 115 kPA (2.2 TO 16.7 psi)
0.2 TO 4.8 V OUTPUT

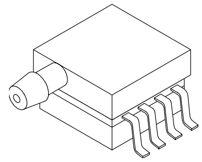
SMALL OUTLINE PACKAGE



MPXAZ6115A6U
CASE 482-01



MPXAZ6115AC6U
CASE 482A-01



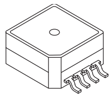
MPXAZ6115AP
CASE 1369-01

SMALL OUTLINE PACKAGE PIN NUMBERS[1]

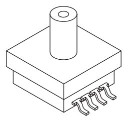
1	N/C	5	N/C
2	V_S	6	N/C
3	GND	7	N/C
4	V_{OUT}	8	N/C

1. Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is denoted by the notch in the lead.

SUPER SMALL OUTLINE PACKAGE



MPXHZ6115A6U
CASE 1317-04



MPXHZ6115AC6U
CASE 1317A-03

SMALL OUTLINE PACKAGE PIN NUMBERS[1]

1	N/C	5	N/C
2	V_S	6	N/C
3	GND	7	N/C
4	V_{OUT}	8	N/C

1. Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is denoted by the notch in the lead.

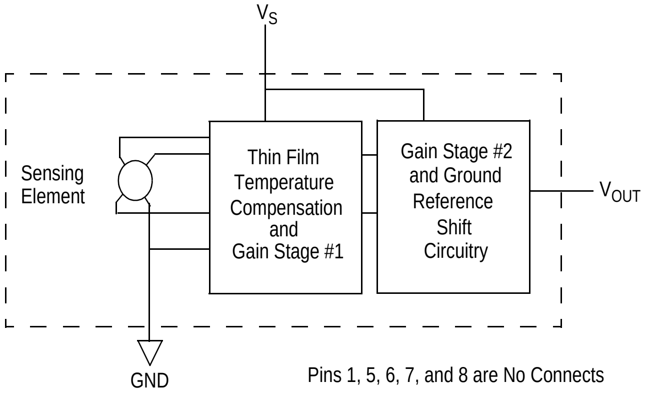


Figure 1. Fully Integrated Pressure Sensor Schematic

Table 1. Maximum Ratings[1]

Rating	Symbol	Value	Units
Maximum Pressure (P1 > P2)	P_{max}	400	kPa
Storage Temperature	T_{stg}	-40° to +125°	°C
Operating Temperature	T_A	-40° to +125°	°C
Output Source Current @ Full Scale Output[2]	I_o+	0.5	mAdc
Output Sink Current @ Minimum Pressure Offset[2]	I_o-	-0.5	mAdc

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.
2. Maximum Output Current is controlled by effective impedance from V_{out} to Gnd or V_{out} to V_S in the application circuit.

Table 2. Operating Characteristics (V_S = 5.0 Vdc, T_A = 25°C unless otherwise noted, P1 > P2)

Characteristic		Symbol	Min	Typ	Max	Unit
Pressure Range		P_{OP}	15	—	115	kPa
Supply Voltage(1)		V_S	4.75	5.0	5.25	Vdc
Supply Current		I_o	—	6.0	10	mAdc
Minimum Pressure Offset(2) @ V_S = 5.0 Volts	(0 to 85°C)	V_{off}	0.133	0.200	0.268	Vdc
Full Scale Output(3) @ V_S = 5.0 Volts	(0 to 85°C)	V_{FSO}	4.633	4.700	4.768	Vdc
Full Scale Span(4) @ V_S = 5.0 Volts	(0 to 85°C)	V_{FSS}	4.433	4.500	4.568	Vdc
Accuracy(5)	(0 to 85°C)	—	—	—	±1.5	$\%V_{FSS}$
Sensitivity		V/P	—	45.9	—	mV/kPa
Response Time(6)		t_R	—	1.0	—	ms
Warm-Up Time(7)		—	—	20	—	ms
Offset Stability(8)		—	—	±0.25	—	$\%V_{FSS}$

1. Device is ratiometric within this specified excitation range.
2. Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
3. Full Scale Output (V_{FSO}) is defined as the output voltage at the maximum or full rated pressure.
4. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
5. Accuracy is the deviation in actual output from nominal output over the entire pressure range and temperature range as a percent of span at 25°C due to all sources of error including the following:
    - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
    - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
    - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from minimum or maximum rated pressure at 25°C.
    - TcSpan: Output deviation over the temperature range of 0° to 85°C, relative to 25°C.
    - TcOffset: Output deviation with minimum pressure applied, over the temperature range of 0° to 85°C, relative to 25°C.
6. Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
7. Warm-up Time is defined as the time required for the product to meet the specified output voltage after the pressure has been stabilized.
8. Offset Stability is the product's output deviation when subjected to 1000 cycles of Pulsed Pressure, Temperature Cycling with Bias Test.

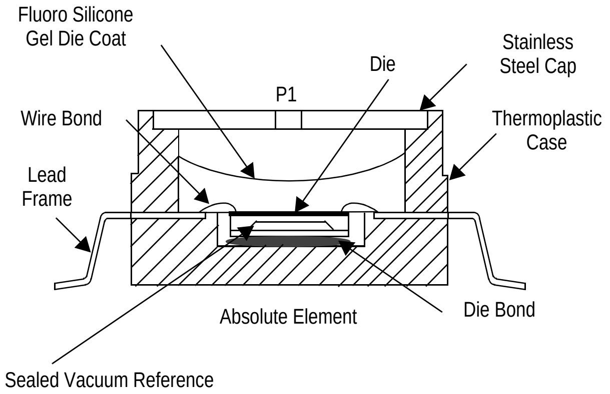


Figure 2. Cross Sectional Diagram SOP (Not to Scale)

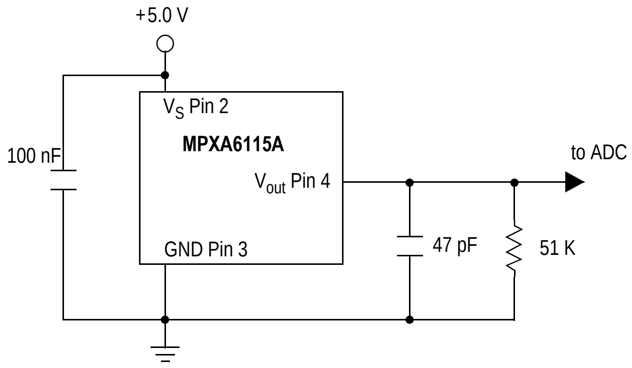


Figure 3. Typical Application Circuit (Output Source Current Operation)

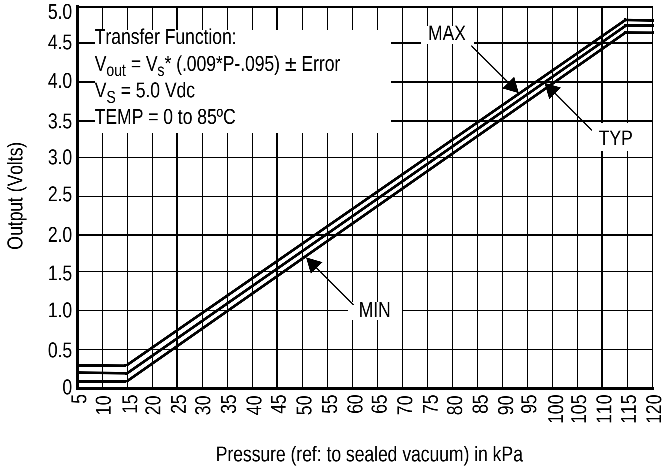


Figure 4. Output versus Absolute Pressure

Figure 4 shows the sensor output signal relative to pressure input. Typical minimum and maximum output curves are shown for operation over 0 to 85°C temperature range. The output will saturate outside of the rated pressure range.

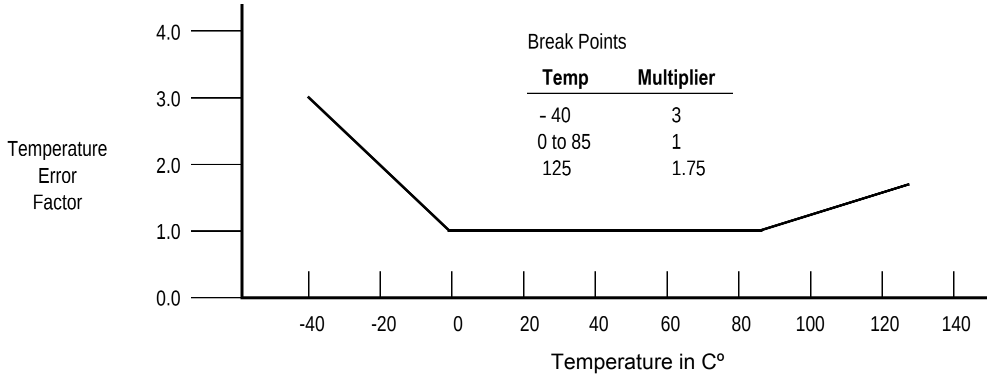
A gel die coat isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the sensor diaphragm. The gel die coat and durable polymer package provide a media resistant barrier that allows the sensor to operate reliably in high humidity conditions as well as environments containing common automotive media. Contact the factory for more information regarding media compatibility in your specific application.

Transfer Function (MPXAZ6115A

Nominal Transfer Value: $V_{out} = V_S \times (0.009 \times P - 0.095)$
$\pm$ (Pressure Error x Temp. Factor x 0.009 x V_S)
$V_S = 5.0 \pm 0.25$ Vdc

Temperature Error Band

MPXAZ6115A Series



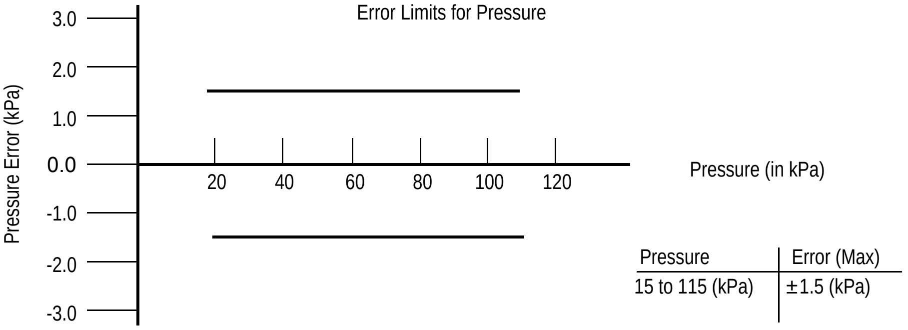
Break Points

Temp	Multiplier
- 40	3
0 to 85	1
125	1.75

NOTE: The Temperature Multiplier is a linear response from 0ºC to -40ºC and from 85ºC to 125ºC

Pressure Error Band

Error Limits for Pressure



Pressure	Error (Max)
15 to 115 (kPa)	±1.5 (kPa)

MINIMUM RECOMMENDED FOOTPRINT FOR SMALL AND SUPER SMALL PACKAGES

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor package must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process. It is always recommended to fabricate boards with a solder mask layer to avoid bridging and/or shorting between solder pads, especially on tight tolerances and/or tight layouts.

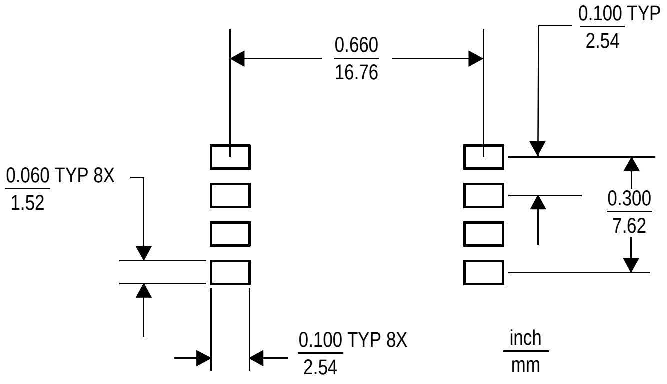


Figure 5. SOP Footprint (Case 482 and 482A)

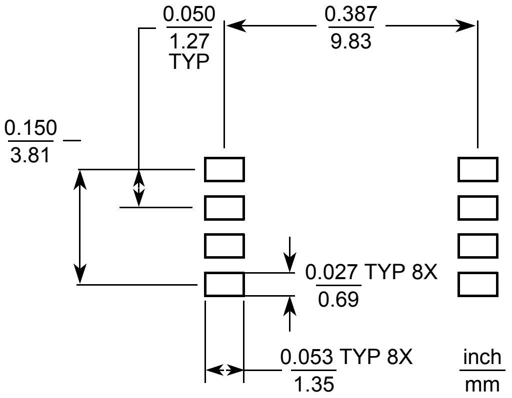
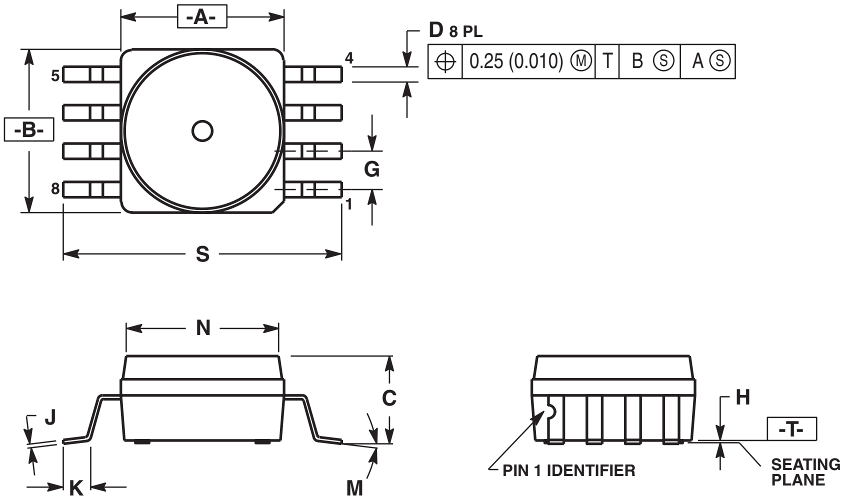


Figure 6. SSOP Footprint (Case 1317 and 1317A)

PACKAGE DIMENSIONS

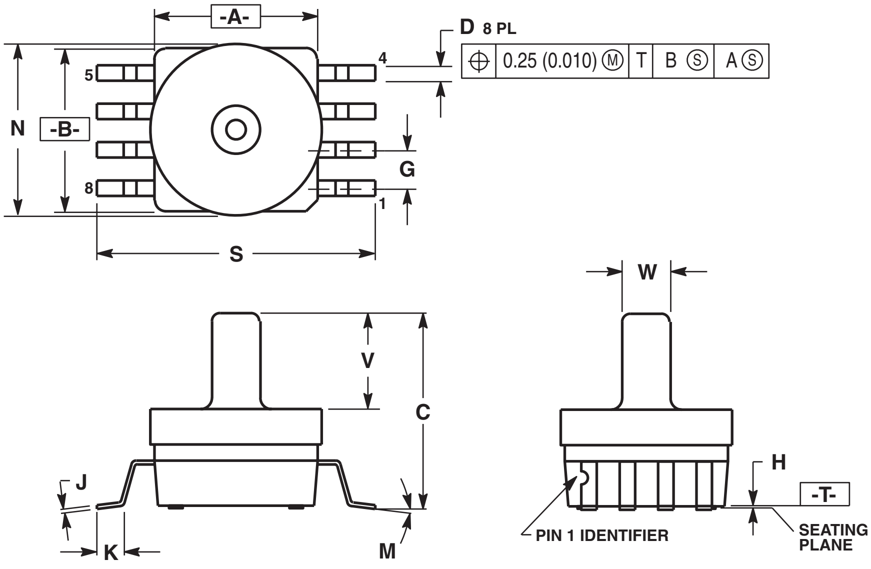


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5˚ TYPICAL DRAFT.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.212	0.230	5.38	5.84
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0˚	7˚	0˚	7˚
N	0.405	0.415	10.29	10.54
S	0.709	0.725	18.01	18.41

CASE 482-01
ISSUE O
SMALL OUTLINE PACKAGE



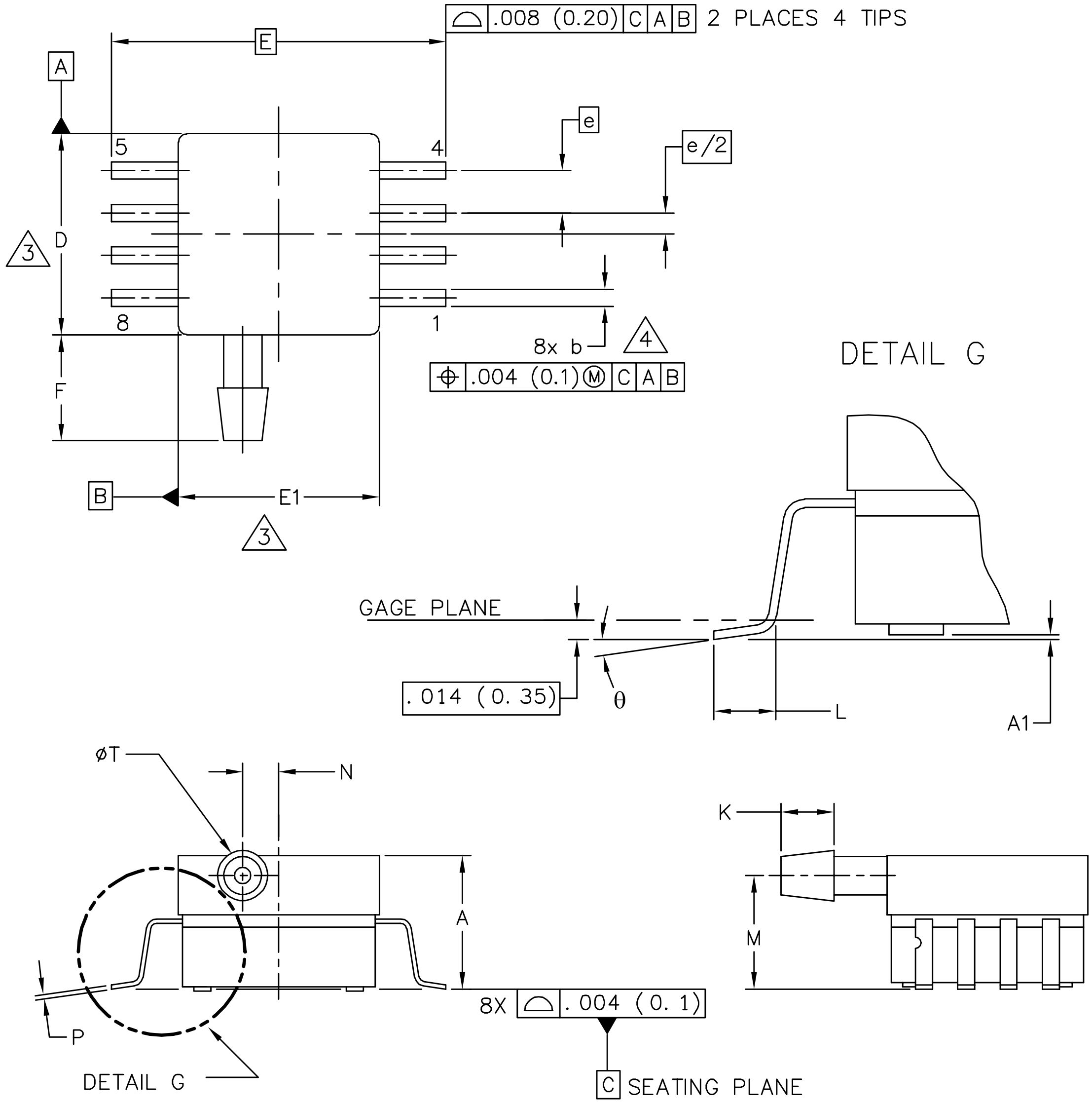
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5˚ TYPICAL DRAFT.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0˚	7˚	0˚	7˚
N	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482A-01
ISSUE A
SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS



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TITLE: 8 LD SOP, SIDE PORT	DOCUMENT NO: 98ASA99303D	REV: B
	CASE NUMBER: 1369-01	24 MAY 2005
	STANDARD: NON-JEDEC	

PAGE 1 OF 2

CASE 1369-01
ISSUE B
SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

△3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS.
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.

△4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.300	.330	7.11	7.62	θ	0°	7°	0°	7°
A1	.002	.010	0.05	0.25	–	---	---	---	---
b	.038	.042	0.96	1.07	–	---	---	---	---
D	.465	.485	11.81	12.32	–	---	---	---	---
E	.717 BSC		18.21 BSC		–	---	---	---	---
E1	.465	.485	11.81	12.32	–	---	---	---	---
e	.100 BSC		2.54 BSC		–	---	---	---	---
F	.245	.255	6.22	6.47	–	---	---	---	---
K	.120	.130	3.05	3.30	–	---	---	---	---
L	.061	.071	1.55	1.80	–	---	---	---	---
M	.270	.290	6.86	7.36	–	---	---	---	---
N	.080	.090	2.03	2.28	–	---	---	---	---
P	.009	.011	0.23	0.28	–	---	---	---	---
T	.115	.125	2.92	3.17	–	---	---	---	---

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

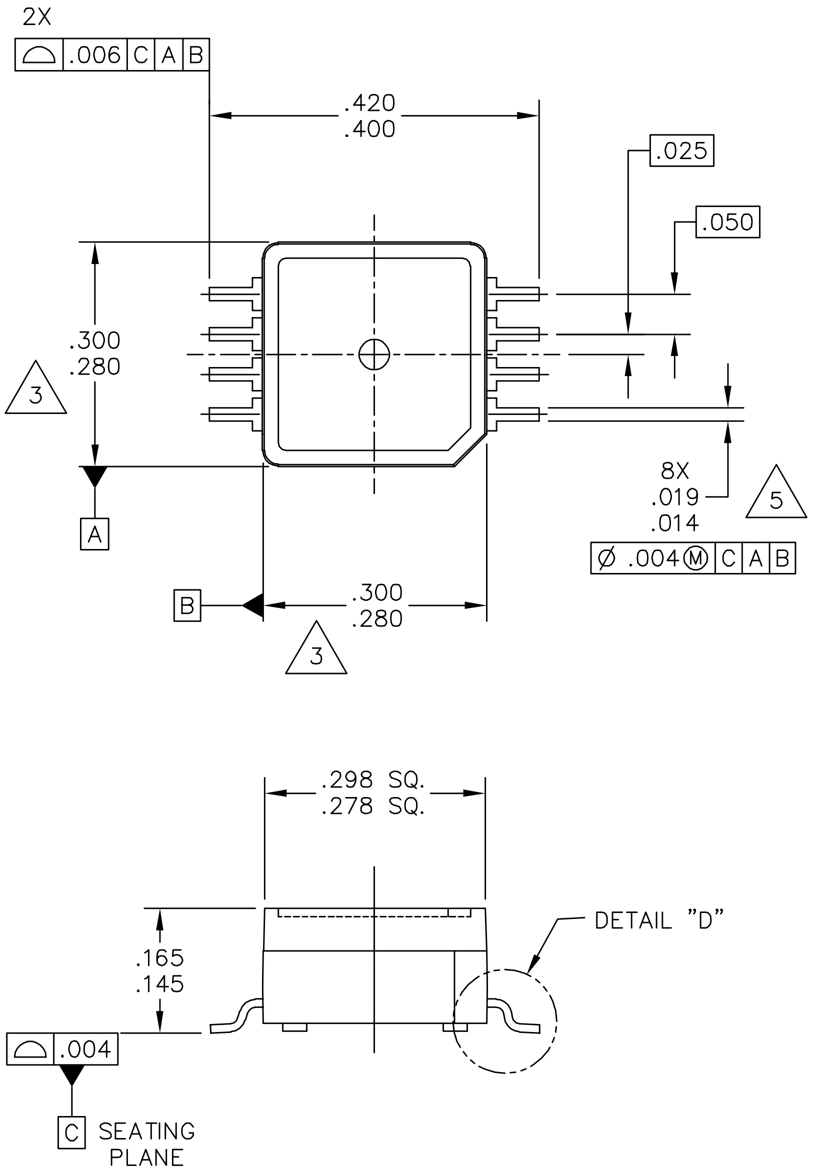
TITLE:
8 LD SOP, SIDE PORT

DOCUMENT NO: 98ASA99303D
REV: B
CASE NUMBER: 1369–01
24 MAY 2005
STANDARD: NON–JEDEC

PAGE 2 OF 2

CASE 1369-01
ISSUE B
SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS



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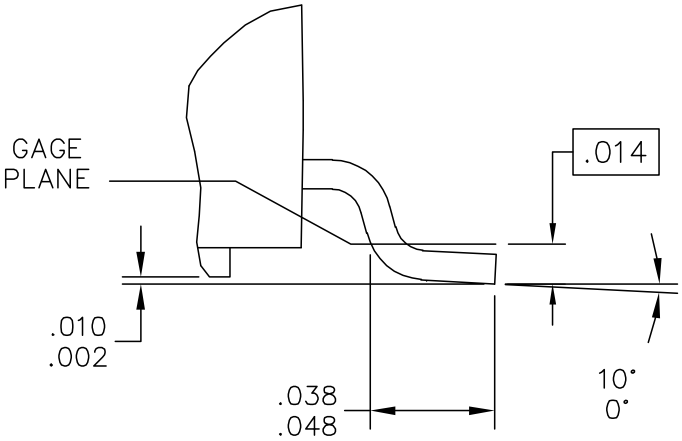
TITLE: 8 LEAD SSOP		DOCUMENT NO: 98ARH99066A	REV: F
		CASE NUMBER: 1317–04	24 MAY 2005
		STANDARD: NON–JEDEC	

PAGE 1 OF 3

CASE 1317-04
ISSUE F
SUPER SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS



DETAIL "D"

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TITLE: 8 LEAD SSOP	DOCUMENT NO: 98ARH99066A	REV: F
	CASE NUMBER: 1317–04	24 MAY 2005
	STANDARD: NON–JEDEC	

PAGE 2 OF 3

CASE 1317-04
ISSUE F
SUPER SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .006 INCHES PER SIDE.
4. ALL VERTICAL SURFACES TO BE 5° MAXIMUM.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 INCHES MAXIMUM.

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE: 8 LEAD SSOP

DOCUMENT NO: 98ARH99066A

REV: F

CASE NUMBER: 1317–04

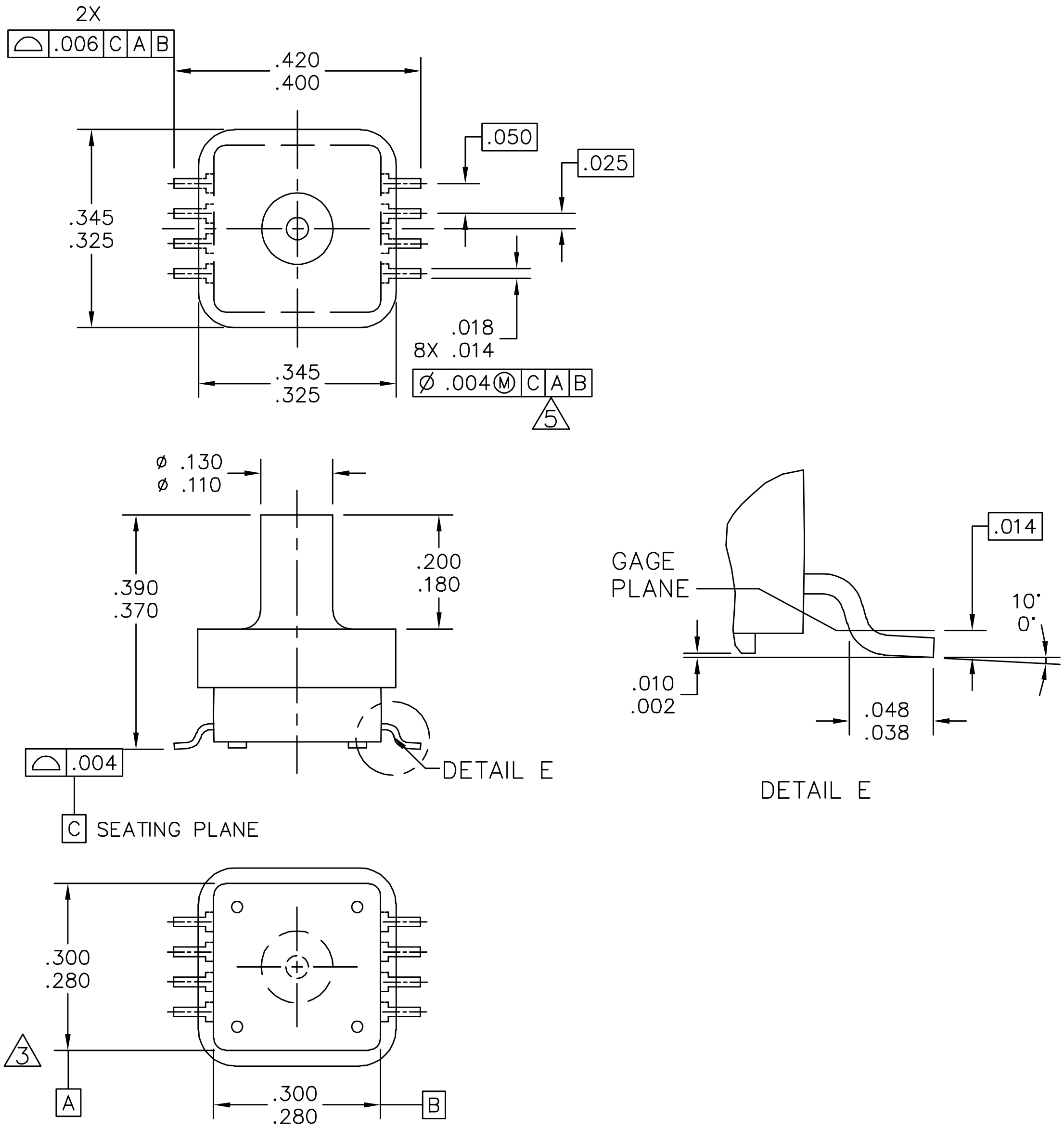
24 MAY 2005

STANDARD: NON–JEDEC

PAGE 3 OF 3

CASE 1317-04
ISSUE F
SUPER SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS



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TITLE: 8 LD, PORTED SSOP	DOCUMENT NO: 98ARH99089A	REV: C
	CASE NUMBER: 1317A-03	24 MAY 2005
	STANDARD: NON-JEDEC	

PAGE 1 OF 2

CASE 1317A-03
ISSUE C
SUPER SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .006 INCHES PER SIDE.
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5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 INCHES MAXIMUM.

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	CASE NUMBER: 1317A–03	24 MAY 2005
	STANDARD: NON–JEDEC	

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CASE 1317A-03
ISSUE C
SUPER SMALL OUTLINE PACKAGE

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