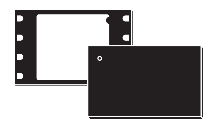
M25PX64

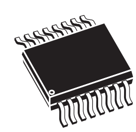
64-Mbit, dual I/O, 4-Kbyte subsector erase, serial flash memory with 75 MHz SPI bus interface

Features

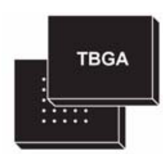
- SPI bus compatible serial interface
- 75 MHz (maximum) clock frequency
- 2.7 V to 3.6 V single supply voltage
- Dual input/output instructions resulting in an equivalent clock frequency of 150 MHz:
  – Dual output fast read instruction
  – Dual input fast program instruction
- Whole memory continuously read by sending once a fast read or a dual output fast read instruction and an address
- 64 Mbit Flash memory
  – Uniform 4-Kbyte subsectors
  – Uniform 64-Kbyte sectors
- Additional 64-byte user-lockable, one-time programmable (OTP) area
- Erase capability
  – Subsector (4-Kbyte) granularity
  – Sector (64-Kbyte) granularity
  – Bulk erase (64 Mbits) in 68 s (typical)
- Write protections
  – Software write protection applicable to every 64-Kbyte sector (volatile lock bit)
  – Hardware write protection: protected area size defined by three non-volatile bits (BP0, BP1 and BP2)
- Deep power-down mode: 5 µA (typical)
- Electronic signature
  – JEDEC standard two-byte signature (7117h)
  – Unique ID code (UID) with 16 bytes read-only, available upon customer request
- More than 100 000 write cycles per sector
- More than 20 years data retention
- Packages
  – RoHS compliant



VDFPN8 (ME)
8 × 6 mm (MLP8)



SO16 (MF)
300 mils width



TBGA24 (ZM) 6x8 mm

- Automotive Certified Parts Available

Contents

List of tables

List of figures

1 Description

The M25PX64 is a 64-Mbit (8 Mbits x 8) serial flash memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

The M25PX64 supports two new, high-performance dual input/output instructions:

- Dual output fast read (DOFR) instruction used to read data at up to 75 MHz by using both pin DQ1 and pin DQ0 as outputs
- Dual input fast program (DIFP) instruction used to program data at up to 75 MHz by using both pin DQ1 and pin DQ0 as inputs

These new instructions double the transfer bandwidth for read and program operations.

The memory can be programmed 1 to 256 bytes at a time, using the page program instruction.

The memory is organized as 128 sectors that are further divided into 16 subsectors each (2048 subsectors in total).

The memory can be erased a 4-Kbyte subsector at a time, a 64-Kbyte sector at a time, or as a whole. It can be write protected by software using a mix of volatile and non-volatile protection features, depending on the application needs. The protection granularity is of 64 Kbytes (sector granularity).

The M25PX64 has 64 one-time-programmable bytes (OTP bytes) that can be read and programmed using two dedicated instructions, Read OTP (ROTP) and Program OTP (POTP), respectively. These 64 bytes can be permanently locked by a particular program OTP (POTP) sequence. Once they have been locked, they become read-only and this state cannot be reverted.

Further features are available as additional security options. More information on these security features is available, upon completion of an NDA (nondisclosure agreement), and are, therefore, not described in this datasheet. For more details of this option contact your nearest Numonyx sales office.

Figure 1. Logic diagram

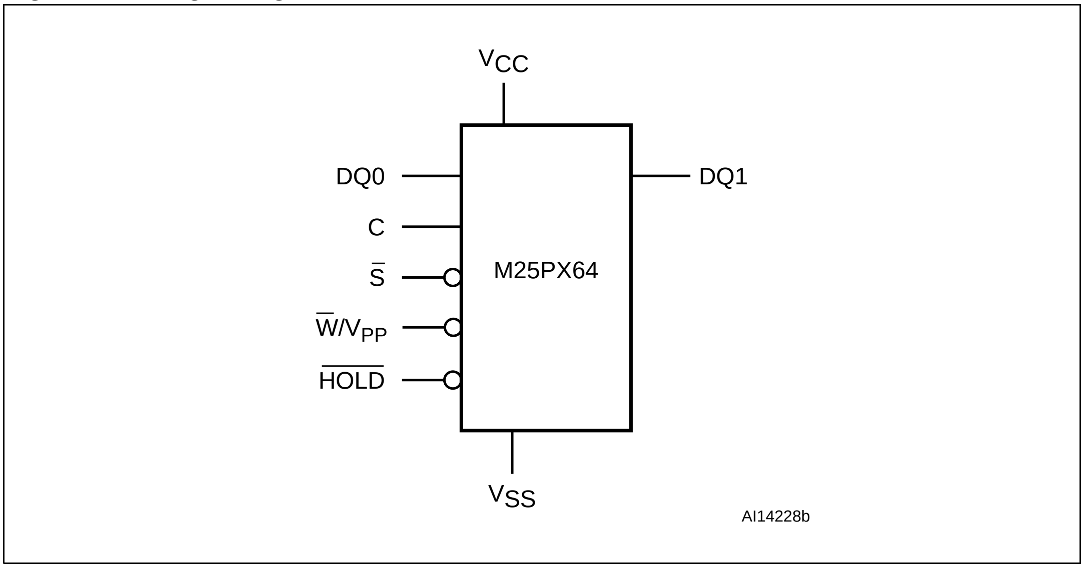
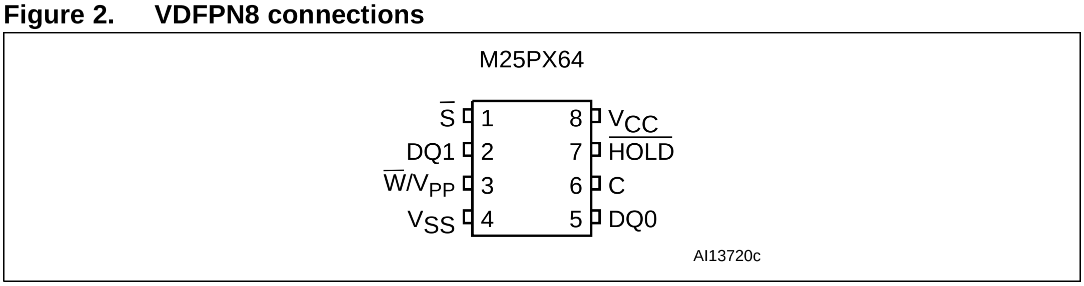


Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
DQ0	Serial Data input	I/O(1)
DQ1	Serial Data output	I/O(2)
$\overline{S}$	Chip Select	Input
$\overline{W}/V_{PP}$	Write Protect/Enhanced Program supply voltage	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	–
V_{SS}	Ground	–

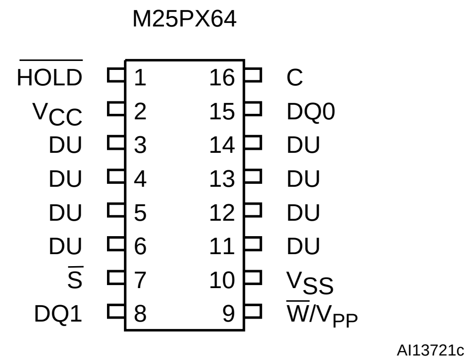
1. Serves as an output during dual output fast read (DOFR) instructions.
2. Serves as an input during dual input fast program (DIFP) instructions.

Figure 2. VDFPN8 connections



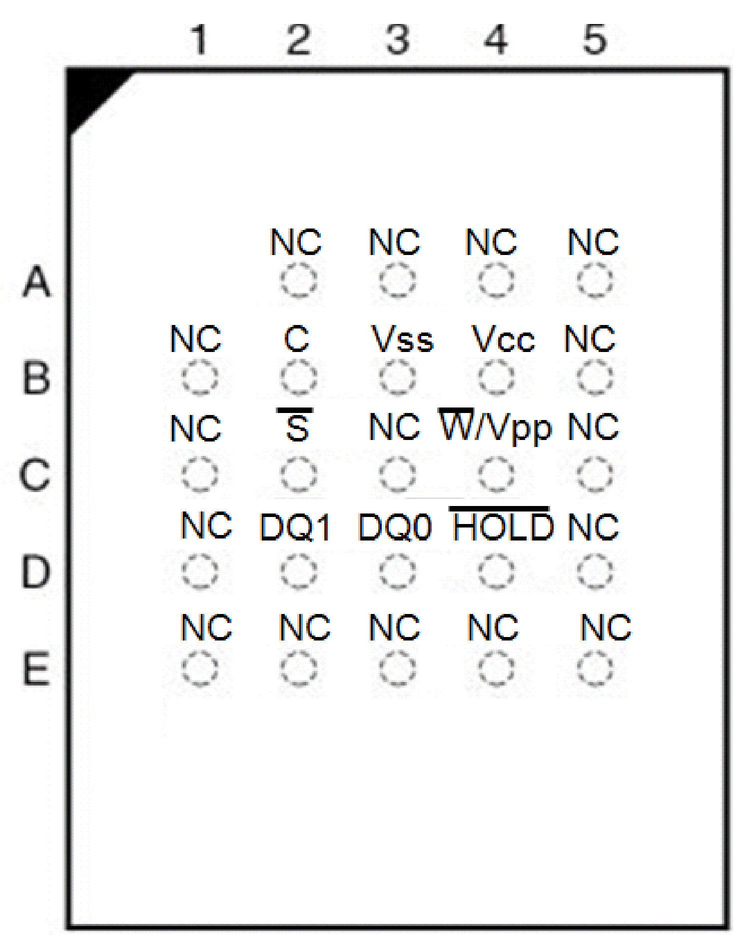
1. There is an exposed central pad on the underside of the VDFPN8 package. This is pulled, internally, to V_{SS}, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See *Package mechanical* section for package dimensions, and how to identify pin-1.

Figure 3. SO16 connections



1. DU = don't use.
2. See *Package mechanical* section for package dimensions, and how to identify pin-1.

Figure 4. BGA 6x8 24 ball ballout



Note: 1 NC = No Connection

2 See Section 11: Package mechanical.

2 Signal descriptions

2.1 Serial data output (DQ1)

This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of Serial Clock (C).

During the dual input fast program (DIFP) instruction, pin DQ1 is used as an input. It is latched on the rising edge of the Serial Clock (C).

2.2 Serial data input (DQ0)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

During the dual output fast read (DOFR) instruction, pin DQ0 is used as an output. Data are shifted out on the falling edge of the Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at serial data input (DQ0) are latched on the rising edge of Serial Clock (C). Data on serial data output (DQ1) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and serial data output (DQ1) is at high impedance. Unless an internal program, erase or write status register cycle is in progress, the device will be in the standby power mode (this is not the deep power-down mode). Driving Chip Select ($\overline{S}$) Low enables the device, placing it in the active power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the hold condition, the serial data output (DQ1) is high impedance, and serial data input (DQ0) and Serial Clock (C) are don't care.

To start the hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.

2.6 Write protect/enhanced program supply voltage ($\overline{W}/V_{PP}$)

$\overline{W}/V_{PP}$ is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If the $\overline{W}/V_{PP}$ input is kept in a low voltage range (0 V to V_{CC}) the pin is seen as a control input. This input signal is used to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP2, BP1 and BP0 bits of the status register. See *Table 9*).

If V_{PP} is in the range of V_{PPH} (as defined in *Table 15*) it acts as an additional power supply.[1]

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

---

1. Avoid applying V_{PPH} to the $\overline{W}$/VPP pin during Bulk Erase.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

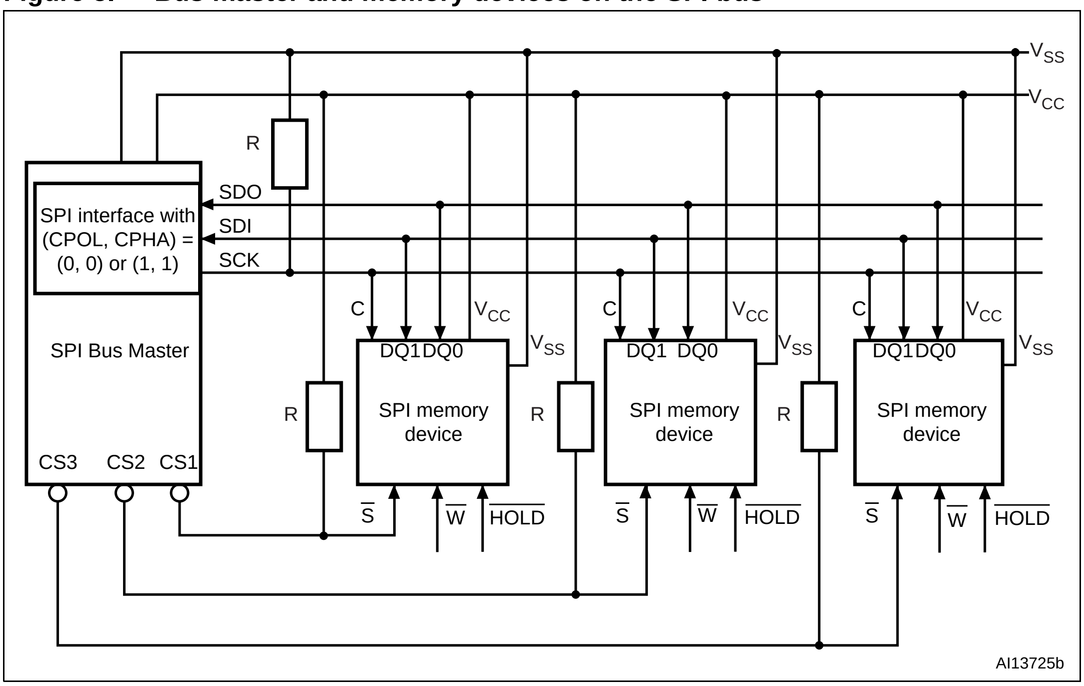
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 6*, is the clock polarity when the bus master is in standby mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 5. Bus master and memory devices on the SPI bus

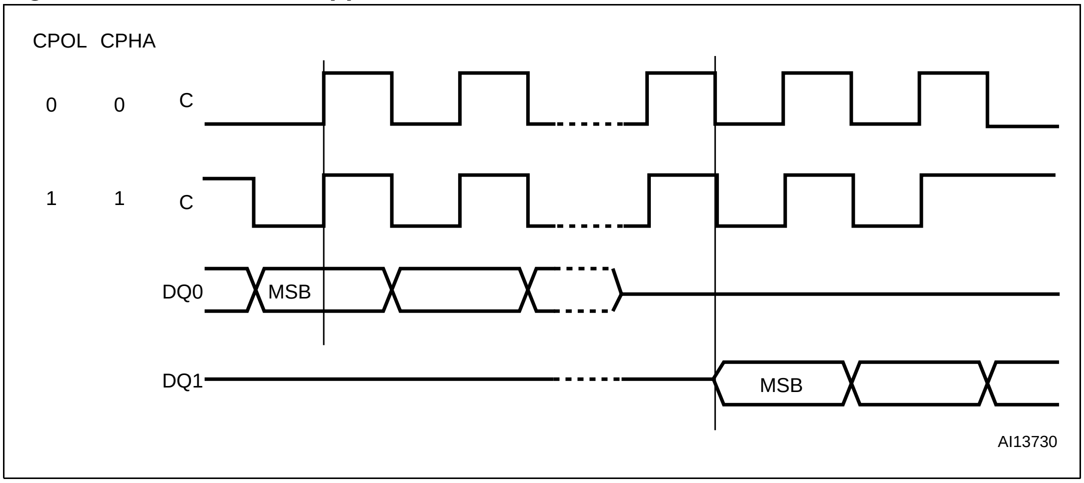


1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

Figure 5 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the serial data output (DQ1) line at a time, the other devices are high impedance. Resistors R (represented in *Figure 5*) ensure that the M25PX64 is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state. As the bus master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the bus master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the $\overline{S}$ line is pulled High while the C line is pulled Low (thus ensuring that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met). The typical value of R is 100 kΩ, assuming that the time constant R*C_p (C_p = parasitic capacitance of the bus line) is shorter than the time during which the bus master leaves the SPI bus in high impedance.

Example: C_p = 50 pF, that is $R*C_p$ = 5 µs <=> the application must ensure that the bus master never leaves the SPI bus in the high impedance state for a time period shorter than 5 µs.

Figure 6. SPI modes supported



4 Operating features

4.1 Page programming

To program one data byte, two instructions are required: write enable (WREN), which is one byte, and a page program (PP) sequence, which consists of four bytes plus data. This is followed by the internal program cycle (of duration t_{PP}).

To spread this overhead, the page program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from ‘1’ to ‘0’), provided that they lie in consecutive addresses on the same page of memory.

For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Page program (PP)* and *Table 18: AC characteristics*).

4.2 Dual input fast program

The dual input fast program (DIFP) instruction makes it possible to program up to 256 bytes using two input pins at the same time (by changing bits from ‘1’ to ‘0’).

For optimized timings, it is recommended to use the dual input fast program (DIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several dual input fast program (DIFP) sequences each containing only a few bytes (see *Section 6.12: Dual input fast program (DIFP)*).

4.3 Subsector erase, sector erase and bulk erase

The page program (PP) instruction allows bits to be reset from ‘1’ to ’0’. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a subsector at a time, using the subsector erase (SSE) instruction, a sector at a time, using the sector erase (SE) instruction, or throughout the entire memory, using the bulk erase (BE) instruction. This starts an internal erase cycle (of duration t_{SSE}, t_{SE} or t_{BE}).

The erase instruction must be preceded by a write enable (WREN) instruction.

4.4 Polling during a write, program or erase cycle

A further improvement in the time to write status register (WRSR), program OTP (POTP), program (PP), dual input fast program (DIFP) or erase (SSE, SE or BE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SSE}, t_{SE}, or t_{BE}). The write in progress (WIP) bit is provided in the status register so that the application program can monitor its value, polling it to establish when the previous write cycle, program cycle or erase cycle is complete.

4.5 Active power, standby power and deep power-down modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the active power mode.

When Chip Select ($\overline{S}$) is High, the device is deselected, but could remain in the active power mode until all internal cycles have completed (program, erase, write status register). The device then goes in to the standby power mode. The device consumption drops to I_{CC1}.

The deep power-down mode is entered when the specific instruction (the deep power-down (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the release from deep power-down (RDP) instruction) is executed.

While in the deep power-down mode, the device ignores all write, program and erase instructions (see *Section 6.18: Deep power-down (DP)*), this can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent write, program or erase instructions.

4.6 Status register

The status register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.4: Read status register (RDSR)* for a detailed description of the status register bits.

4.7 Protection modes

There are protocol-related and specific hardware and software protection modes. They are described below.

4.7.1 Protocol-related protections

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M25PX64 features the following data protection mechanisms:

- Power on reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification
- Program, erase and write status register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution
- All instructions that modify data must be preceded by a write enable (WREN) instruction to set the write enable latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write disable (WRDI) instruction completion
  - Write status register (WRSR) instruction completion
  - Write to lock register (WRLR) instruction completion
  - Program OTP (POTP) instruction completion
  - Page program (PP) instruction completion
  - Dual input fast program (DIFP) instruction completion
  - Subsector erase (SSE) instruction completion
  - Sector erase (SE) instruction completion
  - Bulk erase (BE) instruction completion
- In addition to the low power consumption feature, the deep power-down mode offers extra software protection, as all write, program and erase instructions are ignored.

4.7.2 Specific hardware and software protection

There are two software protected modes, SPM1 and SPM2, that can be combined to protect the memory array as required. The SPM2 can be locked by hardware with the help of the $\overline{W}$ input pin.

SPM1 and SPM2

- The first software protected mode (SPM1) is managed by specific lock registers assigned to each 64-Kbyte sector.

  The lock registers can be read and written using the read lock register (RDLR) and write to lock register (WRLR) instructions.

  In each lock register two bits control the protection of each sector: the write lock bit and the lock down bit.

  – Write lock bit:

    The write lock bit determines whether the contents of the sector can be modified (using the write, program or erase instructions). When the write lock bit is set to '1', the sector is write protected – any operations that attempt to change the data in the sector will fail. When the write lock bit is reset to '0', the sector is not write protected by the lock register, and may be modified.

  – Lock down bit:

    The lock down bit provides a mechanism for protecting software data from simple hacking and malicious attack. When the lock down bit is set to '1', further modification to the write lock and lock down bits cannot be performed. A power-up is required before changes to these bits can be made. When the lock down bit is reset to '0', the write lock and lock down bits can be changed.

  The definition of the lock register bits is given in *Table 9: Lock register out*.

Table 2. Software protection truth table (sectors 0 to 127, 64-Kbyte granularity)

Sector lock register		Protection status
Lock down bit	Write lock bit	
0	0	Sector unprotected from program/erase/write operations, protection status reversible
0	1	Sector protected from program/erase/write operations, protection status reversible
1	0	Sector unprotected from program/erase/write operations, Sector protection status cannot be changed except by a power-up.
1	1	Sector protected from program/erase/write operations, Sector protection status cannot be changed except by a power-up.

- the second software protected mode (SPM2) uses the block protect bits (see *Section 6.4.3: BP2, BP1, BP0 bits*) and the top/bottom bit (see *Section 6.4.4: Top/bottom bit*) to allow part of the memory to be configured as read-only.

Table 3. Protected area sizes

Status register contents				Memory content	
TB bit	BP bit 2	BP bit 1	BP bit 0	Protected area	Unprotected area
0	0	0	0	none	All sectors(1) (128 sectors: 0 to 127)
0	0	0	1	Upper 64th (2 sectors: 126 and 127)	Lower 63/64ths (126 sectors: 0 to 125)
0	0	1	0	Upper 32nd (4 sectors: 124 to 127)	Lower 31/32nds (124 sectors: 0 to 123)
0	0	1	1	Upper 16th (8 sectors: 120 to 127)	Lower 15/16ths (120 sectors: 0 to 119)
0	1	0	0	Upper 8th (16 sectors: 56 to 63)	Lower 7/8ths (112 sectors: 0 to 111)
0	1	0	1	Upper quarter (32 sectors: 96 to 127)	Lower three-quarters (96 sectors: 0 to 95)
0	1	1	0	Upper half (64 sectors: 64 to 127)	Lower half (64 sectors: 0 to 63)
0	1	1	1	All sectors (128 sectors: 0 to 127)	none
1	0	0	0	none	All sectors(1) (128 sectors: 0 to 128)
1	0	0	1	Lower 64th (2 sectors: 0 to1)	Upper 63/64ths (126 sectors: 2 to 127)
1	0	1	0	Lower 32nd (4 sectors: 0 to 3)	Upper 31/32nds (124 sectors: 4 to 127)
1	0	1	1	Lower 16th (8 sectors: 0 to 7)	Upper 15/16ths (120 sectors: 8 to 127)
1	1	0	0	Lower 8th (16 sectors: 0 to15)	Upper 7/8ths (112 sectors: 16 to 127)
1	1	0	1	Lower 4th (32 sectors: 0 to 31)	Upper 3/4ths (96 sectors: 32 to 127)
1	1	1	0	Lower half (64 sectors: 0 to 63)	Upper half (64 sectors: 64 to 127)
1	1	1	1	All sectors (128 sectors: 0 to 127)	none

1. The device is ready to accept a bulk erase instruction if, and only if, all block protect (BP2, BP1, BP0) are 0.

As a second level of protection, the Write Protect signal (applied on the $\overline{W}/V_{PP}$ pin) can freeze the status register in a read-only mode. In this mode, the block protect bits (BP2, BP1, BP0) and the status register write disable bit (SRWD) are protected. For more details, see *Section 6.5: Write status register (WRSR)*.

4.8 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any write status register, program or erase cycle that is currently in progress.

To enter the hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

The hold condition starts on the falling edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low (as shown in *Figure 7*).

The hold condition ends on the rising edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low.

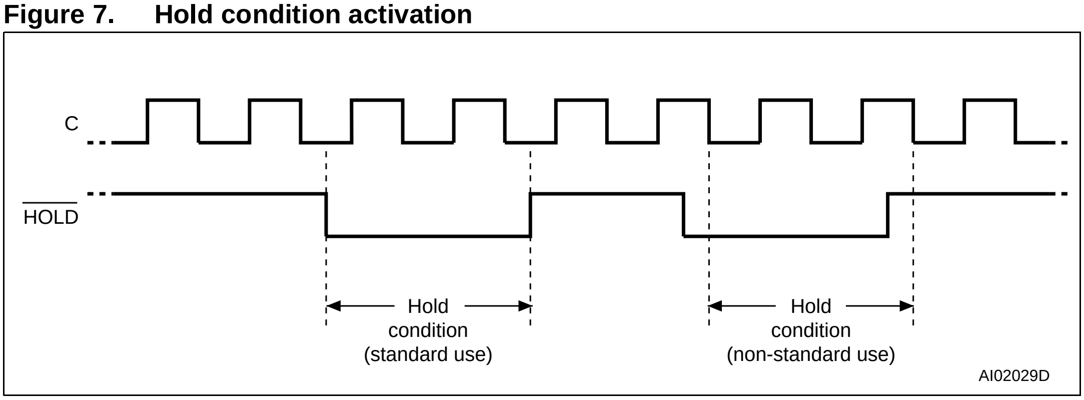
If the falling edge does not coincide with Serial Clock (C) being Low, the hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the hold condition ends after Serial Clock (C) next goes Low (this is shown in *Figure 7*).

During the hold condition, the serial data output (DQ1) is high impedance, and serial data input (DQ0) and Serial Clock (C) are don't care.

Normally, the device is kept selected, with Chip Select ($\overline{S}$) driven Low, for the whole duration of the hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the hold condition.

If Chip Select ($\overline{S}$) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ($\overline{HOLD}$) High, and then to drive Chip Select ($\overline{S}$) Low. This prevents the device from going back to the hold condition.

Figure 7. Hold condition activation



5 Memory organization

The memory is organized as:

- 8 388 608 bytes (8 bits each)
- 2048 subsectors (4 Kbytes each)
- 128 sectors (64 Kbytes each)
- 32768 pages (256 bytes each)
- 64 OTP bytes located outside the main memory array.

Each page can be individually programmed (bits are programmed from ‘1’ to ‘0’). The device is subsector, sector or bulk erasable (bits are erased from ‘0’ to ‘1’) but not page erasable.

Figure 8. Block diagram

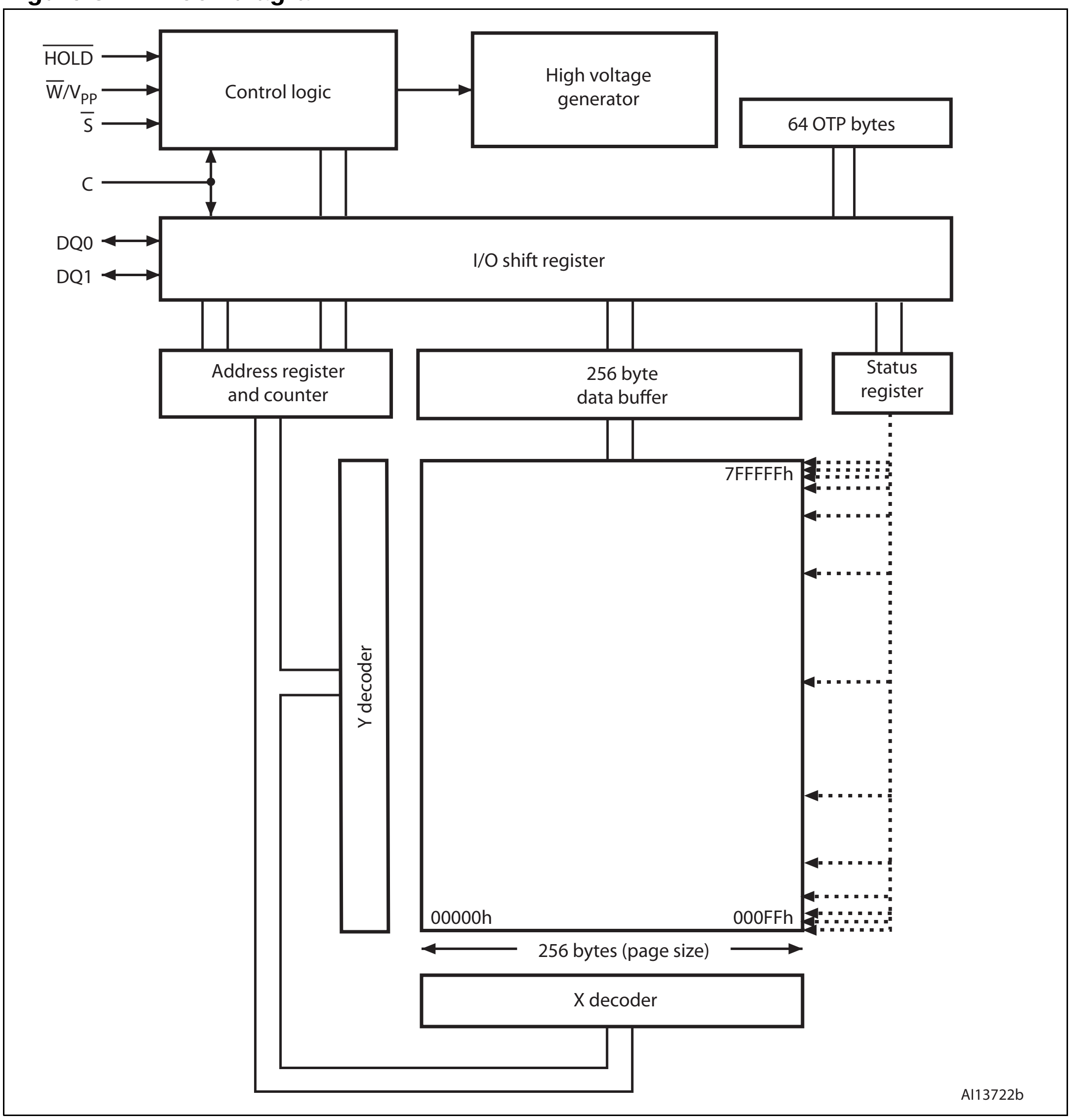


Table 4. Memory organization

Sector	Subsector	Address range	
	2047	7FF000h	7FFFFFh
127	⋮	⋮	⋮
	2032	7F0000h	7F0FFFh
	2031	7EF000h	7EFFFFh
126	⋮	⋮	⋮
	2016	7E0000h	7E0FFFh
	2015	7DF000h	7DFFFFh
125	⋮	⋮	⋮
	2000	7D0000h	7D0FFFh
	1999	7CF000h	7CFFFFh
124	⋮	⋮	⋮
	1984	7C0000h	7C0FFFh
	1983	7BF000h	7BFFFFh
123	⋮	⋮	⋮
	1968	7B0000h	7B0FFFh
	1967	7AF000h	7AFFFFh
122	⋮	⋮	⋮
	1952	7A0000h	7A0FFFh
	1951	79F000h	79FFFFh
121	⋮	⋮	⋮
	1936	790000h	790FFFh
	1935	78F000h	78FFFFh
120	⋮	⋮	⋮
	1920	780000h	780FFFh
	1919	77F000h	77FFFFh
119	⋮	⋮	⋮
	1904	770000h	770FFFh
	1903	76F000h	76FFFFh
118	⋮	⋮	⋮
	1888	760000h	760FFFh
	1887	75F000h	75FFFFh
117	⋮	⋮	⋮
	1872	750000h	750FFFh
	1871	74F000h	74FFFFh
116	⋮	⋮	⋮
	1856	740000h	740FFFh
	1855	73F000h	73FFFFh
115	⋮	⋮	⋮
	1840	730000h	730FFFh
	1839	72F000h	72FFFFh
114	⋮	⋮	⋮
	1824	720000h	720FFFh
	1823	71F000h	71FFFFh
113	⋮	⋮	⋮
	1808	710000h	710FFFh
	1807	70F000h	70FFFFh
112	⋮	⋮	⋮
	1792	700000h	700FFFh
	1791	6FF000h	6FFFFFh
111	⋮	⋮	⋮
	1776	6F0000h	6F0FFFh
	1775	6EF000h	6EFFFFh
110	⋮	⋮	⋮
	1760	6E0000h	6E0FFFh
	1759	6DF000h	6DFFFFh
109	⋮	⋮	⋮
	1744	6D0000h	6D0FFFh
	1743	6CF000h	6CFFFFh
108	⋮	⋮	⋮
	1728	6C0000h	6C0FFFh
	1727	6BF000h	6BFFFFh
107	⋮	⋮	⋮
	1712	6B0000h	6B0FFFh
	1711	6AF000h	6AFFFFh
106	⋮	⋮	⋮
	1696	6A0000h	6A0FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range	
105	1695	69F000h	69FFFFh
	⋮	⋮	⋮
	1680	690000h	690FFFh
104	1679	68F000h	68FFFFh
	⋮	⋮	⋮
	1664	680000h	680FFFh
103	1663	67F000h	67FFFFh
	⋮	⋮	⋮
	1648	670000h	670FFFh
102	1647	66F000h	66FFFFh
	⋮	⋮	⋮
	1632	660000h	660FFFh
101	1631	65F000h	65FFFFh
	⋮	⋮	⋮
	1616	650000h	650FFFh
100	1615	64F000h	64FFFFh
	⋮	⋮	⋮
	1600	640000h	640FFFh
99	1599	63F000h	63FFFFh
	⋮	⋮	⋮
	1584	630000h	630FFFh
98	1583	62F000h	62FFFFh
	⋮	⋮	⋮
	1568	620000h	620FFFh
97	1567	61F000h	61FFFFh
	⋮	⋮	⋮
	1552	610000h	610FFFh
96	1551	60F000h	60FFFFh
	⋮	⋮	⋮
	1536	600000h	600FFFh
95	1535	5FF000h	5FFFFFh
	⋮	⋮	⋮
	1520	5F0000h	5F0FFFh

Sector	Subsector	Address range	
94	1519	5EF000h	5EFFFFh
	⋮	⋮	⋮
	1504	5E0000h	5E0FFFh
93	1503	5DF000h	5DFFFFh
	⋮	⋮	⋮
	464	5D0000h	5D0FFFh
92	1487	5CF000h	5CFFFFh
	⋮	⋮	⋮
	1472	5C0000h	5C0FFFh
91	1471	5BF000h	5BFFFFh
	⋮	⋮	⋮
	1456	5B0000h	5B0FFFh
90	1455	5AF000h	5AFFFFh
	⋮	⋮	⋮
	1440	5A0000h	5A0FFFh
89	1439	59F000h	59FFFFh
	⋮	⋮	⋮
	1424	590000h	590FFFh
88	1423	58F000h	58FFFFh
	⋮	⋮	⋮
	1408	580000h	580FFFh
87	1407	57F000h	57FFFFh
	⋮	⋮	⋮
	1392	570000h	570FFFh
86	1391	56F000h	56FFFFh
	⋮	⋮	⋮
	1376	560000h	560FFFh
85	1375	55F000h	55FFFFh
	⋮	⋮	⋮
	1360	550000h	550FFFh
84	1359	54F000h	54FFFFh
	⋮	⋮	⋮
	1344	540000h	540FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range	
	1343	53F000h	53FFFFh
83	⋮	⋮	⋮
	1328	530000h	530FFFh
	1327	52F000h	52FFFFh
82	⋮	⋮	⋮
	1312	520000h	520FFFh
	1311	51F000h	51FFFFh
81	⋮	⋮	⋮
	1296	510000h	510FFFh
	1295	50F000h	50FFFFh
80	⋮	⋮	⋮
	1280	500000h	500FFFh
	1279	4FF000h	4FFFFFh
79	⋮	⋮	⋮
	1264	4F0000h	4F0FFFh
	1263	4EF000h	4EFFFFh
78	⋮	⋮	⋮
	1248	4E0000h	4E0FFFh
	1247	4DF000h	4DFFFFh
77	⋮	⋮	⋮
	1232	4D0000h	4D0FFFh
	1231	4CF000h	4CFFFFh
76	⋮	⋮	⋮
	1216	4C0000h	4C0FFFh
	1215	4BF000h	4BFFFFh
75	⋮	⋮	⋮
	1200	4B0000h	4B0FFFh
	1199	4AF000h	4AFFFFh
74			
	1184	4A0000h	4A0FFFh
	1183	49F000h	49FFFFh
73	⋮	⋮	⋮
	1168	490000h	490FFFh

Sector	Subsector	Address range	
	1167	48F000h	48FFFFh
72	⋮	⋮	⋮
	1152	480000h	480FFFh
	1151	47F000h	47FFFFh
71	⋮	⋮	⋮
	1136	470000h	470FFFh
	1135	46F000h	46FFFFh
70	⋮	⋮	⋮
	1120	460000h	460FFFh
	1119	45F000h	45FFFFh
69	⋮	⋮	⋮
	1104	450000h	450FFFh
	1103	44F000h	44FFFFh
68	⋮	⋮	⋮
	1088	440000h	440FFFh
	1087	43F000h	43FFFFh
67	⋮	⋮	⋮
	1072	430000h	430FFFh
	1071	42F000h	42FFFFh
66	⋮	⋮	⋮
	1056	420000h	420FFFh
	1055	41F000h	41FFFFh
65	⋮	⋮	⋮
	1040	410000h	410FFFh
	1039	40F000h	40FFFFh
64	⋮	⋮	⋮
	1024	400000h	400FFFh
	1023	3FF000h	3FF000h
63	⋮	⋮	⋮
	1008	3F0000h	3F0FFFh
	1007	3EF000h	3EFFFFh
62	⋮	⋮	⋮
	992	3E0000h	3E0FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range		Sector	Subsector	Address range	
61	991	3DF000h	3DFFFFh	50	815	32F000h	32FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	976	3D0000h	3D0FFFh		800	320000h	320FFFh
60	975	3CF000h	3CFFFFh	49	799	31F000h	31FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	960	3C0000h	3C0FFFh		784	310000h	310FFFh
59	959	3BF000h	3BFFFFh	48	783	30F000h	30FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	944	3B0000h	3B0FFFh		768	300000h	300FFFh
58	943	3AF000g	3AFFFFh	47	767	2FF000h	2FFFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	928	3A0000h	3A0FFFh		752	2F0000h	2F0FFFh
57	927	39F000h	39FFFFh	46	751	2EF000h	2EFFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	912	390000h	390FFFh		736	2E0000h	2E0FFFh
56	911	38F000h	38FFFFh	45	735	2DF000h	2DFFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	896	380000h	380FFFh		720	2D0000h	2D0FFFh
55	895	37F000h	37FFFFh	44	719	2CF000h	2CFFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	880	370000h	370FFFh		704	2C0000h	2C0FFFh
54	879	36F000h	36FFFFh	43	703	2BF000h	2BFFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	864	360000h	360FFFh		688	2B0000h	2B0FFFh
53	863	35F000h	35FFFFh	42	687	2AF000h	2AFFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	848	350000h	350FFFh		672	2A0000h	2A0FFFh
52	847	34F000h	34FFFFh	41	671	29F000h	29FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	832	340000h	340FFFh		656	290000h	290FFFh
51	831	33F000h	33FFFFh	40	655	28F000h	28FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	816	330000h	330FFFh		640	280000h	280FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range		Sector	Subsector	Address range	
39	639	27F000h	27FFFFh	28	463	1CF000h	1CFFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	624	270000h	270FFFh		448	1C0000h	1C0FFFh
38	623	26F000h	26FFFFh	27	447	1BF000h	1BFFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	608	260000h	260FFFh		432	1B0000h	1B0FFFh
37	607	25F000h	25FFFFh	26	431	1AF000h	1AFFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	592	250000h	250FFFh		416	1A0000h	1A0FFFh
36	591	24F000h	24FFFFh	25	415	19F000h	19FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	576	240000h	240FFFh		400	190000h	190FFFh
35	575	23F000h	23FFFFh	24	399	18F000h	18FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	560	230000h	230FFFh		384	180000h	180FFFh
34	559	22F000h	22FFFFh	23	383	17F000h	17FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	544	220000h	220FFFh		368	170000h	170FFFh
33	543	21F000h	21FFFFh	22	367	16F000h	16FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	528	210000h	210FFFh		352	160000h	160FFFh
32	527	20F000h	20FFFFh	21	351	15F000h	15FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	512	200000h	200FFFh		336	150000h	150FFFh
31	511	1FF000h	1FFFFFh	20	335	14F000h	14FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	496	1F0000h	1F0FFFh		320	140000h	140FFFh
30	495	1EF000h	1EFFFFh	19	319	13F000h	13FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	480	1E0000h	1E0FFFh		304	130000h	130FFFh
29	479	1DF000h	1DFFFFh	18	303	12F000h	12FFFFh
	⋮	⋮	⋮		⋮	⋮	⋮
	464	1D0000h	1D0FFFh		288	120000h	120FFFh

Table 4. Memory organization (continued)

Sector	Subsector	Address range	
17	287	11F000h	11FFFFh
	⋮	⋮	⋮
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	⋮	⋮	⋮
	256	100000h	100FFFh
15	255	FF000h	FFFFFh
	⋮	⋮	⋮
	240	F0000h	F0FFFh
14	239	EF000h	EFFFFh
	⋮	⋮	⋮
	224	E0000h	E0FFFh
13	223	DF000h	DFFFFh
	⋮	⋮	⋮
	208	D0000h	D0FFFh
12	207	CF000h	CFFFFh
	⋮	⋮	⋮
	192	C0000h	C0FFFh
11	191	BF000h	BFFFFh
	⋮	⋮	⋮
	176	B0000h	B0FFFh
10	175	AF000h	AFFFFh
	160	A0000h	A0FFFh
9	159	9F000h	9FFFFh
	⋮	⋮	⋮
	144	90000h	90FFFh
8	143	8F000h	8FFFFh
	⋮	⋮	⋮
	128	80000h	80FFFh
7	127	7F000h	7FFFFh
	⋮	⋮	⋮
	112	70000h	70FFFh
6	111	6F000h	6FFFFh
	⋮	⋮	⋮
	96	60000h	60FFFh
5	95	5F000h	5FFFFh
	⋮	⋮	⋮
	80	50000h	50FFFh
4	79	4F000h	4FFFFh
	⋮	⋮	⋮
	64	40000h	40FFFh
3	63	3F000h	3FFFFh
	⋮	⋮	⋮
	48	30000h	30FFFh
2	47	2F000h	2FFFFh
	⋮	⋮	⋮
	32	20000h	20FFFh
1	31	1F000h	1FFFFh
	⋮	⋮	⋮
	16	10000h	10FFFh
0	15	0F000h	0FFFFh
	⋮	⋮	⋮
	4	04000h	04FFFh
	3	03000h	03FFFh
	2	02000h	02FFFh
	1	01000h	01FFFh
	0	00000h	00FFFh

6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial data input(s) DQ0 (DQ1) is (are) sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on serial data input(s) DQ0 (DQ1), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in *Table 5*.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a read data bytes (READ), read data bytes at higher speed (FAST_READ), dual output fast read (DOFR), read OTP (ROTP), read lock registers (RDLR), read status register (RDSR), read identification (RDID) or release from deep power-down (RDP) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a page program (PP), program OTP (POTP), dual input fast program (DIFP), subsector erase (SSE), sector erase (SE), bulk erase (BE), write status register (WRSR), write to lock register (WRLR), write enable (WREN), write disable (WRDI) or deep power-down (DP) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a write status register cycle, program cycle or erase cycle are ignored, and the internal write status register cycle, program cycle or erase cycle continues unaffected.

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Table 5. Instruction set

Instruction	Description	One-byte instruction code		Address bytes	Dummy bytes	Data bytes
WREN	Write enable	0000 0110	06h	0	0	0
WRDI	Write disable	0000 0100	04h	0	0	0
RDID	Read identification	1001 1111	9Fh	0	0	1 to 20
		1001 1110	9Eh	0	0	1 to 3
RDSR	Read status register	0000 0101	05h	0	0	1 to ∞
WRSR	Write status register	0000 0001	01h	0	0	1
WRLR	Write to lock register	1110 0101	E5h	3	0	1
RDLR	Read lock register	1110 1000	E8h	3	0	1
READ	Read data bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read data bytes at higher speed	0000 1011	0Bh	3	1	1 to ∞
DOFR	Dual output fast read	0011 1011	3Bh	3	1	1 to ∞
ROTP	Read OTP (read 64 bytes of OTP area)	0100 1011	4Bh	3	1	1 to 65
POTP	Program OTP (program 64 bytes of OTP area)	0100 0010	42h	3	0	1 to 65
PP	Page program	0000 0010	02h	3	0	1 to 256
DIFP	Dual input fast program	1010 0010	A2h	3	0	1 to 256
SSE	Subsector erase	0010 0000	20h	3	0	0
SE	Sector erase	1101 1000	D8h	3	0	0
BE	Bulk erase	1100 0111	C7h	0	0	0
DP	Deep power-down	1011 1001	B9h	0	0	0
RDP	Release from deep power-down	1010 1011	ABh	0	0	0

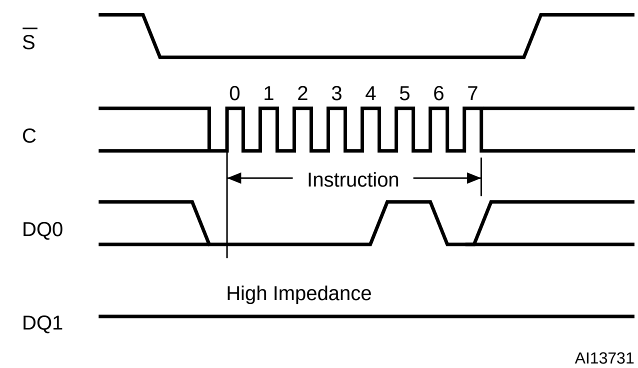
6.1 Write enable (WREN)

The write enable (WREN) instruction (*Figure 9*) sets the write enable latch (WEL) bit.

The write enable latch (WEL) bit must be set prior to every page program (PP), dual input fast program (DIFP), program OTP (POTP), write to lock register (WRLR), subsector erase (SSE), sector erase (SE), bulk erase (BE) and write status register (WRSR) instruction.

The write enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 9. Write enable (WREN) instruction sequence



6.2 Write disable (WRDI)

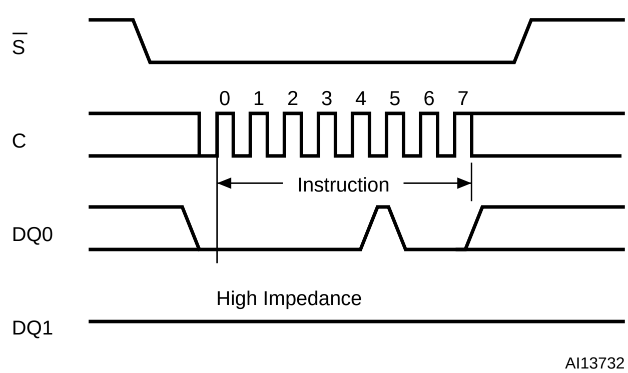
The write disable (WRDI) instruction (*Figure 10*) resets the write enable latch (WEL) bit.

The write disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

The write enable latch (WEL) bit is reset under the following conditions:

- Power-up
- Write disable (WRDI) instruction completion
- Write status register (WRSR) instruction completion
- Write to lock register (WRLR) instruction completion
- Page program (PP) instruction completion
- Dual input fast program (DIFP) instruction completion
- Program OTP (POTP) instruction completion
- Subsector erase (SSE) instruction completion
- Sector erase (SE) instruction completion
- Bulk erase (BE) instruction completion

Figure 10. Write disable (WRDI) instruction sequence



6.3 Read identification (RDID)

The read identification (RDID) instruction allows to read the device identification data:

- Manufacturer identification (1 byte)
- Device identification (2 bytes)
- A unique ID code (UID) (17 bytes, of which 16 available upon customer request).

The manufacturer identification is assigned by JEDEC, and has the value 20h for Numonyx. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (71h), and the memory capacity of the device in the second byte (17h). The UID contains the length of the following data in the first byte (set to 10h) and 16 bytes of the optional customized factory data (CFD) content. The CFD bytes are read-only and can be programmed with customers data upon their demand. If the customers do not make requests, the devices are shipped with all the CFD bytes programmed to zero (00h).

Any read identification (RDID) instruction while an erase or program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The read identification (RDID) instruction should not be issued while the device is in deep power-down mode.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. After this, the 24-bit device identification, stored in the memory, the 8-bit CFD length followed by 16 bytes of CFD content will be shifted out on serial data output (DQ1). Each bit is shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 11*.

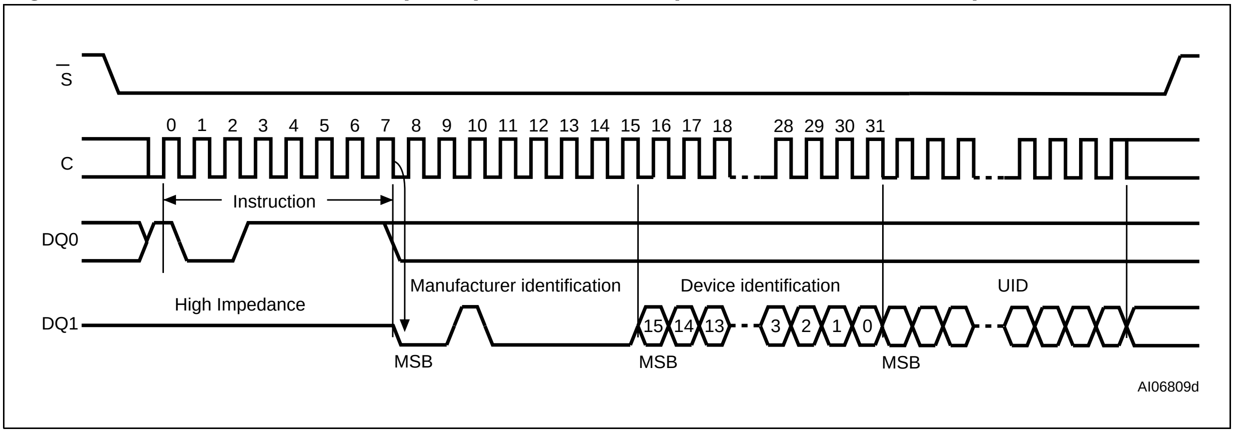
The read identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the standby power mode. Once in the standby power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 6. Read identification (RDID) data-out sequence

Manufacturer identification	Device identification		UID	
	Memory type	Memory capacity	CFD length	CFD content
20h	71h	17h	10h	16 bytes

Figure 11. Read identification (RDID) instruction sequence and data-out sequence



6.4 Read status register (RDSR)

The read status register (RDSR) instruction allows the status register to be read. The status register may be read at any time, even while a program, erase or write status register cycle is in progress. When one of these cycles is in progress, it is recommended to check the write in progress (WIP) bit before sending a new instruction to the device. It is also possible to read the status register continuously, as shown in *Figure 12*.

Table 7. Status register format

b7							b0
SRWD	0	TB	BP2	BP1	BP0	WEL	WIP

Status register write protect

Top/bottom bit

Block protect bits

Write enable latch bit

Write in progress bit

The status and control bits of the status register are as follows:

6.4.1 WIP bit

The write in progress (WIP) bit indicates whether the memory is busy with a write status register, program or erase cycle. When set to ‘1’, such a cycle is in progress, when reset to ‘0’ no such cycle is in progress.

6.4.2 WEL bit

The write enable latch (WEL) bit indicates the status of the internal write enable latch. When set to ‘1’ the internal write enable latch is set, when set to ‘0’ the internal write enable latch is reset and no write status register, program or erase instruction is accepted.

6.4.3 BP2, BP1, BP0 bits

The block protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against program and erase instructions. These bits are written with the write status register (WRSR) instruction. When one or more of the block protect (BP2, BP1, BP0) bits is set to ‘1’, the relevant memory area (as defined in *Table 3*) becomes protected against page program (PP) and sector erase (SE) instructions. The block protect (BP2, BP1, BP0) bits can be written provided that the hardware protected mode has not been set. The bulk erase (BE) instruction is executed if, and only if, all block protect (BP2, BP1, BP0) bits are 0.

6.4.4 Top/bottom bit

The top/bottom (TB) bit is non-volatile. It can be set and reset with the write status register (WRSR) instruction provided that the write enable (WREN) instruction has been issued. The top/bottom (TB) bit is used in conjunction with the block protect (BP0, BP1, BP2) bits to determine if the protected area defined by the block protect bits starts from the top or the bottom of the memory array:

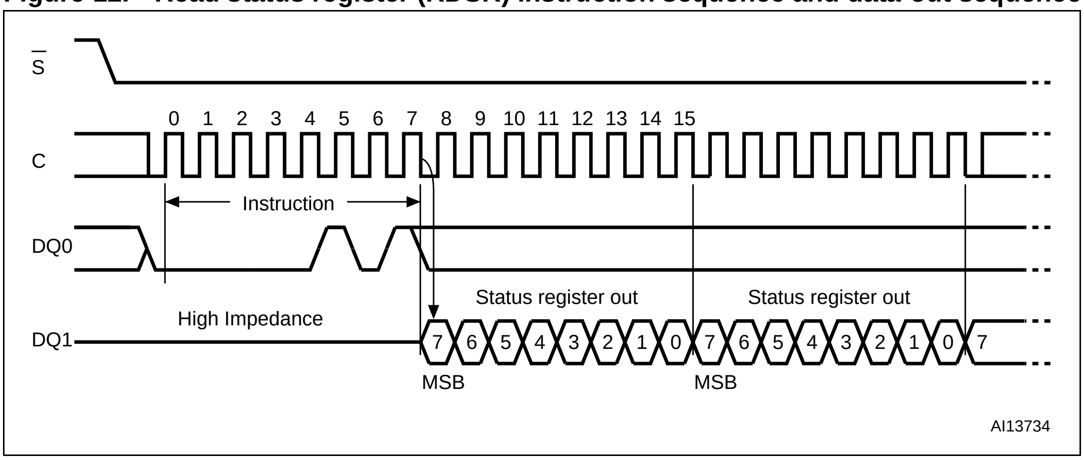
- When top/bottom bit is reset to ‘0’ (default value), the area protected by the block protect bits starts from the top of the memory array (see *Table 3: Protected area sizes*)
- When top/bottom bit is set to ‘1’, the area protected by the block protect bits starts from the bottom of the memory array (see *Table 3: Protected area sizes*).

The top/bottom bit cannot be written when the SRWD bit is set to ‘1’ and the $\overline{W}$ pin is driven Low.

6.4.5 SRWD bit

The status register write disable (SRWD) bit is operated in conjunction with the write protect ($\overline{W}/V_{PP}$) signal. The status register write disable (SRWD) bit and the write protect ($\overline{W}/V_{PP}$) signal allow the device to be put in the hardware protected mode (when the status register write disable (SRWD) bit is set to ‘1’, and write protect ($\overline{W}/V_{PP}$) is driven Low). In this mode, the non-volatile bits of the status register (SRWD, BP2, BP1, BP0) become read-only bits and the write status register (WRSR) instruction is no longer accepted for execution.

Figure 12. Read status register (RDSR) instruction sequence and data-out sequence



6.5 Write status register (WRSR)

The write status register (WRSR) instruction allows new values to be written to the status register. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded and executed, the device sets the write enable latch (WEL).

The write status register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code and the data byte on serial data input (DQ0).

The instruction sequence is shown in *Figure 13*.

The write status register (WRSR) instruction has no effect on b6, b1 and b0 of the status register. b6 is always read as '0'.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the data byte has been latched in. If not, the write status register (WRSR) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed write status register cycle (whose duration is t_W) is initiated. While the write status register cycle is in progress, the status register may still be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed write status register cycle, and is 0 when it is completed. When the cycle is completed, the write enable latch (WEL) is reset.

The write status register (WRSR) instruction allows the user to change the values of the block protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in *Table 3*. The write status register (WRSR) instruction also allows the user to set and reset the status register write disable (SRWD) bit in accordance with the Write Protect ($\overline{W}/V_{PP}$) signal. The status register write disable (SRWD) bit and Write Protect ($\overline{W}/V_{PP}$) signal allow the device to be put in the hardware protected mode (HPM). The write status register (WRSR) instruction is not executed once the hardware protected mode (HPM) is entered.

Figure 13. Write status register (WRSR) instruction sequence

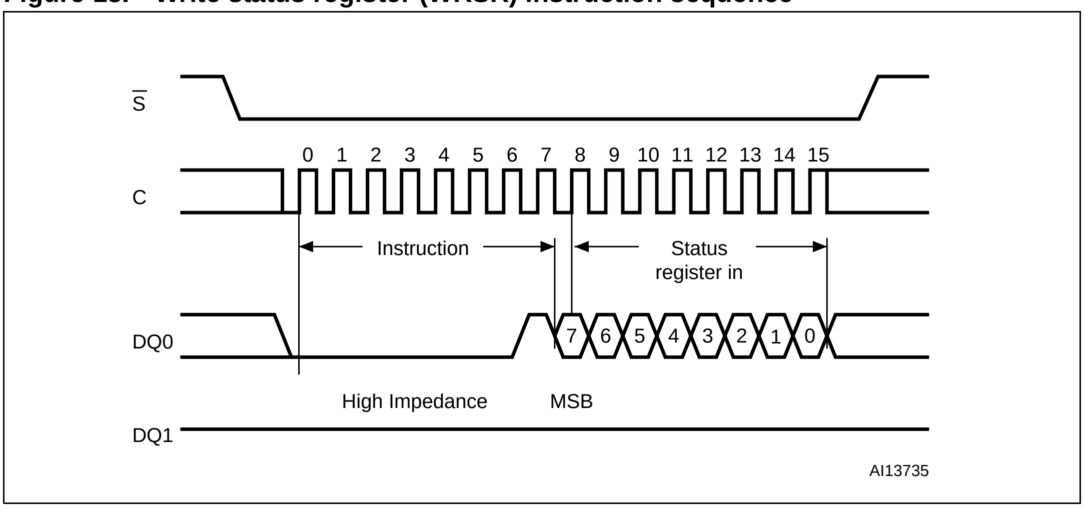


Table 8. Protection modes

$\overline{W}/V_{PP}$ signal	SRWD bit	Mode	Write protection of the status register	Memory content	
				Protected area[(1)]	Unprotected area[(1)]
1	0	Software protected (SPM)	Status register is writable (if the WREN instruction has set the WEL bit) The values in the SRWD, BP2, BP1 and BP0 bits can be changed	Protected against page program, sector erase and bulk erase	Ready to accept page program and sector erase instructions
0	0				
1	1				
0	1	Hardware protected (HPM)	Status register is hardware write protected The values in the SRWD, BP2, BP1 and BP0 bits cannot be changed	Protected against page program, sector erase and bulk erase	Ready to accept page program and sector erase instructions

1. As defined by the values in the block protect (BP2, BP1, BP0) bits of the status register, as shown in *Table 3*.

The protection features of the device are summarized in *Table 8*.

When the status register write disable (SRWD) bit of the status register is 0 (its initial delivery state), it is possible to write to the status register provided that the write enable latch (WEL) bit has previously been set by a write enable (WREN) instruction, regardless of the whether Write Protect ($\overline{W}/V_{PP}$) is driven High or Low.

When the status register write disable (SRWD) bit of the status register is set to ‘1’, two cases need to be considered, depending on the state of Write Protect ($\overline{W}/V_{PP}$):

- If Write Protect ($\overline{W}/V_{PP}$) is driven High, it is possible to write to the status register provided that the write enable latch (WEL) bit has previously been set by a write enable (WREN) instruction.
- If write protect ($\overline{W}/V_{PP}$) is driven Low, it is not possible to write to the status register even if the write enable latch (WEL) bit has previously been set by a write enable (WREN) instruction (attempts to write to the status register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the block protect (BP2, BP1, BP0) bits of the status register, are also hardware protected against data modification.

Regardless of the order of the two events, the hardware protected mode (HPM) can be entered:

- by setting the status register write disable (SRWD) bit after driving Write Protect ($\overline{W}/V_{PP}$) Low
- or by driving Write Protect ($\overline{W}/V_{PP}$) Low after setting the status register write disable (SRWD) bit.

The only way to exit the hardware protected mode (HPM) once entered is to pull Write Protect ($\overline{W}/V_{PP}$) High.

If Write Protect ($\overline{W}/V_{PP}$) is permanently tied High, the hardware protected mode (HPM) can never be activated, and only the software protected mode (SPM), using the block protect (BP2, BP1, BP0) bits of the status register, can be used.

6.6 Read data bytes (READ)

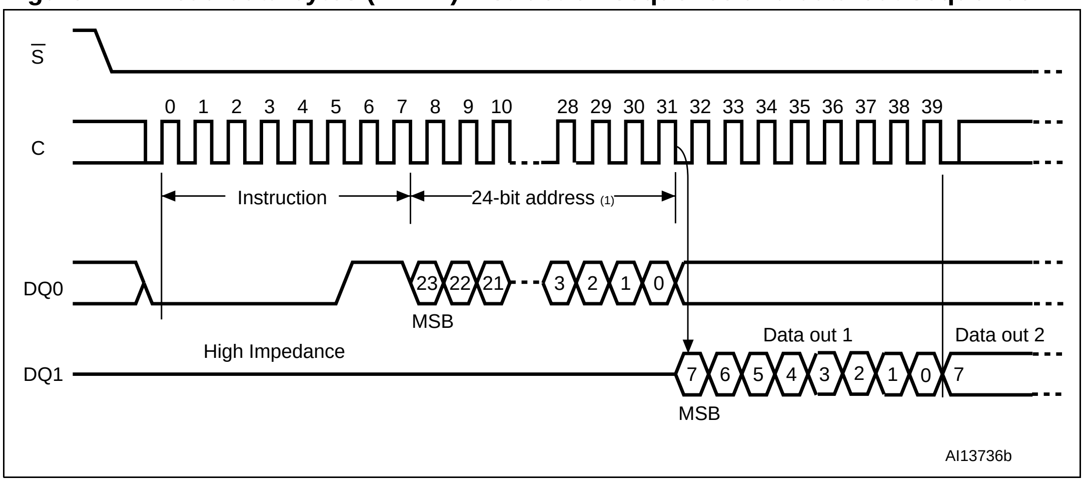
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read data bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on serial data output (DQ1), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 14*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single read data bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The read data bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any read data bytes (READ) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 14. Read data bytes (READ) instruction sequence and data-out sequence



1. Address bit A23 is don't care.

6.7 Read data bytes at higher speed (FAST_READ)

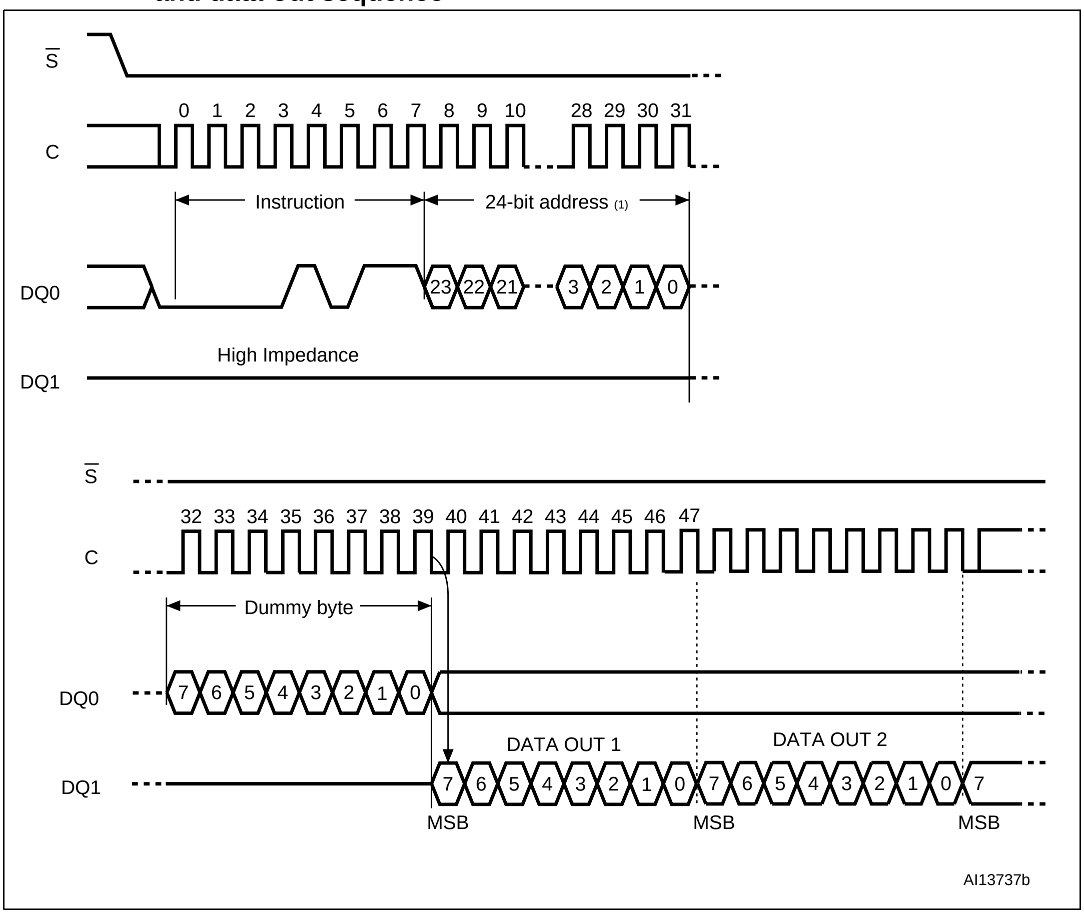
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read data bytes at higher speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, are shifted out on serial data output (DQ1) at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 15*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single read data bytes at higher speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The read data bytes at higher speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any read data bytes at higher speed (FAST_READ) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 15. Read data bytes at higher speed (FAST_READ) instruction sequence and data-out sequence



1. Address bit A23 is don't care.

6.8 Dual output fast read (DOFR)

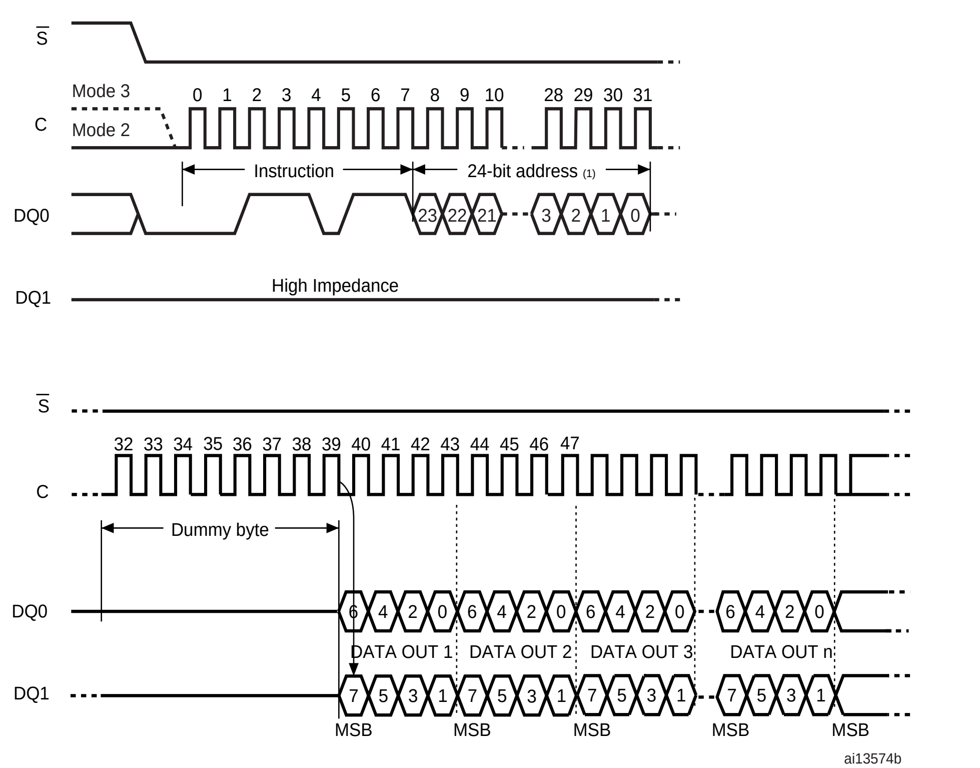
The dual output fast read (DOFR) instruction is very similar to the read data bytes at higher speed (FAST_READ) instruction, except that the data are shifted out on two pins (pin DQ0 and pin DQ1) instead of only one. Outputting the data on two pins instead of one doubles the data transfer bandwidth compared to the read data bytes at higher speed (FAST_READ) instruction.

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the dual output fast read instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, are shifted out on DQ0 and DQ1 at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 16*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out on DQ0 and DQ1. The whole memory can, therefore, be read with a single dual output fast read (DOFR) instruction. When the highest address is reached, the address counter rolls over to 00 0000h, so that the read sequence can be continued indefinitely.

Figure 16. Dual output fast read instruction sequence



1. Address bit A23 is don't care.

6.9 Read lock register (RDLR)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read lock register (RDLR) instruction is followed by a 3-byte address (A23-A0) pointing to any location inside the concerned sector. Each address bit is latched-in during the rising edge of Serial Clock (C). Then the value of the lock register is shifted out on serial data output (DQ1), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 17*.

The read lock register (RDLR) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

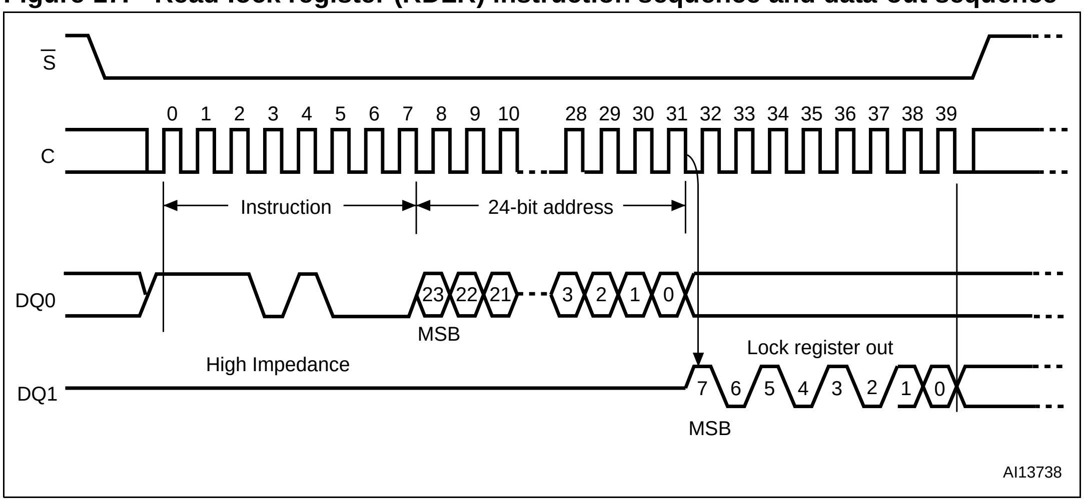
Any read lock register (RDLR) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Table 9. Lock register out(1)

Bit	Bit name	Value	Function
b7-b2	Reserved		
b1	Sector lock down	'1'	The write lock and lock down bits cannot be changed. Once a '1' is written to the lock down bit it cannot be cleared to '0', except by a power-up.
		'0'	The write lock and lock down bits can be changed by writing new values to them.
b0	Sector write lock	'1'	Write, program and erase operations in this sector will not be executed. The memory contents will not be changed.
		'0'	Write, program and erase operations in this sector are executed and will modify the sector contents.

1. Values of (b1, b0) after power-up are defined in *Section 7: Power-up and power-down*.

Figure 17. Read lock register (RDLR) instruction sequence and data-out sequence



6.10 Read OTP (ROTP)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read OTP (ROTP) instruction is followed by a 3-byte address (A23- A0) and a dummy byte. Each bit is latched in on the rising edge of Serial Clock (C).

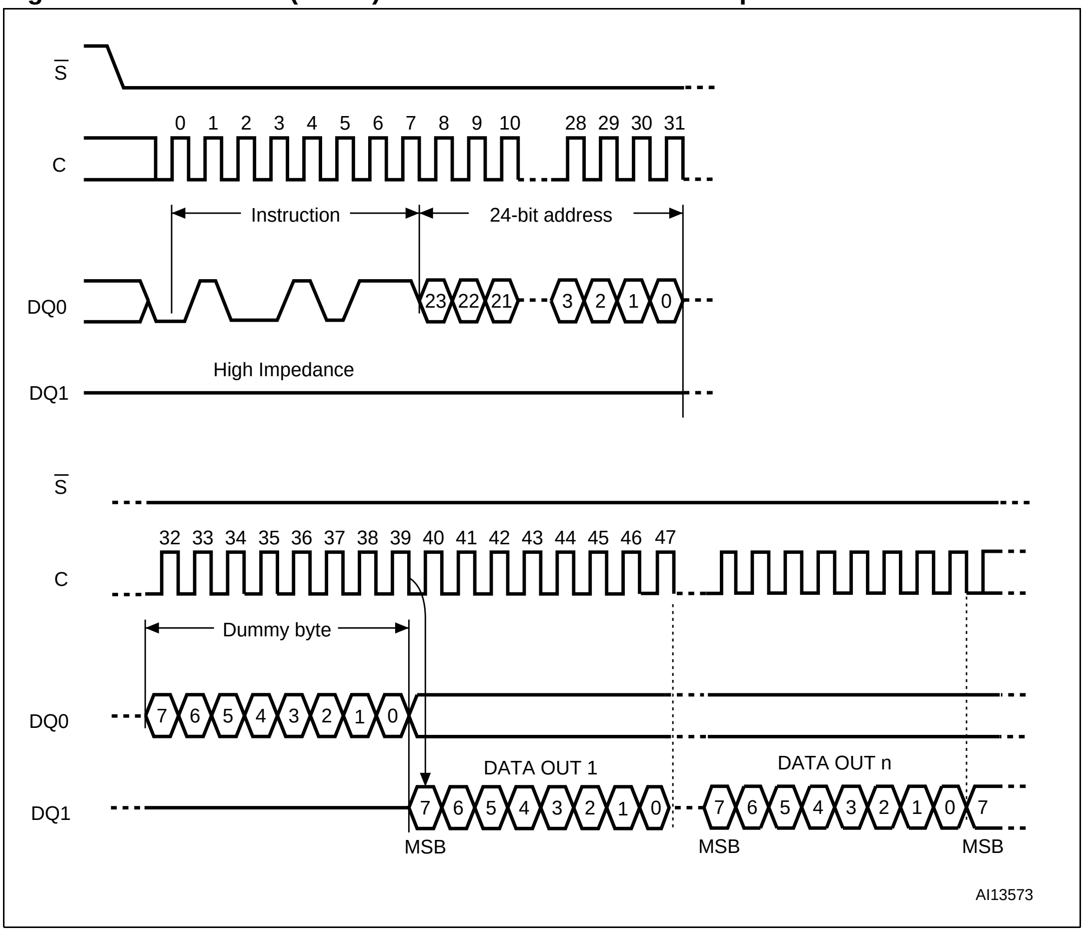
Then the memory contents at that address are shifted out on serial data output (DQ1). Each bit is shifted out at the maximum frequency, $f_C$max, on the falling edge of Serial Clock (C). The instruction sequence is shown in *Figure 18*.

The address is automatically incremented to the next higher address after each byte of data is shifted out.

There is no rollover mechanism with the read OTP (ROTP) instruction. This means that the read OTP (ROTP) instruction must be sent with a maximum of 65 bytes to read, since once the 65th byte has been read, the same (65th) byte keeps being read on the DQ1 pin.

The read OTP (ROTP) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any read OTP (ROTP) instruction issued while an erase, program or write cycle is in progress, is rejected without having any effect on the cycle that is in progress.

Figure 18. Read OTP (ROTP) instruction and data-out sequence



1. A23 to A7 are don't care.
2. $1 \leq n \leq 65$.

6.11 Page program (PP)

The page program (PP) instruction allows bytes to be programmed in the memory (changing bits from ‘1’ to ‘0’). Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

The page program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on serial data input (DQ0). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 19*.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

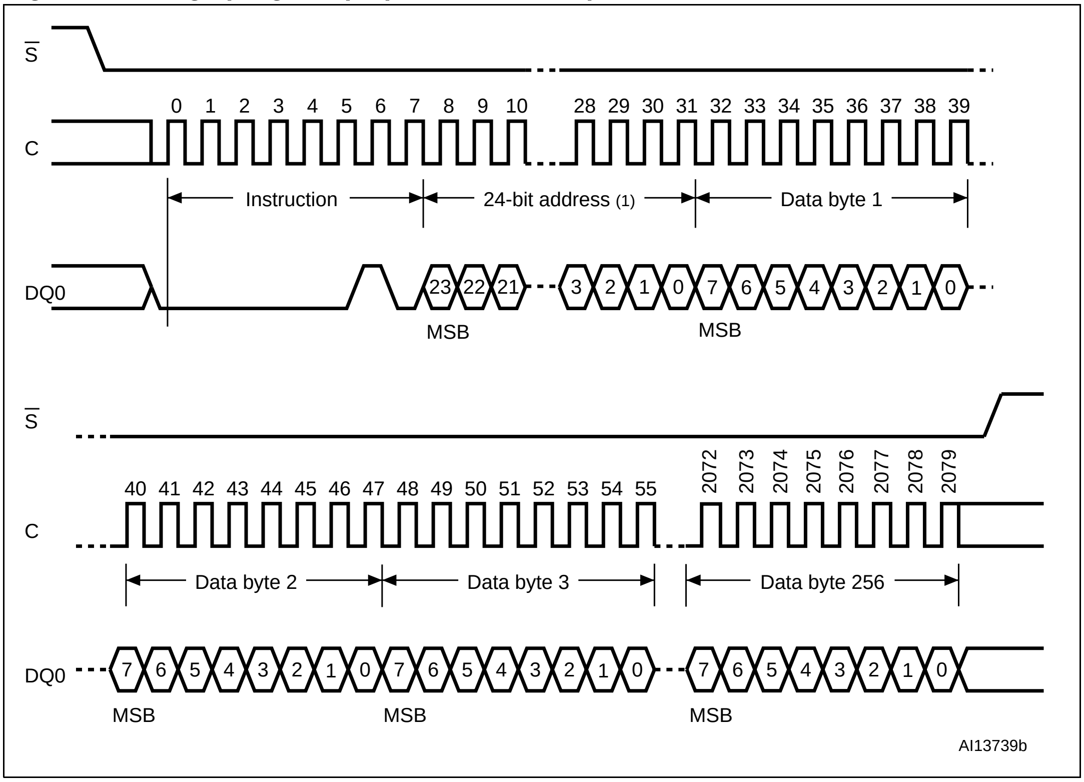
For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Table 18: AC characteristics*).

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the page program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page program cycle (whose duration is t_{PP}) is initiated. While the page program cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed page program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset.

A page program (PP) instruction applied to a page which is protected by the block protect (BP2, BP1, BP0) bits (see *Table 3* and *Table 4*) is not executed.

Figure 19. Page program (PP) instruction sequence



1. Address bit A23 is don't care.

6.12 Dual input fast program (DIFP)

The dual input fast program (DIFP) instruction is very similar to the page program (PP) instruction, except that the data are entered on two pins (pin DQ0 and pin DQ1) instead of only one. Inputting the data on two pins instead of one doubles the data transfer bandwidth compared to the page program (PP) instruction.

The dual input fast program (DIFP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on serial data input (DQ0).

If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 20*.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes in the same page.

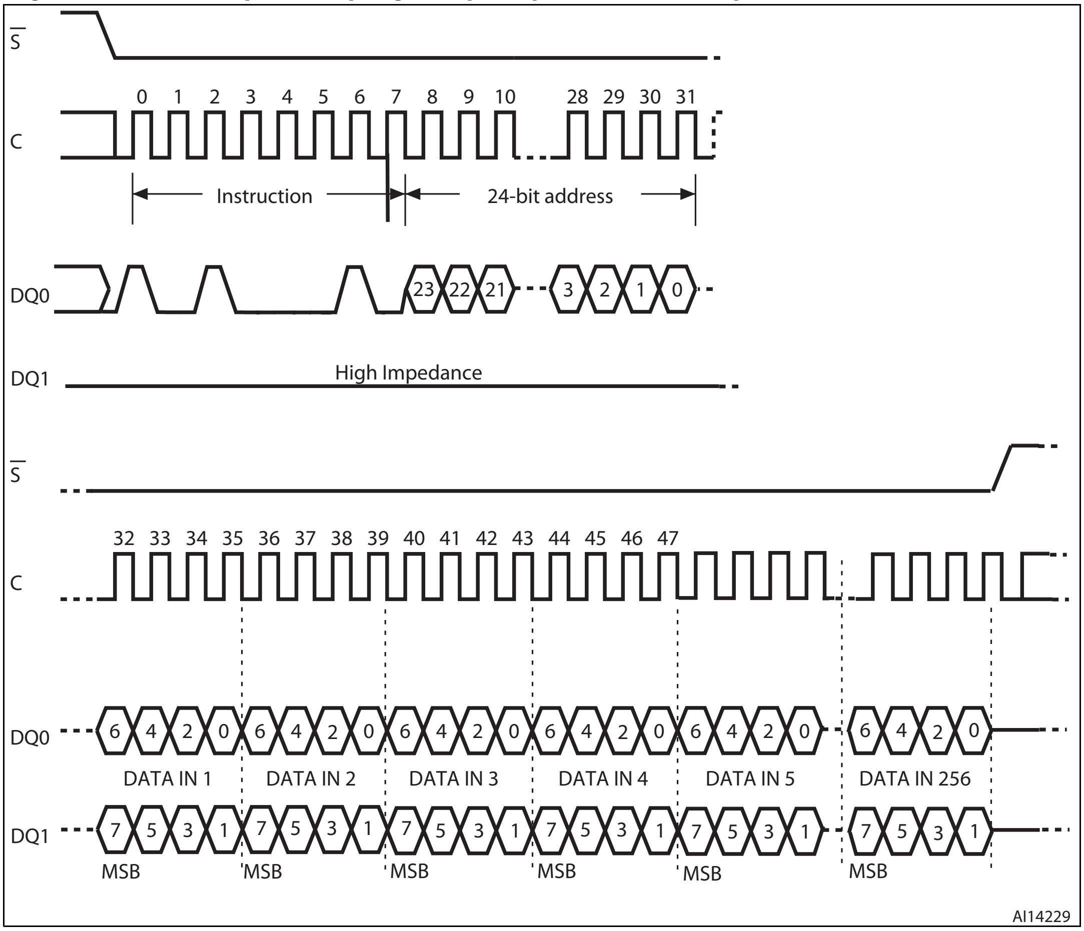
For optimized timings, it is recommended to use the dual input fast program (DIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several dual input fast program (DIFP) sequences each containing only a few bytes (see *Table 18: AC characteristics*).

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the dual input fast program (DIFP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page program cycle (whose duration is t_{PP}) is initiated. While the dual input fast program (DIFP) cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed page program cycle, and 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset.

A dual input fast program (DIFP) instruction applied to a page that is protected by the block protect (BP2, BP1, BP0) bits (see *Table 2* and *Table 3*) is not executed.

Figure 20. Dual input fast program (DIFP) instruction sequence



1. Address bit A23 is don’t care.

6.13 Program OTP instruction (POTP)

The program OTP instruction (POTP) is used to program at most 64 bytes to the OTP memory area (by changing bits from ‘1’ to ‘0’, only). Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL) bit.

The program OTP instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction opcode, three address bytes and at least one data byte on serial data input (DQ0).

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the program OTP instruction is not executed.

There is no rollover mechanism with the program OTP (POTP) instruction. This means that the program OTP (POTP) instruction must be sent with a maximum of 65 bytes to program, once all 65 bytes have been latched in, any following byte will be discarded.

The instruction sequence is shown in *Figure 21*.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page program cycle (whose duration is t_{PP}) is initiated. While the program OTP cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed program OTP cycle, and it is 0 when it is completed. At some unspecified time before the cycle is complete, the write enable latch (WEL) bit is reset.

To lock the OTP memory:

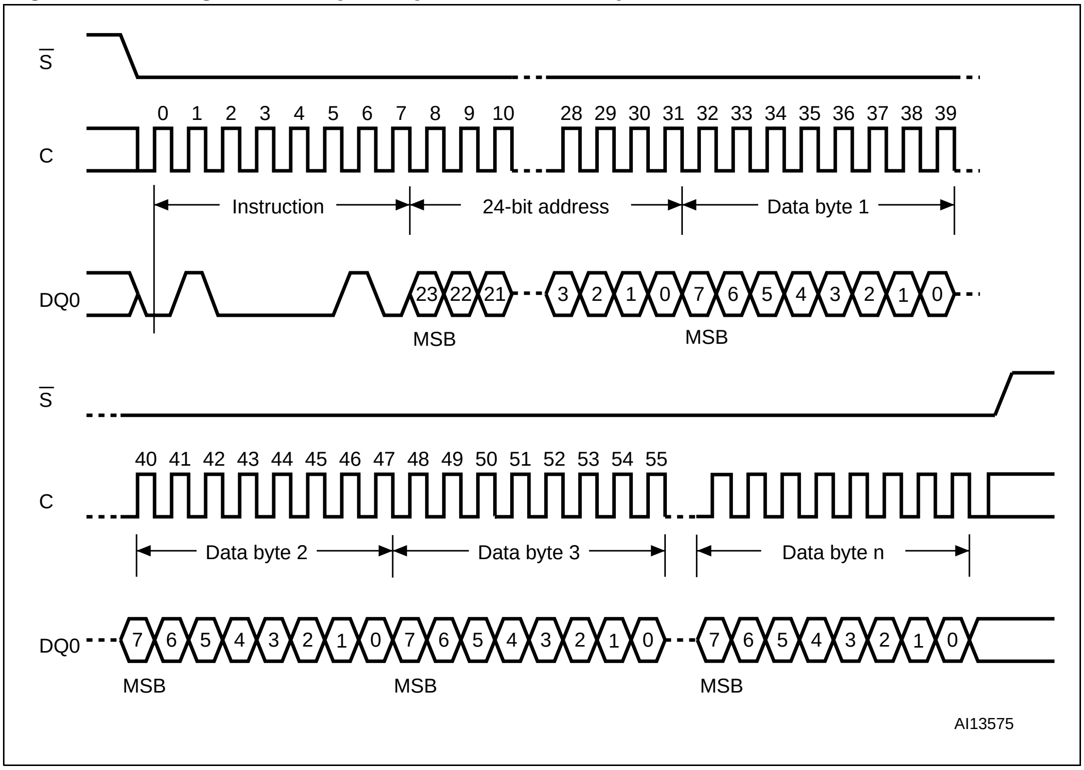
Bit 0 of the OTP control byte, that is byte 64, (see *Figure 22*) is used to permanently lock the OTP memory array.

- When bit 0 of byte 64 = ’1’, the 64 bytes of the OTP memory array can be programmed.
- When bit 0 of byte 64 = ‘0’, the 64 bytes of the OTP memory array are read-only and cannot be programmed anymore.

Once a bit of the OTP memory has been programmed to ‘0’, it can no longer be set to ‘1’. Therefore, as soon as bit 0 of byte 64 (control byte) is set to ‘0’, the 64 bytes of the OTP memory array become read-only in a permanent way.

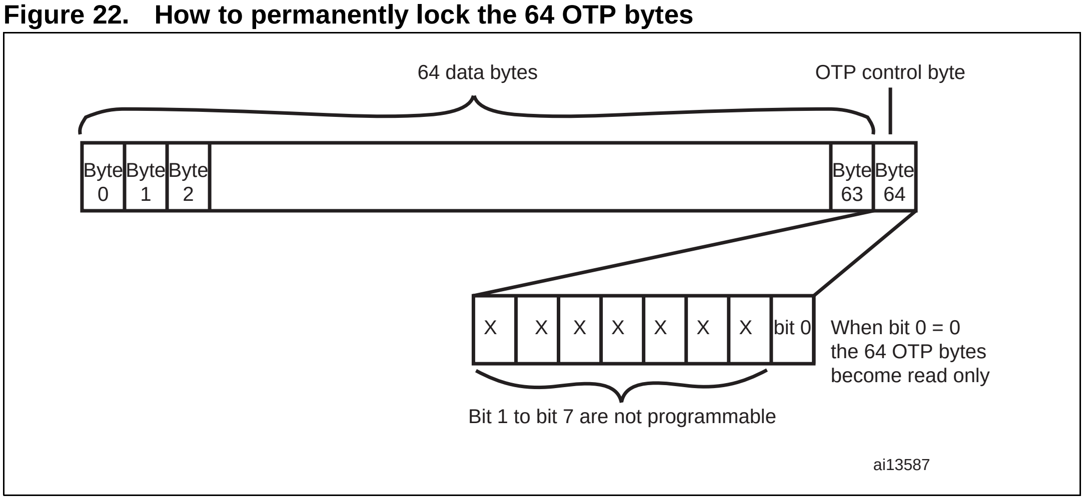
Any program OTP (POTP) instruction issued while an erase, program or write cycle is in progress is rejected without having any effect on the cycle that is in progress.

Figure 21. Program OTP (POTP) instruction sequence



1. A23 to A7 are don't care.
2. 1 ≤ n ≤ 65.

Figure 22. How to permanently lock the 64 OTP bytes



6.14 Write to lock register (WRLR)

The write to lock register (WRLR) instruction allows bits to be changed in the lock registers. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

The write to lock register (WRLR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes (pointing to any address in the targeted sector and one data byte on serial data input (DQ0). The instruction sequence is shown in *Figure 23*. Chip Select ($\overline{S}$) must be driven High after the eighth bit of the data byte has been latched in, otherwise the write to lock register (WRLR) instruction is not executed.

Lock register bits are volatile, and therefore do not require time to be written. When the write to lock register (WRLR) instruction has been successfully executed, the write enable latch (WEL) bit is reset after a delay time less than t_{SHSL} minimum value.

Any write to lock register (WRLR) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 23. Write to lock register (WRLR) instruction sequence

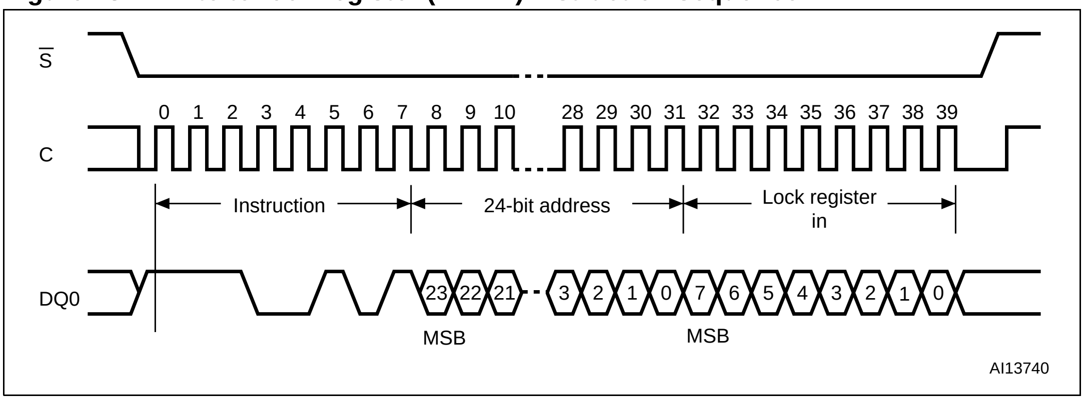


Table 10. Lock register in(1)

Sector	Bit	Value
All sectors	b7-b2	'0'
	b1	Sector lock down bit value (refer to *Table 9*)
	b0	Sector write lock bit value (refer to *Table 9*)

1. Values of (b1, b0) after power-up are defined in *Section 7: Power-up and power-down*.

6.15 Subsector erase (SSE)

The subsector erase (SSE) instruction sets to '1' (FFh) all bits inside the chosen subsector. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

The subsector erase (SSE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on serial data input (DQ0). Any address inside the subsector (see *Table 4*) is a valid address for the subsector erase (SSE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

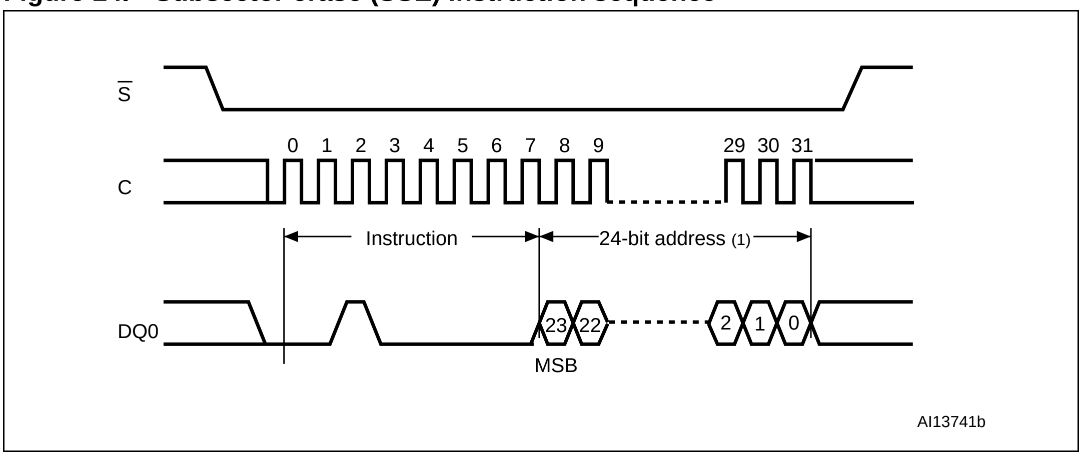
The instruction sequence is shown in *Figure 24*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the subsector erase (SSE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed subsector erase cycle (whose duration is t_{SSE}) is initiated. While the subsector erase cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed subsector erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the write enable latch (WEL) bit is reset.

A subsector erase (SSE) instruction issued to a sector that is hardware or software protected, is not executed.

Any subsector erase (SSE) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 24. Subsector erase (SSE) instruction sequence



1. Address bit A23 is don't care.

6.16 Sector erase (SE)

The sector erase (SE) instruction sets to '1' (FFh) all bits inside the chosen sector. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

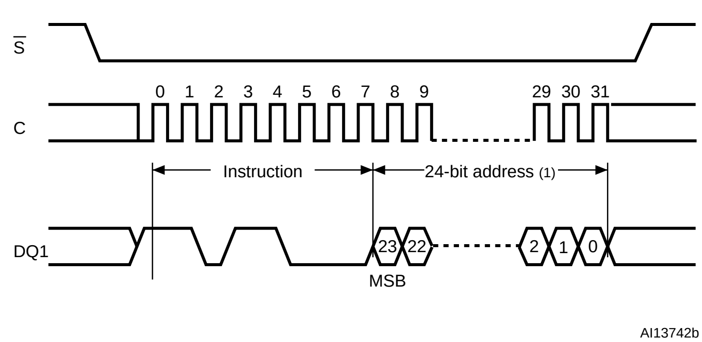
The sector erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on serial data input (DQ0). Any address inside the sector (see *Table 4*) is a valid address for the sector erase (SE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 25*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the sector erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed sector erase cycle (whose duration is t_{SE}) is initiated. While the sector erase cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed sector erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset.

A sector erase (SE) instruction applied to a page which is protected by the block protect (BP2, BP1, BP0) bits (see *Table 3* and *Table 4*) is not executed.

Figure 25. Sector erase (SE) instruction sequence



1. Address bit A23 is don't care.

6.17 Bulk erase (BE)

The bulk erase (BE) instruction sets all bits to ‘1’ (FFh). Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

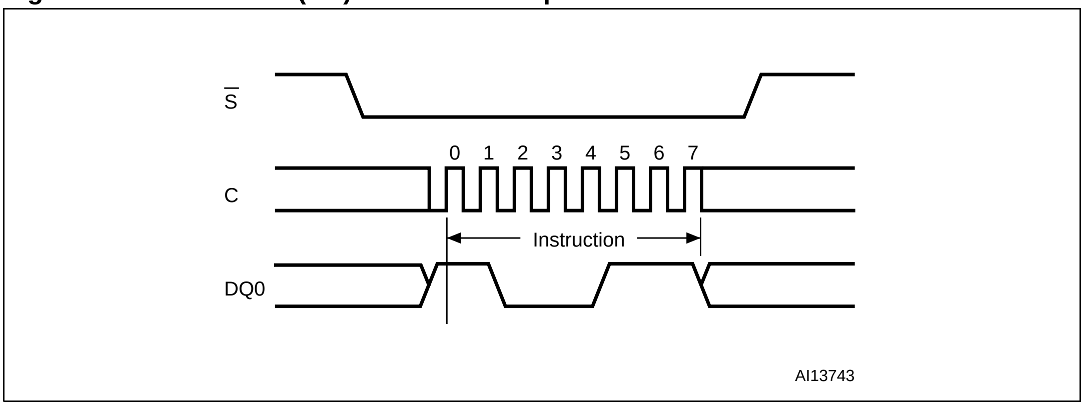
The bulk erase (BE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on serial data input (DQ0). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 26*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the bulk erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed bulk erase cycle (whose duration is t_{BE}) is initiated. While the bulk erase cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed bulk erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset.

The bulk erase (BE) instruction is executed only if all block protect (BP2, BP1, BP0) bits are 0. The bulk erase (BE) instruction is ignored if one, or more, sectors are protected.

Figure 26. Bulk erase (BE) instruction sequence



6.18 Deep power-down (DP)

Executing the deep power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the deep power-down mode). It can also be used as a software protection mechanism, while the device is not in active use, as in this mode, the device ignores all write, program and erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in the standby power mode (if there is no internal cycle currently in progress). But this mode is not the deep power-down mode. The deep power-down mode can only be entered by executing the deep power-down (DP) instruction, subsequently reducing the standby current (from I_{CC1} to I_{CC2}, as specified in *Table 17*).

To take the device out of deep power-down mode, the release from deep power-down (RDP) instruction must be issued. No other instruction must be issued while the device is in deep power-down mode.

The deep power-down mode automatically stops at power-down, and the device always powers up in the standby power mode.

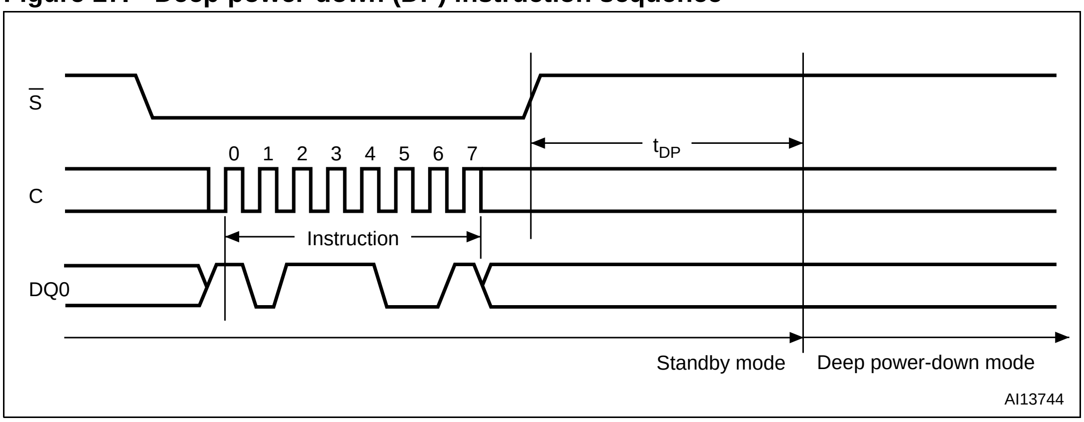
The deep power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on serial data input (DQ0). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 27*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the deep power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the deep power-down mode is entered.

Any deep power-down (DP) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 27. Deep power-down (DP) instruction sequence



6.19 Release from deep power-down (RDP)

Once the device has entered the deep power-down mode, all instructions are ignored except the release from deep power-down (RDP) instruction. Executing this instruction takes the device out of the deep power-down mode.

The release from deep power-down (RDP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on serial data input (DQ0). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

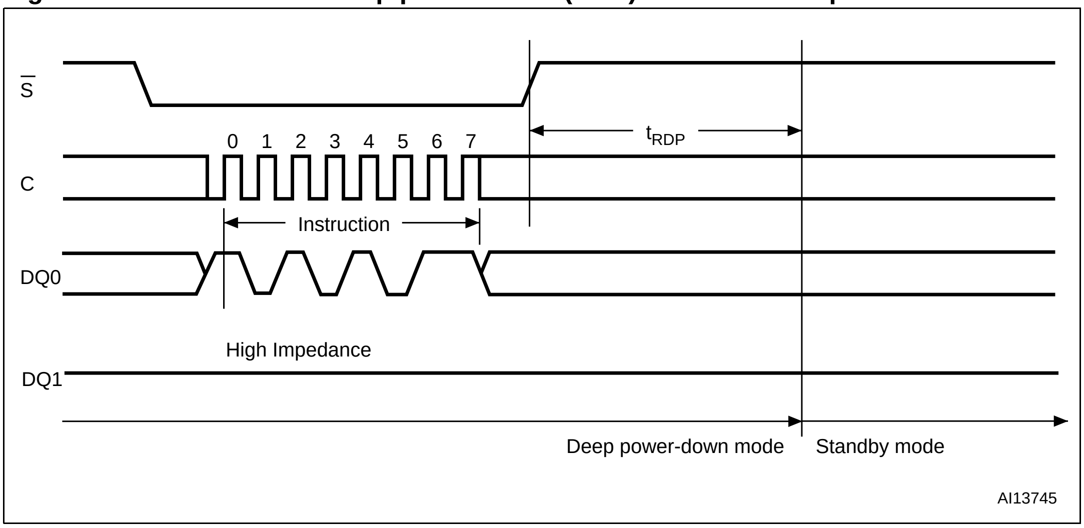
The instruction sequence is shown in *Figure 28*.

The release from deep power-down (RDP) instruction is terminated by driving Chip Select ($\overline{S}$) High. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the instruction to be rejected, and not executed.

After Chip Select ($\overline{S}$) has been driven High, followed by a delay, t_{RDP}, the device is put in the standby mode. Chip Select ($\overline{S}$) must remain High at least until this period is over. The device waits to be selected, so that it can receive, decode and execute instructions.

Any release from deep power-down (RDP) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 28. Release from deep power-down (RDP) instruction sequence



7 Power-up and power-down

At power-up and power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC}(min) at power-up, and then for a further delay of t_{VSL}
- V_{SS} at power-down.

A safe configuration is provided in *Section 3: SPI modes*.

To avoid data corruption and inadvertent write operations during power-up, a power on reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the power on reset (POR) threshold voltage, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all write enable (WREN), page program (PP), dual input fast program (DIFP), program OTP (POTP), subsector erase (SSE), sector erase (SE), bulk erase (BE), write status register (WRSR) and write to lock register (WRLR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No write status register, program or erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} has passed the V_{WI} threshold
- t_{VSL} after V_{CC} has passed the V_{CC}(min) level.

These values are specified in *Table 11*.

If the time, t_{VSL}, has elapsed, after V_{CC} rises above V_{CC}(min), the device can be selected for read instructions even if the t_{PUW} delay has not yet fully elapsed.

After power-up, the device is in the following state:

- The device is in the standby power mode (not the deep power-down mode)
- The write enable latch (WEL) bit is reset
- The write in progress (WIP) bit is reset
- The lock registers are configured as: (write lock bit, lock down bit) = (0,0).

Normal precautions must be taken for supply line decoupling, to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitable capacitor close to the package pins (generally, this capacitor is of the order of 100 nF).

At power-down, when V_{CC} drops from the operating voltage, to below the power on reset (POR) threshold voltage, V_{WI}, all operations are disabled and the device does not respond to any instruction (the designer needs to be aware that if power-down occurs while a write, program or erase cycle is in progress, some data corruption may result).

- V_{PPH} must be applied only when V_{CC} is stable and in the V_{CC}(min) to V_{CC}(max) voltage range.

Figure 29. Power-up timing

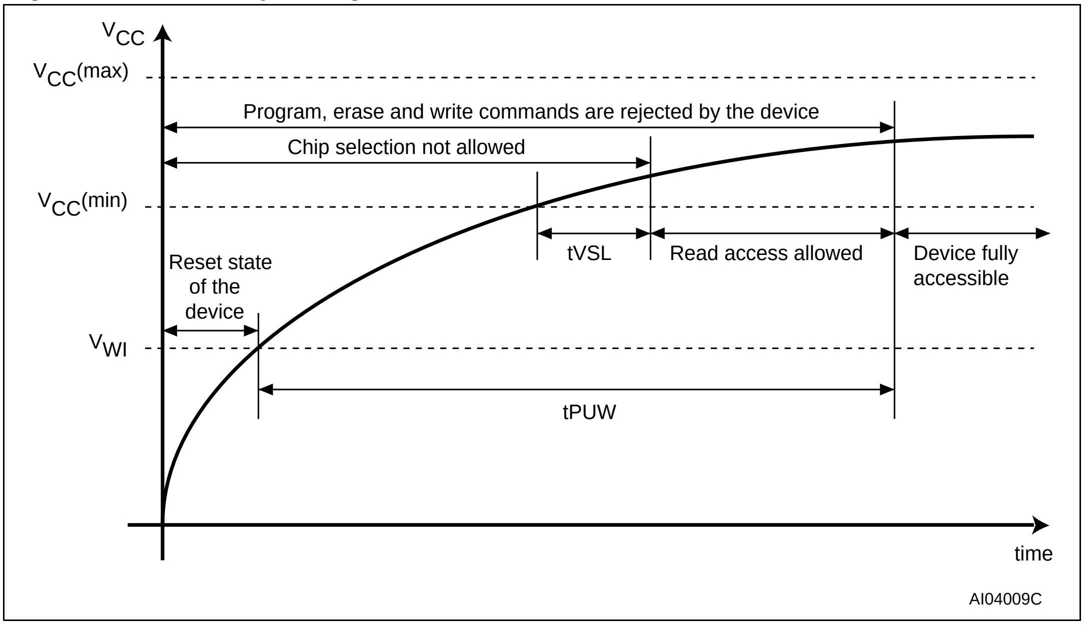


Table 11. Power-up timing and V_{WI} threshold

Symbol	Parameter	Min	Max	Unit
t_{VSL}(1)	V_{CC}(min) to $\overline{S}$ Low	30		µs
t_{PUW}(1)	Time delay to write instruction	1	10	ms
V_{WI}(1)	Write inhibit voltage	1.5	2.5	V

1. These parameters are characterized only.

8 Initial delivery state

The device is delivered with the memory array erased: all bits are set to ‘1’ (each byte contains FFh). The status register contains 00h (all status register bits are 0).

9 Maximum ratings

Stressing the device outside the ratings listed in *Table 12: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE program and other relevant quality documents.

Table 12. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering		see[1]	°C
V_{IO}	Input and output voltage (with respect to ground)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	4.0	V
V_{PP}	Fast program/erase voltage[2]	–0.2	10.0	V
V_{ESD}	Electrostatic discharge voltage (human body model)[3]	–2000	2000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. Avoid applying V_{PPH} to the $\overline{W}$/VPP pin during Bulk Erase.
3. JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 13. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
Vcc	Supply Voltage	2.7		3.6	V
Vphh	Supply Voltage on Vpp	8.5		9.5	V
tA	Ambient operating temperature (device grade 6)	-40		85	C
	Ambient operating temperature (device grade 3)	-40		125	

Table 14. Data Retention and Endurance

Parameter	Condition	Min.	Max.	Unit
Program/Erase Cycles	Grade 3, Autograde 6, Grade 6	100000		Cycles per Sector
Data Retention	at 55°C	20		years

Table 15. AC measurement conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		5	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output timing reference voltages	V_{CC} / 2		V

Figure 30. AC measurement I/O waveform

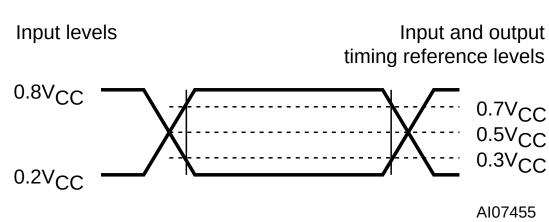


Table 16. Capacitance(1)

Symbol	Parameter	Test condition	Min	Max	Unit
$C_{IN/OUT}$	Input/output capacitance (DQ0/DQ1)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A=25 °C and a frequency of 33 MHz.

Table 17. DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table 13*)	Min	Max	Unit
I_{LI}	Input leakage current			± 2	µA
I_{LO}	Output leakage current			± 2	µA
I_{CC1}	Standby current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		50	µA
I_{CC2}	Deep Power-down current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		10	µA
I_{CC3}	Operating current (READ)	C = 0.1V_{CC} / 0.9V_{CC} at 75 MHz, DQ1 = open		12	mA
		C = 0.1V_{CC} / 0.9V_{CC} at 33 MHz, DQ1 = open		4	mA
	Operating current (DOFR)	C = 0.1V_{CC} / 0.9V_{CC} at 75 MHz, DQ1 = open		15	mA
I_{CC4}	Operating current (PP)	$\overline{S} = V_{CC}$		15	mA
	Operating current (DIFP)	$\overline{S} = V_{CC}$		15	mA
I_{CC5}	Operating current (WRSR)	$\overline{S} = V_{CC}$		15	mA
I_{CC6}	Operating current (SE)	$\overline{S} = V_{CC}$		15	mA
I_{PP}	V_{PP} operating current in fast bulk erase mode	$\overline{S} = V_{CC}$, $V_{PP} = V_{PPH}$		20	mA
V_{IL}	Input low voltage		– 0.5	0.3V_{CC}	V
V_{IH}	Input high voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –100 µA	V_{CC}–0.2		V

Table 18. AC characteristics

Test conditions specified in *Table 13* and *Table 15*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ[(1)]**	**Max**	**Unit**
f_C	f_C	Clock frequency for the following instructions: DOFR, DIFP, FAST_READ, SSE, SE, BE, DP, WREN, WRDI, RDID, RDSR, WRSR, ROTP, PP, POTP, WRLR, RDLR, RDP	D.C.		75	MHz
f_R		Clock frequency for read instructions	D.C.		33	MHz
t_{CH}[(2)]	t_{CLH}	Clock High time	6			ns
t_{CL}[(2)]	t_{CLL}	Clock Low time	6			ns
t_{CLCH}[(3)]		Clock rise time[(4)] (peak to peak)	0.1			V/ns
t_{CHCL}[(3)]		Clock fall time[(4)] (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ active setup time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ not active hold time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data in setup time	2			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{S}$ active hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ not active setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ deselect time	80			ns
t_{SHQZ}[(3)]	t_{DIS}	Output disable time			8	ns
t_{CLQV}	t_V	Clock Low to Output valid under 30 pF			8	ns
		Clock Low to Output valid under 10 pF			6	ns
t_{CLQX}	t_{HO}	Output hold time	0			ns
t_{HLCH}		$\overline{HOLD}$ setup time (relative to C)	5			ns
t_{CHHH}		$\overline{HOLD}$ hold time (relative to C)	5			ns
t_{HHCH}		$\overline{HOLD}$ setup time (relative to C)	5			ns
t_{CHHL}		$\overline{HOLD}$ hold time (relative to C)	5			ns
t_{HHQX}[(3)]	t_{LZ}	$\overline{HOLD}$ to Output Low-Z			8	ns
t_{HLQZ}[(3)]	t_{HZ}	$\overline{HOLD}$ to Output High-Z			8	ns
t_{WHSL}[(5)]		Write protect setup time	20			ns
t_{SHWL}[(5)]		Write protect hold time	100			ns
t_{VPPHSL}[(6)]		Enhanced program supply voltage High (V_{PPH}) to Chip Select Low	200			ns
t_{DP}[(3)]		$\overline{S}$ High to deep power-down mode			3	µs
t_{RDP}[(3)]		$\overline{S}$ High to standby mode			30	µs

Table 18. AC characteristics (continued)

Test conditions specified in *Table 13* and *Table 15*						
Symbol	Alt.	Parameter	Min	Typ(1)	Max	Unit
t_W		Write status register cycle time		1.3	15	ms
t_{PP}(7)		Page program cycle time (256 bytes)		0.8	5	ms
		Page program cycle time (n bytes)		int(n/8) × 0.025(8)		
		Program OTP cycle time (64 bytes)		0.2		ms
t_{SSE}		Subsector erase cycle time		70	150	ms
t_{SE}		Sector erase cycle time		0.7	3	s
t_{BE}		Bulk erase cycle time		68	160	s

1. Typical values given for T_A = 25° C.
2. t_{CH} + t_{CL} must be greater than or equal to 1/ f_C.
3. Value guaranteed by characterization, not 100% tested in production.
4. Expressed as a slew-rate.
5. Only applicable as a constraint for a WRSR instruction when SRWD is set to ‘1’.
6. V_{PPH} should be kept at a valid level until the program or erase operation has completed and its result (success or failure) is known. Avoid applying V_{PPH} to the W/VPP pin during Bulk Erase.
7. When using the page program (PP) instruction to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes (1 ≤ n ≤ 256).
8. int(A) corresponds to the upper integer part of A. For example int(12/8) = 2, int(32/8) = 4 int(15.3) =16.

Figure 31. Serial input timing

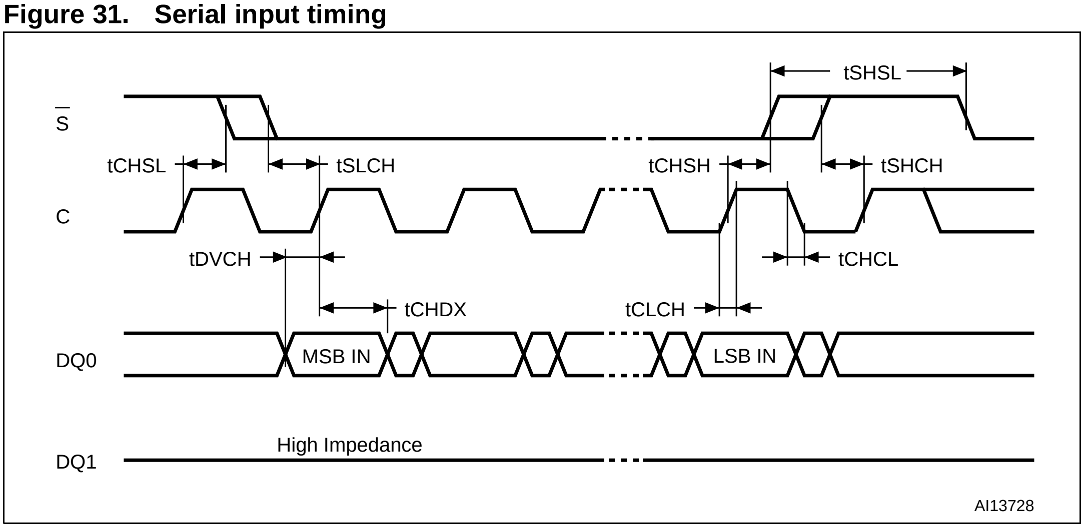


Figure 32. Write protect setup and hold timing during WRSR when SRWD=1

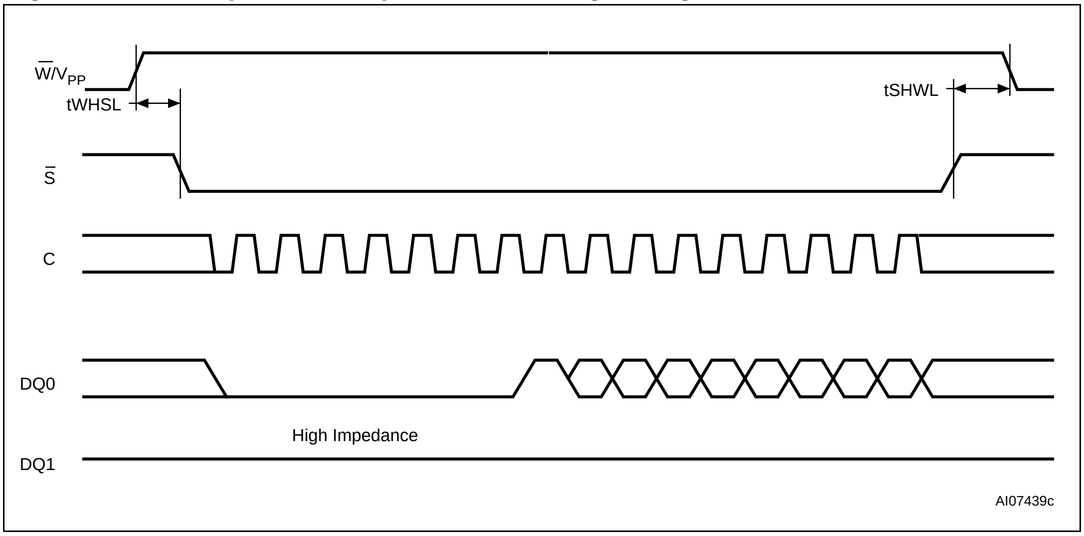


Figure 33. Hold timing

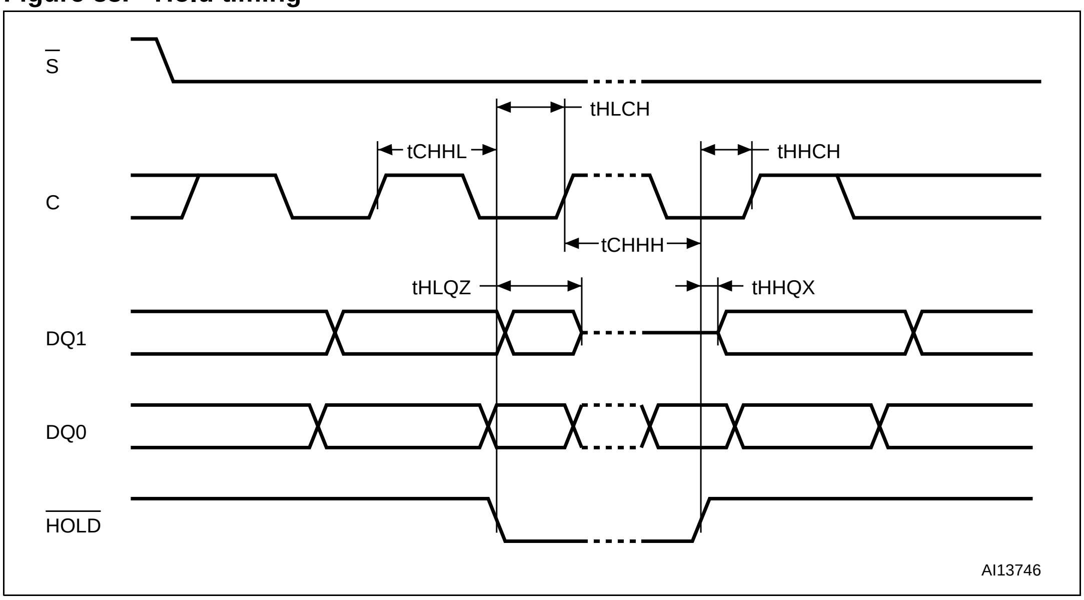


Figure 34. Output timing

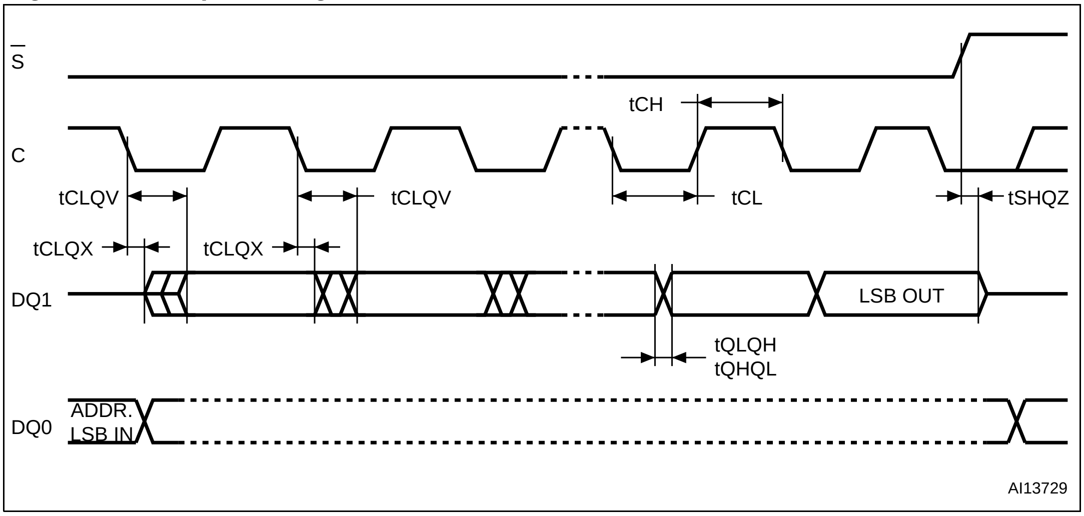
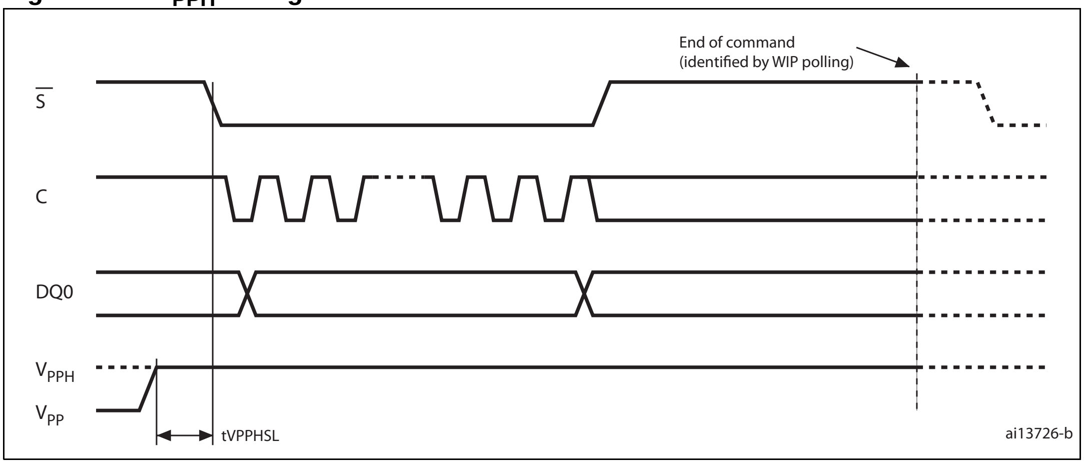


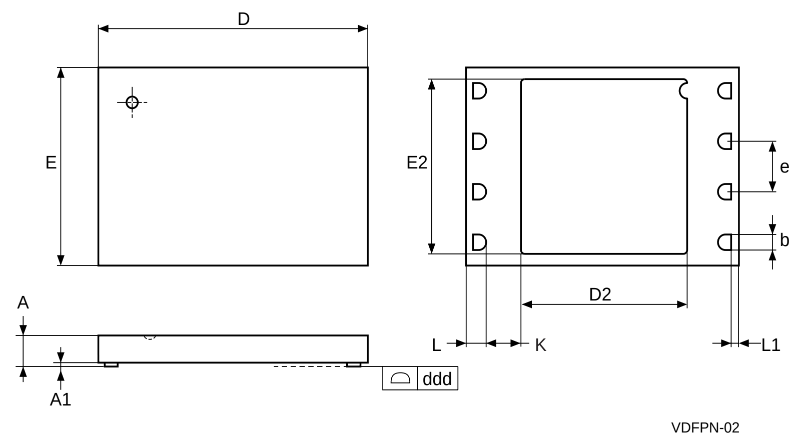
Figure 35. V_{PPH} timing



11 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in RoHS packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 36. VDFPN8 (MLP8) 8-lead very thin dual flat package no lead, 8 × 6 mm, package outline



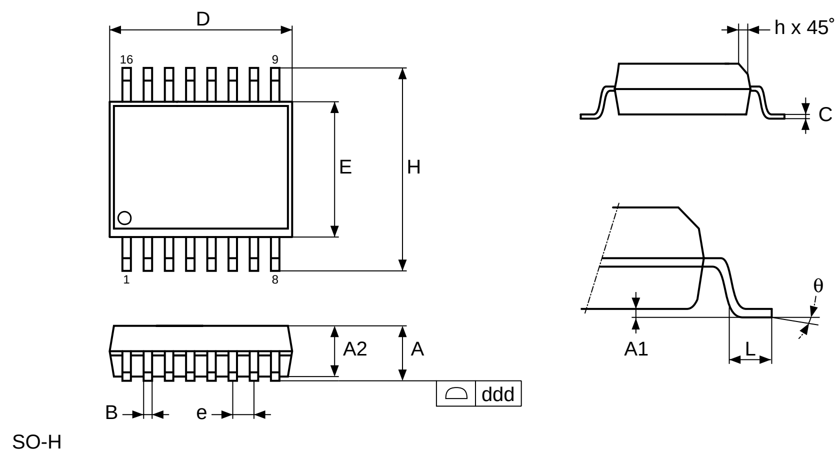
1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

Table 19. VDFPN8 (MLP8) 8-lead very thin dual flat package no lead, 8 × 6 mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	0.85		1.00	0.033		0.039
A1		0.00	0.05		0.000	0.002
b	0.40	0.35	0.48	0.016	0.014	0.019
D	8.00			0.315		
D2	5.16		(1)	0.203		
ddd			0.05			0.002
E	6.00			0.236		
E2	4.80			0.189		
e	1.27	–	–	0.050	–	–
K		0.82			0.032	
L	0.50	0.45	0.60	0.020	0.018	0.024
L1			0.15			0.006
N	8			8		

1. D2 Max must not exceed (D – K – 2 × L).

Figure 37. SO16 wide - 16-lead plastic small outline, 300 mils body width, package outline



1. Drawing is not to scale.

Table 20. SO16 wide - 16-lead plastic small outline, 300 mils body width, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A		2.35	2.65		0.093	0.104
A1		0.10	0.30		0.004	0.012
B		0.33	0.51		0.013	0.020
C		0.23	0.32		0.009	0.013
D		10.10	10.50		0.398	0.413
E		7.40	7.60		0.291	0.299
e	1.27	–	–	0.050	–	–
H		10.00	10.65		0.394	0.419
h		0.25	0.75		0.010	0.030
L		0.40	1.27		0.016	0.050
θ		0°	8°		0°	8°
ddd			0.10			0.004

Figure 38. TBGA, 6x8 mm, 24 ball package outline

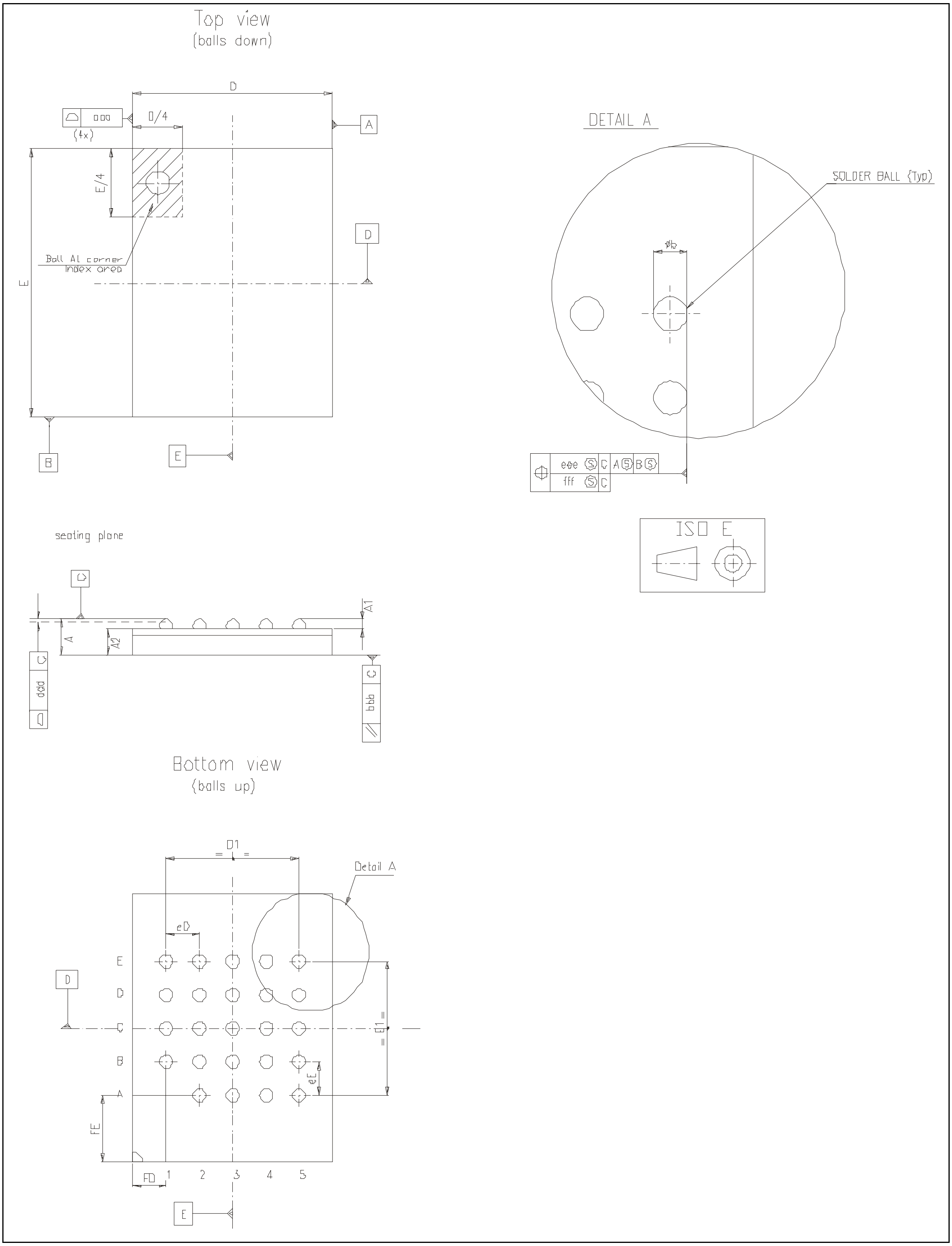


Table 21. TBGA 6x8 mm 24-ball package dimensions

	MIN	NOM	MAX
A			1.20
A1	0.20		
A2		0.79	
Øb	0.35	0.40	0.45
D	5.90	6.00	6.10
D1		4.00	
E	7.90	8.00	8.10
E1		4.00	
eD		1.00	
eE		1.00	
FD		1.00	
FE		2.00	
MD	5		
ME	5		
n	24 balls		
aaa			0.15
bbb			0.10
ddd			0.10
eee			0.15
fff			0.08
Control unit: mm			

12 Ordering information

Table 22. Ordering information scheme

Example:	M25PX64	–	V	ME	3	T	P	B	A

Device type

M25PX = serial Flash memory, 4-Kbyte and 64-Kbyte erasable sectors, dual input/output

Device function

64 = 64 Mbit (8 Mb × 8)

Security features(1)

– = no extra security

SO = OTP configurable

ST = OTP configurable + protection at power_up

S = CFD programmed with UID

Operating voltage

V = V_{CC} = 2.7 V to 3.6 V

Package

ME = VDFPN8 8 × 6 mm (MLP8)

MF = SO16 (300 mils width)

ZM = TBGA24 6 x 8 mm

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

3(2) = Automotive temperature range, –40 to 125 °C.

Device tested with high reliability certified flow(3).

Option

blank = Standard packing

T = Tape and reel packing

Plating Technology

P or G = RoHS compliant

Lithography

B = 110nm, Fab.2 Diffusion Plant
blank = 110 nm

Automotive Grade

A(2) = Automotive –40 to 125 °C Part.

Device tested with high reliability certified flow.(3)

blank = standard –40 to 85 °C device

1. Secure options are available upon customer request.
2. Numonyx strongly recommends the use of the Automotive Grade devices(AutoGrade 6 and Grade 3) for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801.
3. Device grade 3 available in an SO8 RoHS compliant package.

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest Numonyx sales office.

13 Revision history

Table 23. Document revision history

Date	Revision	Changes
05-Nov-2007	1	Initial release.
25-Mar-2008	2	Updated the minimum value for t_{SHSL} in *Table 18: AC characteristics*. Applied Numonyx branding.
24-Sept-2008	3	Corrected bulk erase specifications on the cover page. Added the following information regarding Bulk Erase: Avoid applying V_{PPH} to the $\overline{W}$/VPP pin during Bulk Erase.
04-February-2009	4	Added the TBGA package and accompanying informaiton.
16-February-2009	5	Added Notes to the TBGA package and deleted a blank page.
6-March-2009	6	Added “Automotive Certified Parts” information.

Please Read Carefully: