LPC32x0

16/32-bit ARM microcontroller; hardware floating-point coprocessor, USB On-The-Go, and EMC memory interface

Rev. 00.01 — 25 March 2008 **Preliminary data sheet**

1. General description

N01XP Semiconductor designed the LPC32x0 family for embedded applications requiring high performance combined with low power consumption.

NXP achieved their performance goals using 90 nanometer process technology to implement an ARM926EJ-S CPU core with a Vector Floating Point co-processor and a large set of standard peripherals including USB On-The-Go. Figure 1 shows a block diagram of the LPC32x0 family. The LPC32x0 family operates at CPU frequencies exceeding 200 MHz. The basic ARM926EJ-S CPU Core implementation uses a Harvard architecture with a 5-stage pipeline. The ARM926EJ-S core also has an integral Memory Management Unit (MMU) to provide the virtual memory capabilities needed to support the multi-programming demands of modern operating systems. The basic ARM926EJ-S core also includes a set of DSP instruction extensions including single cycle MAC operations and native Jazelle Java Byte-code execution in hardware. The NXP implementation has a 32 KB Instruction Cache and a 32 KB Data Cache.

For low power consumption, the LPC32x0 family takes advantage of NXP Semiconductor's advanced technology development to optimize Intrinsic Power, and uses software controlled architectural enhancements to optimize application based Power Management.

The LPC32x0 family also includes 256 KB of on-chip static RAM, a NAND Flash interface, an Ethernet MAC, an LCD controller that supports STN and TFT panels, and an external bus interface that supports SDR and DDR SDRAM as well as static devices. In addition, the LPC32x0 family includes a USB 2.0 Full Speed interface, seven UARTs, two I2C interfaces, two SPI/SSP ports, two I2S interfaces, two multi-channel PWMs, four general purpose timers with capture inputs and compare outputs, a Secure Digital (SD) interface, and a 10-bit A/D converter with a touch screen sense option.

2. Features

- ARM926EJS processor, running at CPU clock speeds up to 208 MHz
- A Vector Floating Point coprocessor.
- A 32 KB instruction cache and a 32 KB data cache.
- Up to 256 KB of internal SRAM (IRAM).
- Selectable boot-up from various external devices: NAND Flash, SPI memory, USB, UART, or static memory.

- A Multi-layer AHB system that provides a separate bus for each AHB master, including both an instruction and data bus for the CPU, two data busses for the DMA controller, and another bus for the USB controller, one for the LCD and a final one for the Ethernet MAC. There are no arbitration delays in the system unless two masters attempt to access the same slave at the same time.
- An External memory controller for DDR and SDR SDRAM, as well as static devices.
- Two NAND Flash controllers. One for single level NAND Flash devices and the other for multi-level NAND Flash devices.
- A Master Interrupt Controller (MIC) and two Slave Interrupt Controllers (SIC), supporting 74 interrupt sources.
- An eight channel General Purpose AHB DMA controller (GPDMA) that can be used with the SD card port, the high-speed UARTs, I2S ports, and SPI interfaces, as well as memory-to-memory transfers.
- Serial Interfaces:
  - A 10/100 Ethernet MAC with dedicated DMA Controller.
  - A USB interface supporting either Device, Host (OHCI compliant), or On-The-Go (OTG) with an integral DMA controller and dedicated PLL to generate the required 48 MHz USB clock.
  - Four standard UARTs with fractional baud rate generation and 64 byte FIFOs. One of the standard UART's supports irDA.
  - Three additional high-speed UARTs intended for on-board communications that support baud rates up to 921,600 bps when using a 13 MHz main oscillator. All high-speed UARTs provide 64-byte FIFOs.
  - Two SPI controllers.
  - Two SSP controllers.
  - Two I2C-bus Interfaces with standard open drain pins. The I2C-bus Interfaces support single master, slave and multi-master I2C configurations.
  - Two I2S interfaces, each with separate input (RX) and output (TX) channels. Each channel can be operated independently on 3 pins, or both input and output channels can be used with only 4 pins and a shared clock.
- Additional Peripherals:
  - LCD controller supporting both STN and TFT panels, with dedicated DMA controller. Programmable display resolution up to 1024x768.
  - Secure Digital (SD) memory card interface, which conforms to the SD Memory Card Specification Version 1.01.
  - General purpose input, output, and I/O pins. Includes 12 GP input pins, 24 GP output pins, and 51 GP I/O pins.
  - 10 bit, 400kHz A/D Converter with input multiplexing from 3 pins. Optionally, the A/D Converter can operate as a touch screen controller.
  - Real Time Clock (RTC) with separate power pin. This RTC has a dedicated 32 kHz oscillator. NXP implemented the RTC in an independent on-chip power domain so it can remain active while the rest of the chip is not powered. The RTC also Includes a 32 byte scratch pad memory.
  - A 32-bit general purpose high speed timer with a 16-bit pre-scaler. This timer includes one external capture input pin and a capture connection to the RTC clock. Interrupts may be generated using 3 match registers.

  - Four enhanced Timer/Counters which are identical except for the peripheral base address. A minimum of two Capture inputs and two Match outputs are pinned out for all four timers, with a choice of several pins for each. Timer 1 brings out a third Match output, while Timers 2 and 3 bring out all four Match outputs.
  - A 32-bit Millisecond timer driven from the RTC clock. This timer can generate Interrupts using 2 match registers.
  - A Watchdog Timer. The watchdog timer is clocked by PERIPH_CLK.
  - Two versatile PWM blocks with 6 and 4 outputs respectively, programmable resolution, and an external clock capability.
  - Two additional single output PWM blocks.
  - Keyboard scanner function allows automatic scanning of up to an 8x8 key matrix.
  - Up to 18 external interrupts.
- Standard ARM Test/Debug interface for compatibility with existing tools.
- Emulation Trace Buffer with 2K x 24 bit RAM allows trace via JTAG.
- Stop mode saves power, while allowing many peripheral functions to restart CPU activity.
- On-chip crystal oscillator.
- An on-chip PLL allows CPU operation up to the maximum CPU rate without the requirement for a high frequency crystal. Another PLL allows operation from the 32 kHz RTC clock rather than the external crystal.
- Boundary Scan for simplified board testing.
- 296 pin TFBGA package.

3. Applications

3.1 Application Type

- Consumer
- Medical
- Industrial
- Automotive
- Network Control

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC3220FET296[1]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls; body 15 x 15 x 0.7 mm	SOT1048-1
LPC3230FET296[1]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls; body 15 x 15 x 0.7 mm	SOT1048-1
LPC3240FET296[1]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls; body 15 x 15 x 0.7 mm	SOT1048-1
LPC3250FET296[1]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls; body 15 x 15 x 0.7 mm	SOT1048-1

[1] F = -40 °C to +85 °C temperature range.

4.1 Ordering options

Table 2. Part options

Type number	SRAM(KB)	10/100 Ethernet	LCD Controller	Temperature range (°C)	Package
LPC3220FET296	128	0	0	-40 to +85	TFBGA296
LPC3230FET296	256	0	1	-40 to +85	TFBGA296
LPC3240FET296	256	1	0	-40 to +85	TFBGA296
LPC3250FET296	256	1	1	-40 to +85	TFBGA296

5. Block diagram

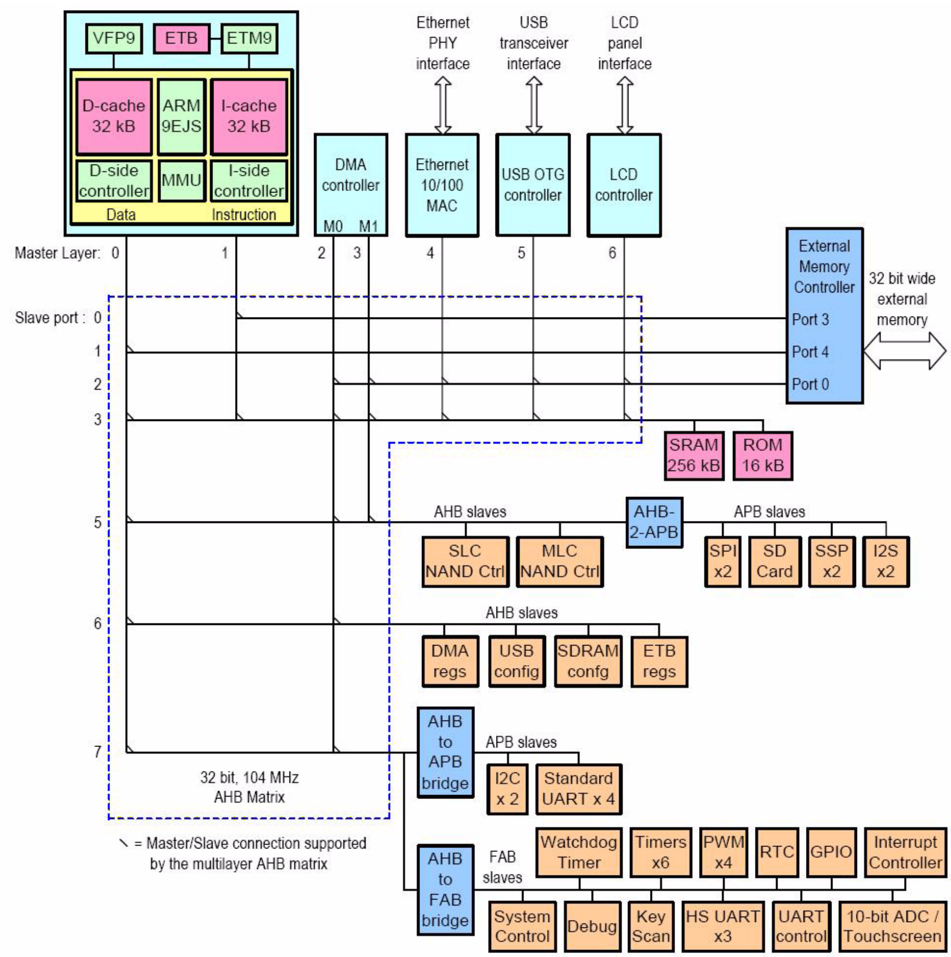
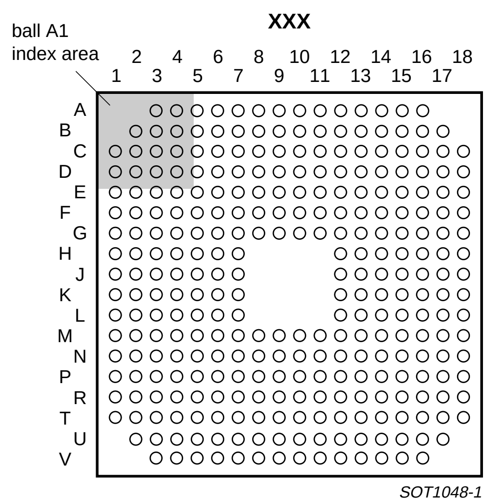


Fig 1. Block diagram of LPC32x0 family

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration for SOT1048-1 (TFBGA296)

Table 3. Pin Allocation Table SOT1048-1 (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A					
				A3	I2C2_SCL
A4	I2S1TX_CLK / MAT3.0	A5	I2C1_SCL	A6	MS_BS / MAT2.1 / PWM3.6
A7	MS_DIO1 / MAT0.1 / PWM3.2	A8	MS_DIO0 / MAT0.0 / PWM3.1	A9	SPI2_DATIO / MOSI1 /LCDVD[20]
A10	SPI2_DATIN / MISO1 / LCDVD[21] / GPI27	A11	GPIO_01	A12	GPIO_00
A13	GPO_21 / U4_TX / LCDVD[3]	A14	GPO_15 / PWM3.3 / LCDFP	A15	GPO_07 / LCDVD[2]
A16	GPO_06 / PWM4.3 / LCDVD[18]				
Row B					
		B2	GPO_20	B3	GPO_05
B4	I2S1TX_WS / CAP3.0	B5	P0.0 / I2S1RX_CLK	B6	I2C1_SDA
B7	MS_SCLK / MAT2.0 / PWM3.5	B8	MS_DIO2 / MAT0.2 / PWM3.3	B9	SPI1_DATIO / MOSI0
B10	SPI2_CLK / SCK1 / LCDVD[23]	B11	GPIO_04 / SSEL1 / LCDVD[22]	B12	GPO_12 / PWM3.5 / LCDLE
B13	GPO_13 / PWM3.4 / LCDDCLK	B14	GPO_02 / MAT1.0 / LCDVD[0]	B15	GPI_19 / U4_RX
B16	GPI_08 / KEY_COL6 /SPI2_BUSY / ENET_RX_DV	B17	N.C.		
Row C					
C1	FLASH_RD_N	C2	GPO_19	C3	GPO_00 / TST_CLK1
C4	USB_ATX_INT_N	C5	USB_SE0_ VM / U5_TX	C6	TST_CLK2

Table 3. Pin Allocation Table SOT1048-1 (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
C7	GPI_06 / HSTIM_CAP / I2S1RX_SDA	C8	MS_DIO3 / MAT0.3 / PWM3.4	C9	SPI1_CLK / SCK0
C10	SPI1_DATIN / MISO0 / GPI_25	C11	GPIO_03 / KEY_ROW7 / ENET_MDIO	C12	GPO_09 / PWM4.1 / LCDVD[9]
C13	GPO_08 / PWM4.2 / LCDVD[8]	C14	GPI_02 / CAP2.0 / ENET_RXD3	C15	GPI_01 / SERVICE_N
C16	GPI_00 / ENET_RXD2	C17	KEY_ROW4 / ENET_TXD0	C18	KEY_ROW5 / ENET_TXD1
Row D					
D1	FLASH_RDY	D2	FLASH_ALE	D3	GPO_14
D4	GPO_01	D5	USB_DAT_VP / U5_RX / GPI_20	D6	USB_OE_TP_N
D7	P0.1 / I2S1RX_WS	D8	GPO_04	D9	GPIO_02 / KEY_ROW6 / ENET_MDC
D10	GPO_16 / PWM3.2 /LCDENAB / LCDM	D11	GPO_18 / PWM3.1 / LCDLP	D12	GPO_03 / LCDVD[1]
D13	GPI_07 / PCAP3.0	D14	PWM_OUT1 / LCDVD[16]	D15	PWM_OUT2 / LCDVD[19]
D16	KEY_ROW3 / ENET_TX_EN	D17	KEY_COL2 / ENET_RX_ER	D18	KEY_COL3 / ENET_CRS
Row E					
E1	FLASH_IO[03]	E2	FLASH_IO[07]	E3	FLASH_CE_N
E4	I2C2_SDA	E5	USB_I2C_SCL	E6	USB_I2C_SDA
E7	I2S1TX_SDA / MAT3.1	E8	GPO_11	E9	GPIO_05 / SSEL0
E10	GPO_22 / U7_HRTS / LCDVD[14]]	E11	GPO_10 / PWM3.6 / LCDPWR	E12	GPI_09 / KEY_COL7 / ENET_COL
E13	GPI_04 / SPI1_BUSY	E14	KEY_ROW1 / ENET_TXD2	E15	KEY_ROW0 / ENET_TX_ER
E16	KEY_COL1 /ENET_RX_CLK /ENET_REF_CLK	E17	U7_RX / CAP0.0 / LCDVD[10] /GPI_23	E18	U7_TX / MAT1.1 / LCDVD[11]
Row F					
F1	FLASH_IO[02]	F2	FLASH_WR_N	F3	FLASH_CLE
F4	GPI_03	F5	VSS_IOC	F6	VSS_IOB
F7	VDD_IOC	F8	VDD_IOB	F9	VDD_IOD
F10	VSS_IOD	F11	VSS_IOD	F12	VSS_IOD
F13	VDD_IOD	F14	KEY_ROW2 / ENET_RXD3	F15	KEY_COL0 / ENET_TX_CLK
F16	KEY_COL5 / ENET_RXD1	F17	U6_IRRX / GPI_21	F18	U5_RX
Row G					
G1	EMC_DYCS1_N	G2	FLASH_IO[05]	G3	FLASH_IO[06]
G4	RESOUT_N	G5	VSS_IOC	G6	VDD_IOC
G7	VDD_CORE12	G8	VSS_CORE	G9	VDD_CORE12
G10	VSS_CORE	G11	VDD_CORE12	G12	VSS_CORE
G13	U7_HCTS / CAP0.1 /LCDCLKIN / GPI_22	G14	DBGEN	G15	KEY_COL4 / ENET_RXD0
G16	U6_IRTX	G17	SYSCLKEN / LCDVD[15]	G18	JTAG_TMS
Row H					
H1	EMC_OE_N	H2	FLASH_IO[00]	H3	FLASH_IO[01]
H4	FLASH_IO[04]	H5	VSS_IOC	H6	VDD_IOC

Table 3. Pin Allocation Table SOT1048-1 (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
H7	VSS_CORE				
				H12	VSS_IOD
H13	VDD_IOA	H14	JTAG_TCK	H15	U5_TX
H16	HIGHCORE / LCDVD[17]	H17	JTAG_NTRST	H18	JTAG_RTCK
Row J					
J1	EMC_A[20] / P1.20	J2	EMC_A[21] / P1.21	J3	EMC_A[22] / P1.22
J4	EMC_A[23] / P1.23	J5	VDD_IOC	J6	VDD_EMC
J7	VDD_CORE12				
				J12	VDD_CORE12
J13	VDD_IOA	J14	U3_RX / GPI_18	J15	JTAG_TDO
J16	JTAG_TDI	J17	U3_TX	J18	U2_HCTS / U3_CTS / GPI_16
Row K					
K1	EMC_A[19] / P1.19	K2	EMC_A[18] / P1.18	K3	EMC_A[16] / P1.16
K4	EMC_A[17] / P1.17	K5	VSS_EMC	K6	VDD_EMC
K7	VDD_EMC				
				K12	VSS_CORE
K13	VSS_IOA	K14	VDD_RTC	K15	U1_RX / CAP1.0 / GPI_15
K16	U1_TX	K17	U2_TX / U3_DTR	K18	U2_RX / U3_DSR / GPI_17
Row L					
L1	EMC_A[15] / P1.15	L2	EMC_CKE1	L3	EMC_A[00] / P1.0
L4	EMC_A[01] / P1.1	L5	VSS_EMC	L6	VDD_EMC
L7	VSS_CORE				
				L12	VDD_COREFXD
L13	VDD_RTCCORE	L14	VSS_RTCCORE	L15	P0.4 / I2S0RX_WS / LCDVD[6]
L16	P0.5 / I2S0TX_SDA / LCDVD[7]	L17	P0.6 / I2S0TX_CLK / LCDVD[12]	L18	P0.7 / I2S0TX_WS / LCDVD[13]
Row M					
M1	EMC_A[02] / P1.2	M2	EMC_A[03] / P1.3	M3	EMC_A[04] / P1.4
M4	EMC_A[08] / P1.8	M5	VSS_EMC	M6	VDD_EMC
M7	VDD_CORE12	M8	VDD_EMC	M9	VSS_CORE
M10	VSS_CORE	M11	VDD_CORE12	M12	VSS_CORE
M13	VDD_COREFXD	M14	RESET_N	M15	ONSW
M16	GPO_23 / U2_HRTS / U3_RTS	M17	P0.2 / I2S0RX_SDA / LCDVD[4]	M18	P0.3 / I2S0RX_CLK / LCDVD[5]
Row N					
N1	EMC_A[05] / P1.5	N2	EMC_A[06] / P1.6	N3	EMC_A[07 / P1.7
N4	EMC_A[12] / P1.12	N5	VSS_EMC	N6	VSS_EMC
N7	VDD_EMC	N8	VDD_EMC	N9	VDD_EMC
N10	VDD_EMC	N11	VDD_EMC	N12	VDD_AD
N13	VDD_AD	N14	VDD_FUSE	N15	VDD_RTCOSC
N16	GPI_05 / U3_DCD	N17	GPI_28 / U3_RI	N18	GPO_17

Table 3. Pin Allocation Table SOT1048-1 (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
Row P					
P1	EMC_A[09] / P1.9	P2	EMC_A[10] / P1.10	P3	EMC_A[11] / P1.11
P4	EMC_DQM[1]	P5	EMC_DQM[3]	P6	VSS_EMC
P7	VSS_EMC	P8	VSS_EMC	P9	VSS_EMC
P10	VSS_EMC	P11	VSS_EMC	P12	EMC_BLS[3]
P13	VSS_AD	P14	VSS_OSC	P15	VDD_PLLUSB
P16	RTCX_IN	P17	RTCX_OUT	P18	VSS_RTCOSC
Row R					
R1	EMC_A[13] / P1.13	R2	EMC_A[14] / P1.14	R3	EMC_DQM[0]
R4	EMC_WR_N	R5	EMC_CAS_N	R6	EMC_DYCS0_N
R7	EMC_D[01]	R8	EMC_D[07]	R9	EMC_D[17]/ DDR_DQS1
R10	EMC_D[24] / P2.5	R11	EMC_CS1_N	R12	EMC_BLS[2]
R13	TS_XP	R14	PLL397_LOOP	R15	SYSX_OUT
R16	VSS_PLLUSB	R17	VDD_PLLHCLK	R18	VSS_PLLHCLK
Row T					
T1	EMC_DQM[2]	T2	EMC_RAS_N	T3	EMC_CLK
T4	EMC_CLKIN	T5	EMC_D[02]	T6	EMC_D[06]
T7	EMC_D[11]	T8	EMC_D[14]	T9	EMC_D[20] / P2.1
T10	EMC_D[23] / P2.4	T11	EMC_D[27] / P2.8	T12	EMC_CS2_N
T13	EMC_BLS[1]	T14	ADIN1 (TS_YP)	T15	VSS_PLL397
T16	VDD_PLL397	T17	SYSX_IN	T18	VDD_OSC
Row U					
		U2	N.C.	U3	EMC_CKE0
U4	EMC_D[00]	U5	EMC_D[03]	U6	EMC_D[09]
U7	EMC_D[12]	U8	EMC_D[15]	U9	EMC_D[19] / P2.0
U10	EMC_D[22] / P2.3	U11	EMC_D[26] / P2.7	U12	EMC_D[30] / P2.11
U13	EMC_CS0_N	U14	EMC_BLS[0]	U15	ADIN0 (TS_XP)
U16	TS_YP	U17	N.C.		
Row V					
				V3	EMC_D[04]
V4	EMC_D[05]	V5	EMC_D[08]	V6	EMC_D[10]
V7	EMC_D[13]	V8	EMC_D[16]/ DDR_DQS0	V9	EMC_D[18]/ DDR_NCLK
V10	EMC_D[21] / P2.2	V11	EMC_D[25] / P2.6	V12	EMC_D[28] / P2.9
V13	EMC_D[29] / P2.10	V14	EMC_D[31] / P2.12	V15	EMC_CS3_N
V16	ADIN2 (TS_AUX_IN)				

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
ADIN0 (TS_XM)	U15	VDD_AD	analog in	input	ADC input 0, Touch Screen X minus
ADIN1 (TS_YM)	T14	VDD_AD	analog in	input	ADC input 1, Touch Screen Y minus
ADIN2 (TS_AUX_IN)	V16	VDD_AD	analog in	input	ADC input 2, Touch Screen AUX input
DBGEN	G14	VDD_IOD	I : PD	input	Device test input (JTAG select)
EMC_A[00] / P1.0	L3	VDD_EMC	I/O	L	EMC address bit 0
			I/O		Port 1 bit 0
EMC_A[01] / P1.1	L4	VDD_EMC	I/O	L	EMC address bit 1
			I/O		Port 1 bit 1
EMC_A[02] / P1.2	M1	VDD_EMC	I/O	L	EMC address bit 2
			I/O		Port 1 bit 2
EMC_A[03] / P1.3	M2	VDD_EMC	I/O	L	EMC address bit 3
			I/O		Port 1 bit 3
EMC_A[04] / P1.4	M3	VDD_EMC	I/O	L	EMC address bit 4
			I/O		Port 1 bit 4
EMC_A[05] / P1.5	N1	VDD_EMC	I/O	L	EMC address bit 5
			I/O		Port 1 bit 5
EMC_A[06] / P1.6	N2	VDD_EMC	I/O	L	EMC address bit 6
			I/O		Port 1 bit 6
EMC_A[07 / P1.7	N3	VDD_EMC	I/O	L	EMC address bit 7
			I/O		Port 1 bit 7
EMC_A[08] / P1.8	M4	VDD_EMC	I/O	L	EMC address bit 8
			I/O		Port 1 bit 8
EMC_A[09] / P1.9	P1	VDD_EMC	I/O	L	EMC address bit 9
			I/O		Port 1 bit 9
EMC_A[10] / P1.10	P2	VDD_EMC	I/O	L	EMC address bit 10
			I/O		Port 1 bit 10
EMC_A[11] / P1.11	P3	VDD_EMC	I/O	L	EMC address bit 11
			I/O		Port 1 bit 11
EMC_A[12] / P1.12	N4	VDD_EMC	I/O	L	EMC address bit 12
			I/O		Port 1 bit 12
EMC_A[13] / P1.13	R1	VDD_EMC	I/O	L	EMC address bit 13
			I/O		Port 1 bit 13
EMC_A[14] / P1.14	R2	VDD_EMC	I/O	L	EMC address bit 14
			I/O		Port 1 bit 14
EMC_A[15] / P1.15	L1	VDD_EMC	I/O	L	EMC address bit 15
			I/O		Port 1 bit 15
EMC_A[16] / P1.16	K3	VDD_EMC	I/O	L	EMC address bit 16
			I/O		Port 1 bit 16

Table 4. Pin description *...continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
EMC_A[17] / P1.17	K4	VDD_EMC	I/O	L	EMC address bit 17
			I/O		Port 1 bit 17
EMC_A[18] / P1.18	K2	VDD_EMC	I/O	L	EMC address bit 18
			I/O		Port 1 bit 18
EMC_A[19] / P1.19	K1	VDD_EMC	I/O	L	EMC address bit 19
			I/O		Port 1 bit 19
EMC_A[20] / P1.20	J1	VDD_EMC	I/O	L	EMC address bit 20
			I/O		Port 1 bit 20
EMC_A[21] / P1.21	J2	VDD_EMC	I/O	L	EMC address bit 21
			I/O		Port 1 bit 21
EMC_A[22] / P1.22	J3	VDD_EMC	I/O	L	EMC address bit 22
			I/O		Port 1 bit 22
EMC_A[23] / P1.23	J4	VDD_EMC	I/O	L	EMC address bit 23
			I/O		Port 1 bit 23
EMC_BLS[0]	U14	VDD_EMC	O	H	Static memory byte lane 0 select
EMC_BLS[1]	T13	VDD_EMC	O	H	Static memory byte lane 1 select
EMC_BLS[2]	R12	VDD_EMC	O	H	Static memory byte lane 2 select
EMC_BLS[3]	P12	VDD_EMC	O	H	Static memory byte lane 3 select
EMC_CAS_N	R5	VDD_EMC	O	H	SDRAM column addr strobe out, active low
EMC_CKE0	U3	VDD_EMC	O	L	Clock enable out for SDRAM bank 0
EMC_CKE1	L2	VDD_EMC	O	L	Clock enable out for SDRAM bank 1
EMC_CLK	T3	VDD_EMC	O	L/R	SDRAM clock out
EMC_CLKIN	T4	VDD_EMC	I	input	SDRAM clock feedback
EMC_CS0_N	U13	VDD_EMC	O	H	EMC static memory chip select 0
EMC_CS1_N	R11	VDD_EMC	O	H	EMC static memory chip select 1
EMC_CS2_N	T12	VDD_EMC	O	H	EMC static memory chip select 2
EMC_CS3_N	V15	VDD_EMC	O	H	EMC static memory chip select 3
EMC_D[00]	U4	VDD_EMC	I/O [1]	input	EMC data bit 0
EMC_D[01]	R7	VDD_EMC	I/O [1]	input	EMC data bit 1
EMC_D[02]	T5	VDD_EMC	I/O [1]	input	EMC data bit 2
EMC_D[03]	U5	VDD_EMC	I/O [1]	input	EMC data bit 3
EMC_D[04]	V3	VDD_EMC	I/O [1]	input	EMC data bit 4
EMC_D[05]	V4	VDD_EMC	I/O [1]	input	EMC data bit 5
EMC_D[06]	T6	VDD_EMC	I/O [1]	input	EMC data bit 6
EMC_D[07]	R8	VDD_EMC	I/O[1]	input	EMC data bit 7
EMC_D[08]	V5	VDD_EMC	I/O [1]	input	EMC data bit 8
EMC_D[09]	U6	VDD_EMC	I/O [1]	input	EMC data bit 9
EMC_D[10]	V6	VDD_EMC	I/O [1]	input	EMC data bit 10
EMC_D[11]	T7	VDD_EMC	I/O [1]	input	EMC data bit 11
EMC_D[12]	U7	VDD_EMC	I/O[1]	input	EMC data bit 12

Table 4. Pin description *...continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
EMC_D[13]	V7	VDD_EMC	I/O [1]	input	EMC data bit 13
EMC_D[14]	T8	VDD_EMC	I/O [1]	input	EMC data bit 14
EMC_D[15]	U8	VDD_EMC	I/O [1]	input	EMC data bit 15
EMC_D[16]/ DDR_DQS0	V8	VDD_EMC	I/O [1]	input	EMC data bit 16, DDR data strobe 0 I/O
EMC_D[17]/ DDR_DQS1	R9	VDD_EMC	I/O [1]	input	EMC data bit 17, DDR data strobe 1 I/O
EMC_D[18]/ DDR_NCLK	V9	VDD_EMC	I/O	input	EMC data bit 18, DDR inverted clock out
EMC_D[19] / P2.0	U9	VDD_EMC	I/O	input	EMC data bit 19
			I/O		parallel I/O bit 0
EMC_D[20] / P2.1	T9	VDD_EMC	I/O	input	EMC data bit 20
			I/O		parallel I/O bit 1
EMC_D[21] / P2.2	V10	VDD_EMC	I/O	input	EMC data bit 21
			I/O		parallel I/O bit 2
EMC_D[22] / P2.3	U10	VDD_EMC	I/O	input	EMC data bit 22
			I/O		parallel I/O bit 3
EMC_D[23] / P2.4	T10	VDD_EMC	I/O	input	EMC data bit 23
			I/O		parallel I/O bit 4
EMC_D[24] / P2.5	R10	VDD_EMC	I/O	input	EMC data bit 24
			I/O		parallel I/O bit 5
EMC_D[25] / P2.6	V11	VDD_EMC	I/O	input	EMC data bit 25
			I/O		parallel I/O bit 6
EMC_D[26] / P2.7	U11	VDD_EMC	I/O	input	EMC data bit 26
			I/O		parallel I/O bit 7
EMC_D[27] / P2.8	T11	VDD_EMC	I/O	input	EMC data bit 27
			I/O		parallel I/O bit 8
EMC_D[28] / P2.9	V12	VDD_EMC	I/O	input	EMC data bit 28
			I/O		parallel I/O bit 9
EMC_D[29] / P2.10	V13	VDD_EMC	I/O	input	EMC data bit 29
			I/O		parallel I/O bit 10
EMC_D[30] / P2.11	U12	VDD_EMC	I/O	input	EMC data bit 30
			I/O		parallel I/O bit 11
EMC_D[31] / P2.12	V14	VDD_EMC	I/O	input	EMC data bit 31
			I/O		parallel I/O bit 12
EMC_DQM[0]	R3	VDD_EMC	O	L	SDRAM data mask 0 out
EMC_DQM[1]	P4	VDD_EMC	O	L	SDRAM data mask 1 out
EMC_DQM[2]	T1	VDD_EMC	O	L	SDRAM data mask 2 out
EMC_DQM[3]	P5	VDD_EMC	O	L	SDRAM data mask 3 out
EMC_DYCS0_N	R6	VDD_EMC	O	H	SDRAM active low chip select 0
EMC_DYCS1_N	G1	VDD_EMC	O	H	SDRAM active low chip select 1

Table 4. Pin description *…continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
EMC_OE_N	H1	VDD_EMC	O	H	EMC static memory output enable
EMC_RAS_N	T2	VDD_EMC	O	H	SDRAM row address strobe, active low
EMC_WR_N	R4	VDD_EMC	O	H	EMC write strobe, active low
FLASH_ALE	D2	VDD_IOC	O	L	Flash address latch enable
FLASH_CE_N	E3	VDD_IOC	O	H	Flash chip enable
FLASH_CLE	F3	VDD_IOC	O	L	Flash command latch enable
FLASH_IO[00]	H2	VDD_IOC	I/O [1]	input	Flash data bus, bit 0
FLASH_IO[01]	H3	VDD_IOC	I/O [1]	input	Flash data bus, bit 1
FLASH_IO[02]	F1	VDD_IOC	I/O [1]	input	Flash data bus, bit 2
FLASH_IO[03]	E1	VDD_IOC	I/O [1]	input	Flash data bus, bit 3
FLASH_IO[04]	H4	VDD_IOC	I/O [1]	input	Flash data bus, bit 4
FLASH_IO[05]	G2	VDD_IOC	I/O [1]	input	Flash data bus, bit 5
FLASH_IO[06]	G3	VDD_IOC	I/O [1]	input	Flash data bus, bit 6
FLASH_IO[07]	E2	VDD_IOC	I/O [1]	input	Flash data bus, bit 7
FLASH_RD_N	C1	VDD_IOC	O	H	Flash read enable
FLASH_RDY	D1	VDD_IOC	I	input	Flash ready (from Flash device)
FLASH_WR_N	F2	VDD_IOC	O	H	Flash write enable
GPI_00 / ENET_RXD2	C16	VDD_IOD	I	input	GP input 00
			I		Ethernet receive data 2
GPI_01 / SERVICE_N	C15	VDD_IOD	I	input	GP input 01
			I		boot select input
GPI_02 / CAP2.0 / ENET_RXD3	C14	VDD_IOD	I	input	GP input 02
			I		Timer 2 Cap 0
			I		Ethernet receive data 3
GPI_03	F4	VDD_IOC	I	input	GP input 03
GPI_04 / SPI1_BUSY	E13	VDD_IOD	I	input	GP input 04
			I		SPI1 busy input
GPI_05 / U3_DCD	N16	VDD_IOA	I	input	GP input 05
			I		Uart 3 data carrier detect input
GPI_06 / HSTIM_CAP / I2S1RX_SDA	C7	VDD_IOB	I	input	GP input 06
			I		HS timer capture input
			I		I2S1 receive data
GPI_07 / PCAP3.0	D13	VDD_IOD	I	input	GP input 07
			I	input	PWM3 capture/clock input
GPI_08 / KEY_COL6 / SPI2_BUSY / ENET_RX_DV	B16	VDD_IOD	I	input	GP input 08
			I		keyscan column 6 input
			I		SPI2 busy input
			I		Ethernet receive data valid input

Table 4. Pin description *…continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
GPI_09 / KEY_COL7 / ENET_COL	L2	VDD_IOD	I	input	GP input 09
			I		keyscan column 7 input
			I		Ethernet collision input
GPI_19 / U4_RX	B15	VDD_IOD	I	input	GP input 10
			I		Uart 4 receive
GPI_28 / U3_RI	N17	VDD_IOA	I	input	GP input 11
			I		Uart 3 ring indicator input
GPIO_00	A12	VDD_IOD	I/O	input	GP I/O 00
GPIO_01	A11	VDD_IOD	I/O	input	GP I/O 01
GPIO_02 / KEY_ROW6 / ENET_MDC	D9	VDD_IOD	I/O	input	GP I/O 02
			O		keyscan row 6 output
			O		Ethernet PHY interface clock
GPIO_03 / KEY_ROW7 / ENET_MDIO	C11	VDD_IOD	I/O	input	GP I/O 03
			I/O		keyscan row 7 output
			I/O		Ethernet PHY interface data
GPIO_04 / SSEL1 / LCDVD[22]	B11	VDD_IOD	I/O	input	GP I/O 04
			I/O		SSP1 Slave Select
			I/O		LCD data bit 22
GPIO_05 / SSEL0	E9	VDD_IOD	I/O	input	GP I/O 05
			I/O		SSP0 Slave Select
GPO_00 / TST_CLK1	C3	VDD_IOC	O	L	GP out 00
					test clock 1 out
GPO_01	D4	VDD_IOC	O	L	GP out 01
GPO_02 / MAT1.0 / LCDVD[0]	B14	VDD_IOD	O	L	GP out 02
			O	L	Timer 1 Match 0
			O	L	LCD data bit 0
GPO_03 / LCDVD[1]	D12	VDD_IOD	O	H	GP out 03
			O		LCD data bit 1
GPO_04	D8	VDD_IOB	O	L	GP out 04
GPO_05	B3	VDD_IOC	O	H	GP out 05
GPO_06 / PWM4.3 / LCDVD[18]	A16	VDD_IOD	O	L	GP out 06
			O		PWM4 out 3
			O		LCD data bit 18
GPO_07 / LCDVD[2]	A15	VDD_IOD	O	H	GP out 07
			O		LCD data bit 2
GPO_08 / PWM4.2 / LCDVD[8]	C13	VDD_IOD	O	L	GP out 08
			O		PWM4 out 2
			O		LCD data bit 8

Table 4. Pin description *...continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
GPO_09 / PWM4.1 / LCDVD[9]	C12	VDD_IOD	O	L	GP out 09
			O		PWM4 out 1
			O		LCD data bit 9
GPO_10 / PWM3.6 / LCDPWR	E11	VDD_IOD	O	L	GP out 10
			O		PWM3 out 6
			O		LCD panel power enable
GPO_11	E8	VDD_IOB	O	L	GP out 11
GPO_12 / PWM3.5 / LCDLE	B12	VDD_IOD	O	L	GP out 12
			O		PWM3 out 5
			O		LCD line end signal
GPO_13 / PWM3.4 / LCDDCLK	B13	VDD_IOD	O	L	GP out 13
			O		PWM3 out 4
			O		LCD clock output
GPO_14	D3	VDD_IOC	O	L	GP out 14
GPO_15 / PWM3.3 / LCDFP	A14	VDD_IOD	O	L	GP out 15
			O		PWM3 out 3
			O		LCD frame/sync pulse
GPO_16 / PWM3.2 / LCDENAB / LCDM	D10	VDD_IOD	O	L	GP out 16
			O		PWM3 out 2
			O		LCD STN AC bias / TFT data enable
GPO_17	N18	VDD_IOA	O	L	GP out 17
GPO_18 / PWM3.1 / LCDLP	D11	VDD_IOD	O	L	GP out 18
			O		PWM3 out 1
			O		LCD line sync / horizontal sync
GPO_19	C2	VDD_IOC	O	L	GP out 19
GPO_20	B2	VDD_IOC	O	H	GP out 20
GPO_21 / U4_TX / LCDVD[3]	A13	VDD_IOD	O	L	GP out 21
			O		Uart 4 transmit
			O		LCD data bit 3
GPO_22 / U7_HRTS / LCDVD[14]]	E10	VDD_IOD	O	L	GP out 22
			O		HS Uart 7 RTS out
			O		LCD data bit 14
GPO_23 / U2_HRTS / U3_RTS	M16	VDD_IOA	O	L	GP out 23
			O		HS Uart 2 RTS out
			O		Uart 3 RTS out
HIGHCORE / LCDVD[17]	H16	VDD_IOD	O	L	Core voltage control out
			O		LCD data bit 17
I2C1_SCL	A5	VDD_IOB	I/O	T	I2C1 serial clock input/output
I2C1_SDA	B6	VDD_IOB	I/O	T	I2C1 serial data input/output
I2C2_SCL	A3	VDD_IOC	I/O	T	I2C2 serial clock input/output

Table 4. Pin description *...continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
I2C2_SDA	E4	VDD_IOC	I/O	T	I2C2 serial data input/output
I2S1TX_CLK / MAT3.0	A4	VDD_IOB	I/O	L	I2S1 transmit clock
			I/O		Timer 3 Match 0
I2S1TX_SDA / MAT3.1	E7	VDD_IOB	I/O	input	I2S1 transmit data
			I/O		Timer 3 Match 1
I2S1TX_WS / CAP3.0	B4	VDD_IOB	I/O	input	I2S1 transmit word select
			I/O		Timer 3 Cap 0
JTAG_NTRST	H17	VDD_IOD	I : PU	input	JTAG1 reset input
JTAG_RTCK	H18	VDD_IOD	O	L	JTAG1 return clock out
JTAG_TCK	H14	VDD_IOD	I	input	JTAG1 clock input
JTAG_TDI	J16	VDD_IOD	I : PU	input	JTAG1 data input
JTAG_TDO	J15	VDD_IOD	O	L	JTAG1 data out
JTAG_TMS	G18	VDD_IOD	I : PU	input	TAG1 test mode select input
KEY_COL0 / ENET_TX_CLK	F15	VDD_IOD	I	input	Keyscan column 0 input
			I		Ethernet transmit clock
KEY_COL1 / ENET_RX_CLK / ENET_REF_CLK	E16	VDD_IOD	I	input	Keyscan column 1 input,
			I		Ethernet receive clock (MII mode)
			I		Ethernet reference clock (RMII mode)
KEY_COL2 / ENET_RX_ER	D17	VDD_IOD	I	input	Keyscan column 2 input
			I		Ethernet receive error input
KEY_COL3 / ENET_CRS	D18	VDD_IOD	I	input	Keyscan column 3 input
			I		Ethernet carrier sense input
KEY_COL4 / ENET_RXD0	G15	VDD_IOD	I	input	Keyscan column 4 input
			I		Ethernet receive data 0
KEY_COL5 / ENET_RXD1	F16	VDD_IOD	I	input	Keyscan column 5 input
			I		Ethernet receive data 1
KEY_ROW0 / ENET_TX_ER	E15	VDD_IOD	I/O	H	Keyscan row 0 out
			I/O		Ethernet transmit error
KEY_ROW1 / ENET_TXD2	E14	VDD_IOD	I/O	H	Keyscan row 1 out
			I/O		Ethernet transmit data 2
KEY_ROW2 / ENET_RXD3	F14	VDD_IOD	I/O	H	Keyscan row 2 out
			I/O		Ethernet transmit data 3
KEY_ROW3 / ENET_TX_EN	D16	VDD_IOD	I/O	H	Keyscan row 3 out
			I/O		Ethernet transmit enable
KEY_ROW4 / ENET_TXD0	C17	VDD_IOD	I/O	H	Keyscan row 4 out
			I/O		Ethernet transmit data 0
KEY_ROW5 / ENET_TXD1	C18	VDD_IOD	I/O	H	Keyscan row 5 out
			I/O		Ethernet transmit data 1

Table 4. Pin description *…continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
MS_BS / MAT2.1 / PWM3.6	A6	VDD_IOD	I/O	L	MS/SD card command out
			I/O		Timer 2 Match 1
			I/O		PWM3.6 output
MS_DIO0 / MAT0.0 / PWM3.1	A8	VDD_IOD	I/O	input	MS/SD card data 0
			I/O		Timer 0 Match 0
			I/O		PWM3.1 out
MS_DIO1 / MAT0.1 / PWM3.2	A7	VDD_IOD	I/O	input	MS/SD card data 1
			I/O		Timer 0 Match 1
			I/O		PWM3.2 out
MS_DIO2 / MAT0.2 / PWM3.3	B8	VDD_IOD	I/O	input	MS/SD card data 2
			I/O		Timer 0 Match 2
			I/O		PWM3.3 out
MS_DIO3 / MAT0.3 / PWM3.4	C8	VDD_IOD	I/O	input	MS/SD card data 3
			I/O		Timer 0 Match 3
			I/O		PWM3.4 out
MS_SCLK / MAT2.0 / PWM3.5	B7	VDD_IOD	I/O	L	MS/SD card clock out
			I/O		Timer 2 Match 0
			I/O		PWM3.5 output
N.C.	B17	-			pin not connected
N.C.	U17	-			pin not connected
N.C.	U2	-			pin not connected
ONSW	M15	VDD_RTC	O	L	RTC match out for external power control
P0.0 / I2S1RX_CLK	B5	VDD_IOB	I/O	input	Port 0 bit 0
			I/O		I2S1 receive clock
P0.1 / I2S1RX_WS	D7	VDD_IOB	I/O	input	Port 0 bit 1
			I/O		I2S1 receive word select
P0.2 / I2S0RX_SDA / LCDVD[4]	M17	VDD_IOA	I/O	input	Port 0 bit 2
			I/O		I2S0 receive data
			I/O		LCD data bit 4
P0.3 / I2S0RX_CLK / LCDVD[5]	M18	VDD_IOA	I/O	input	Port 0 bit 3
			I/O		I2S0 receive clock
			I/O		LCD data bit 5
P0.4 / I2S0RX_WS / LCDVD[6]	L15	VDD_IOA	I/O	input	Port 0 bit 4
			I/O		I2S0 receive word select
			I/O		LCD data bit 6
P0.5 / I2S0TX_SDA / LCDVD[7]	L16	VDD_IOA	I/O	input	Port 0 bit 5
			I/O		I2S0 transmit data
			I/O		LCD data bit 7

Table 4. Pin description *...continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
P0.6 / I2S0TX_CLK / LCDVD[12]	L17	VDD_IOA	I/O	input	Port 0 bit 6
			I/O		I2S0 transmit clock
			I/O		LCD data bit 12
P0.7 / I2S0TX_WS / LCDVD[13]	L18	VDD_IOA	I/O	input	Port 0 bit 7
			I/O		I2S0 transmit word select
			I/O		LCD data bit 13
PLL397_LOOP	R14	VDD_AD	analog filter		PLL397 loop filter (for external components)
PWM_OUT1 / LCDVD[16]	D14	VDD_IOD	O	L	PWM1 out
			O		LCD data bit 16
PWM_OUT2 / LCDVD[19]	D15	VDD_IOD	O	L	PWM2 out
			O		internal irq/fiq status
			O		LCD data bit 19
RESET_N	M14	VDD_RTC	I	input	Reset input, active low
RESOUT_N	G4	VDD_IOC	O	L/H	Reset out. Reflects external & WDT reset
RTCX_IN	P16	VDD_RTC	analog in	input	RTC oscillator input
RTCX_OUT	P17	VDD_RTC	analog out	output	RTC oscillator output
SPI1_CLK / SCK0	C9	VDD_IOD	O	input	SPI1 clock out
			O		SSP0 clock out
SPI1_DATIN / MISO0 / GPI_25	C10	VDD_IOD	I/O	input	SPI1 data in
			I/O		SSP0 MISO
			I/O		GPI bit 25
SPI1_DATIO / MOSI0	B9	VDD_IOD	I/O	input	SPI1 data out (and opt. input)
			I/O		SSP0 MOSI
SPI2_CLK / SCK1 / LCDVD[23]	B10	VDD_IOD	I/O	input	SPI2 clock out
			I/O		SSP1 clock out
			I/O		LCD data bit 23
SPI2_DATIO / MOSI1 / LCDVD[20]	A9	VDD_IOD	I/O	input	SPI2 data out (and opt. input)
			I/O		SSP1 MOSI
			I/O		LCD data bit 20
SPI2_DATIN / MISO1 / LCDVD[21] / GPI_27	A10	VDD_IOD	I/O	input	SPI2 data in
			I/O		SSP1 MISO
			I/O		LCD data 21
			I/O		GPI bit 27
SYSCLKEN / LCDVD[15]	G17	VDD_IOD	I/O	H	Clock request out for external clock source
			I/O		LCD data bit 15
SYSX_IN	T17	VDD_AD	analog in	input	System clock oscillator input
SYSX_OUT	R15	VDD_AD	analog out	output	System clock oscillator output
TS_XP	R13	VDD_AD	I/O	T	Touchscreen X output
TS_YP	U16	VDD_AD	I/O	T	Touchscreen Y output

Table 4. Pin description *...continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
TST_CLK2	C6	VDD_IOB	O	L	Test clock 2 out
U1_RX / CAP1.0 / GPI_15	K15	VDD_IOA	I/O	input	HS Uart 1 receive
			I/O		Timer 1 Cap 0
			I/O		GPI bit 15
U1_TX	K16	VDD_IOA	O	H	HS Uart 1 transmit
U2_HCTS / U3_CTS / GPI_16	J18	VDD_IOA	I/O	input	HS Uart 2 Clear to Send input
			I		Uart 3 Clear to Send
			I/O		GPI bit 16
U2_RX / U3_DSR / GPI_17	K18	VDD_IOA	I/O	input	HS Uart 2 receive
			I/O		Uart 3 data set ready
			I/O		GPI bit 17
U2_TX / U3_DTR	K17	VDD_IOA	O	H	HS Uart 2 transmit
			O		Uart 3 data terminal ready out
U3_RX / GPI_18	J14	VDD_IOA	I/O	input	Uart 3 receive
			I/O		GPI bit 18
U3_TX	J17	VDD_IOA	O	H	Uart 3 transmit
U5_RX / GPI_20	F18	VDD_IOD	I/O	input	Uart 5 receive
			I		GPI bit 20
U5_TX	H15	VDD_IOD	O	H	Uart 5 transmit
U6_IRRX / GPI_21	F17	VDD_IOD	I/O	input	Uart 6 receive (with IrDA)
			I		GPI bit 21
U6_IRTX	G16	VDD_IOD	O	L	Uart 6 transmit (with IrDA)
U7_HCTS / CAP0.1 / LCDCLKIN / GPI_22	G13	VDD_IOD	I	input	HS Uart 7 CTS in
			I		Timer 0 Cap 1
			I		LCD panel clk in
			I		GPI bit 22
U7_RX / CAP0.0 / LCDVD[10] / GPI_23	E17	VDD_IOD	I/O	input	HS Uart 7 receive
			I/O		Timer 0 Cap 0
			I/O		LCD data bit 10
			I/O		GPI bit 23
U7_TX / MAT1.1 / LCDVD[11]	E18	VDD_IOD	O	H	HS Uart 7 transmit
			O		Timer 1 Match 1
			O		LCD data bit 11
USB_ATX_INT_N	C4	VDD_IOC	I	input	Interrupt from USB ATX
USB_DAT_VP / U5_RX	D5	VDD_IOC	I/O	input	USB transmit data, D+ receive
			I/O		Uart 5 receive
USB_I2C_SCL	E5	VDD_IOC	I/O	T	I2C clock for USB ATX interface
USB_I2C_SDA	E6	VDD_IOC	I/O	T	I2C data for USB ATX interface
USB_OE_TP_N	D6	VDD_IOC	I/O	H	USB transmit enable for DAT/SE0

Table 4. Pin description *...continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
USB_SE0_ VM / U5_TX	C5	VDD_IOC	I/O	input	USB single ended zero transmit, D- Receive
			I/O	input	Uart 5 transmit
VDD_AD	N12, N13	VDD_AD	power	-	2.8V supply for ADC (TS)
VDD_CORE	G7, G9, G11, J7, J12, M7, M11	VDD_CORE	power		1.2V (or 0.9V) supply for core
VDD_COREFXD	L12, M13	VDD_COREFXD	power		Fixed 1.2V supply for core
VDD_EMC	J6, K6, K7, L6, M6, M8, N7, N8, N9 N10, N11	VDD_EMC	power		1.8V supply for External Memory Controller (EMC)
VDD_FUSE	N14	VDD_FUSE	power		Fuse VPP supply
VDD_IOA	H13, J13	VDD_IOA	power		1.8V to 3V Supply for IOA Domain
VDD_IOB	F8	VDD_IOB	power		1.8V to 3V Supply for IOB Domain for GPI_06, GPO_04/11, I2C1
VDD_IOC	F7, G6, H6, J5	VDD_IOC	power		1.8V to 3V Supply for IOC Domain
VDD_IOD	F13, F9	VDD_IOD	power		1.8V to 3V Supply for IOD Domain
VDD_OSC	T18	VDD_IOD	power		1.2V supply for main oscillator
VDD_PLL397	T16	VDD_PLL397	power		1.2V supply for 397x PLL
VDD_PLLHCLK	R17	VDD_PLLHCLK	power		1.2V supply for HCLK PLL
VDD_PLLUSB	P15	VDD_PLLUSB	power		1.2V supply for USB PLL
VDD_RTC	K14	VDD_RTC	power		1.2V supply for RTC I/O
VDD_RTCCORE	L13	VDD_RTCCORE	power		1.2V supply for RTC
VDD_RTCOSC	N15	VDD_RTCOSC	power		1.2V supply for RTC oscillator
VSS_AD	P13		power		Ground for ADC (Touchscreen)

Table 4. Pin description *...continued*

Symbol	Pin	Power Supply Domain	Type	Reset state	Description
VSS_CORE	G8, G10, G12, H7, K12, L7, M9, M10, M12		power		Ground for core
VSS_EMC	K5, L5, M5, N5, N6, P6, P7, P8, P9, P10, P11		power		Ground for EMC
VSS_IOA	K13		power		Ground for 1.8V or 3V I/O
VSS_IOB	F6		power		Ground for 1.8V or 3V I/O for GPI_06, GPO_04/11, I2C1
VSS_IOC	F5, G5, H5		power		Ground IOC Domain
VSS_IOD	F10, F11, F12, H12		power		Ground IOD Domain
VSS_OSC	P14		power		Ground for main oscillator
VSS_PLL397	T15		power		Ground for 397x PLL
VSS_PLLHCLK	R18		power		Ground for HCLK PLL
VSS_PLLUSB	R16		power		Ground for USB PLL
VSS_RTCCORE	L14		power		Ground for RTC
VSS_RTCOSC	P18		power		Ground for RTC oscillator

[1] BK: pin has a bus keeper function that weakly retains the last level driven on an I/O pin when it is switched from output to input.

7. Functional description

7.1 CPU and Subsystems

7.1.1 CPU

NXP created the LPC32x0 family using an ARM926EJ-S CPU core that includes a Harvard architecture and a 5-stage pipeline. To this ARM core, NXP implemented a 32KB Instruction Cache, a 32 KB Data Cache and a Vector Floating Point coprocessor. The ARM926EJ-S core also has an integral Memory Management Unit (MMU) to provide the virtual memory capabilities required to support the multi-programming demands of modern operating systems. The basic ARM926EJ-S core V5TE instruction set includes DSP instruction extensions for native Jazelle Java Byte-code execution in hardware. The LPC32x0 family operates at CPU frequencies up to 208 MHz.

7.1.2 Vector Floating Point (VFP) coprocessor

The LPC32x0 family includes a VFP co-processor providing full support for single-precision and double-precision add, subtract, multiply, divide, and multiply-accumulate operations at CPU clock speeds. It is compliant with the IEEE 754 standard for binary Floating-Point Arithmetic. This hardware floating point capability makes the microcontroller suitable for advanced Motor control and DSP applications. The VFP has 3 separate pipelines for Floating-point MAC operations, divide or square root operations, and Load/Store operations. These pipelines operate in parallel and can complete execution out of order. All single-precision instructions execute in one cycle, except the divide and square root instructions. All double-precision multiply and multiply-accumulate instructions take two cycles. The VFP also provides format conversions between floating-point and integer word formats.

7.1.3 Emulation and debugging

The LPC32x0 family supports emulation and debugging via a dedicated JTAG serial port. An Embedded Trace Buffer allows tracing program execution. The dedicated JTAG port allows debugging of all chip features without impact to any pins that may be used in the application.

Embedded ICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an Embedded ICE protocol converter. The Embedded ICE protocol converter converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or entering the debug state.

Embedded Trace Buffer

The Embedded Trace Module (ETM) is connected directly to the ARM core. It compresses the trace information and exports it through a narrow trace port. An internal Embedded Trace Buffer of 2 k $\times$ 24 bits captures the trace information under software debugger control. Data from the Embedded Trace Buffer is recovered by the debug software through the JTAG port.

The trace contains information about when the ARM core switches between states. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. For data accesses either data or address or both can be traced.

7.2 AHB matrix

The LPC32x0 family has a multi-layer AHB matrix for inter-block communication. AHB is an ARM defined high-speed bus, which is part of the ARM bus architecture. AHB is a high-bandwidth low-latency bus that supports multi-master arbitration and a bus grant/request mechanism. For systems that have only one (CPU), or two (CPU and DMA) bus masters a simple AHB works well. However, if a system requires multiple bus masters and the CPU needs access to external memory, a single AHB bus can cause a bottleneck.

To increase performance, the LPC32x0 family uses an expanded AHB architecture known as Multi-layer AHB. A Multi-layer AHB replaces the request/grant and arbitration mechanism used in a simple AHB with an interconnect matrix that moves arbitration out toward the slave devices. Thus, if a CPU and a DMA controller want access to the same memory, the interconnect matrix arbitrates between the two when granting access to the memory. This advanced architecture allows simultaneous access by bus masters to different resources with an increase in arbitration complexity. In this architectural implementation, removing guaranteed central arbitration and allowing more than one bus master to be active at the same time provides better overall microcontroller performance.

In the LPC32x0 family, the Multi-Layer AHB system has a separate bus for each of seven AHB Masters:

- CPU Data bus
- CPU Instruction bus
- General purpose DMA Master 0
- General purpose DMA Master 1
- Ethernet Controller
- USB Controller
- LCD Controller

There are no arbitration delays unless two masters attempt to access the same slave at the same time.

7.2.1 APB bus

Many peripheral functions are accessed by on-chip APB busses that are attached to the higher speed AHB bus. The APB bus performs reads and writes to peripheral registers in three peripheral clocks.

7.2.2 FAB bus

Some peripherals are placed on a special bus called FAB that allows faster CPU access to those peripheral functions. A write access to FAB peripherals takes a single AHB clock and a read access to FAB peripherals takes two AHB clocks.

7.3 Physical Memory map

The Physical memory map incorporates several distinct regions, as shown in Figure 3. When an application is running, the CPU interrupt vectors are re-mapped to allow them to reside in on-chip SRAM (IRAM).

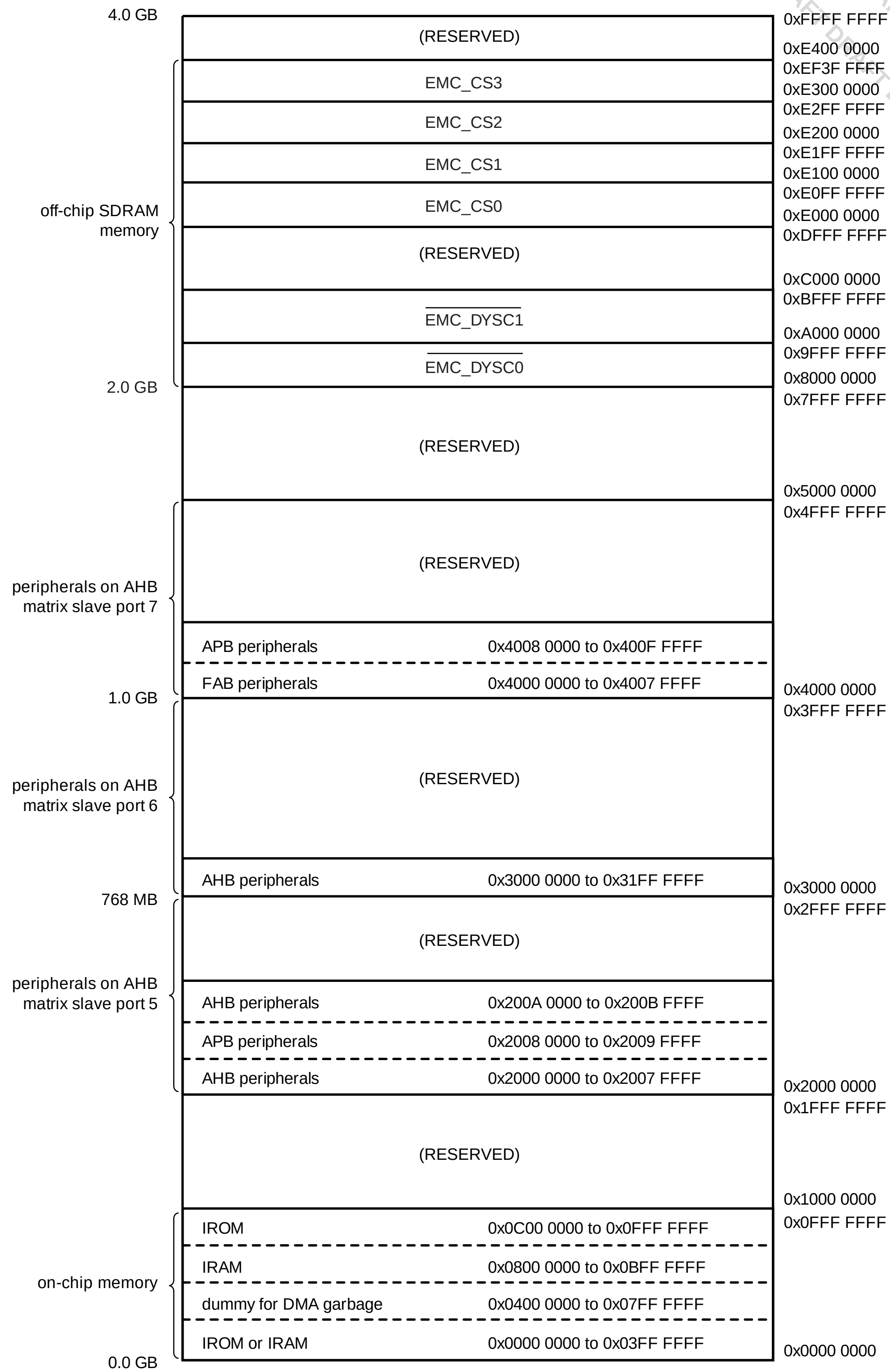


Fig 3. LPC32x0 family Memory map

7.4 Internal Memory

On-Chip ROM

The built-in 16 KB ROM contains a program which runs a boot procedure to load code from one of four external sources, UART5, SSP0 SPI, EMC Static CS0 memory, or NAND FLASH.

After reset, execution always begins from the internal ROM. The bootstrap software first reads the SERVICE_N input (GPI_01). If SERVICE_N is low, the bootstrap starts a service boot and can download a program over serial link UART5 to IRAM and transfer execution to the downloaded code.

If the SERVICE_N pin is high, the bootstrap routine jumps to normal boot. The normal boot process first tests SPI memory for boot information if present it uploads the boot code and transfers execution to the uploaded software. If the SPI is not present or no software is loaded, the bootloader will test the EMC Static CS0 memory for the presence of boot code and if present boots from static memory, If this test fails the boot loader will test external NAND Flash for boot code and boot if code is present.

The Boot loader consumes no user memory space because it is in ROM.

On-Chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8, 16, or 32 bit memory. The LPC32x0 family provides 256 KB of internal SRAM.

7.5 External Memory Interfaces

The LPC32x0 family includes three external memory interfaces, NAND Flash controllers, Secure Digital Memory Controller, and an external memory controller for SDRAM, DDR SDRAM, and Static Memory devices.

7.5.1 NAND flash controllers

The LPC32x0 family includes two NAND flash controllers, one for multi-level NAND flash devices and one for single-level NAND flash devices. The two NAND flash controllers use the same pins to interface to external NAND flash devices, so only one interface is active at a time.

Multi-Level Cell (MLC) NAND flash controller

The MLC NAND flash controller interfaces to either multi-level or single-level NAND flash devices. An external NAND flash device is used to allow the bootloader to automatically load a portion of the application code into internal SRAM for execution following reset.

The MLC NAND flash controller supports up to 2 Gbit devices with small (528 byte) or large (2114 byte) pages. Programmable NAND timing parameters allow support for a variety of NAND flash devices. A built-in Reed-Solomon encoder/decoder provides error detection and correction capability. A 528 byte data buffer reduces the need for CPU supervision during loading. The MLC NAND flash controller also provides DMA support.

Single-Level Cell (SLC) NAND flash controller

The SLC NAND flash controller interfaces to single-level NAND flash devices up to 2 Gbit in size. DMA page transfers are supported, including a 20 byte DMA read and write FIFO. Hardware support for ECC (Error Checking and Correction) is included for the main data area. Software can correct a single bit error.

7.5.2 SD card controller

The SD interface allows access to external SD memory cards. The SD card interface conforms to the SD Memory Card Specification Version 1.01.

Features

- 1-bit and 4-bit data line interface support.
- DMA is supported through the system DMA controller.
- Provides all functions specific to the SD memory card. These include the clock generation unit, power management control, command and data transfer.

7.5.3 External Memory Controller

The LPC32x0 family includes a memory controller that supports data bus SDRAM, DDR SDRAM, and Static memory devices. The memory controller provides an interface between the system bus and external (off-chip) memory devices.

The controller supports 16-bit and 32-bit wide SDR SDRAM devices of 64/128/256/512 Mbit in size, as well as 16-bit wide data bus DDR SDRAM devices of 64/128/256/512 Mbit in size. Two dynamic memory chip selects are supplied, supporting two groups of SDRAM

- DYCS0 in the address range 0x8000 0000 to 0x9FFF FFFF
- DYCS1 in the address range 0xA000 0000 to 0xBFFF FFFF

The memory controller also supports 8-bit, 16-bit, and 32-bit wide asynchronous static memory devices, including RAM, ROM, and Flash, with or without asynchronous page mode. Four static memory chip selects are supplied for SRAM devices.

- CS0 in the address range 0xE000 0000 to 0xE0FF FFFF
- CS1 in the address range 0xE100 0000 to 0xE1FF FFFF
- CS2 in the address range 0xE200 0000 to 0xE2FF FFFF
- CS3 in the address range 0xE300 0000 to 0xE3FF FFFF

The SDRAM controller uses three data ports to allow simultaneous requests from multiple on-chip AHB bus masters and has the following features.

- Dynamic memory interface supports SDRAM, DDR-SDRAM, and low-power variants.
- Read and write buffers to reduce latency and improve performance
- Static memory features include
  - asynchronous page mode read
  - programmable wait states
  - bus turnaround cycles
  - output enable and write enable delays
  - extended wait

- Power-saving modes dynamically control MPMCCKEOUT and MPMCCLKOUT
- Dynamic memory self-refresh mode supported by software
- Controller supports 2K, 4K, and 8K row address synchronous memory parts. That is, typical 512Mb, 256Mb, 128Mb, and 16Mb parts, with 8, 16, or 32 DQ (data) bits per device
- Two reset domains enable dynamic memory contents to be preserved over a soft reset
- This controller does NOT Support Synchronous static memory devices (burst mode devices)

7.6 AHB Master Peripherals

The LPC32x0 family implements four AHB master peripherals, which include a General Purpose Direct Memory Access (GPDMA) controller, a 10/100 Ethernet Media Access Controller (MAC), a Universal Serial Bus (USB) controller, and an LCD Controller. Each of these four peripherals contain an integral DMA controller optimized to support the performance demands of the peripheral.

7.6.1 General purpose DMA controller (GPDMA)

The GPDMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the same AHB master, or one area by each master. The DMA controller supports the following peripheral device transfers.

- Secure Digital (SD) Memory interface
- High Speed UART’s
- I2S0 and I2S1 Ports
- SPI1 and SPI2 Interfaces
- SSP0 and SSP1 interfaces
- Memory

The DMA controls eight DMA channels with hardware prioritization. The DMA controller interfaces to the system via two AHB bus masters, each with a full 32-bit data bus width. DMA operations may be set up for 8-bit, 16-bit, and 32-bit data widths, and can be either big-endian or little-endian. Incrementing or non-incrementing addressing for source and destination are supported, as well as programmable DMA burst size. Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.

7.6.2 Ethernet MAC

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU. The Ethernet DMA can access off-chip memory via the EMC, as well as the IRAM. The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4
  - Fully compliant with IEEE standard 802.3
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure
  - Flexible transmit and receive frame options
  - Virtual Local Area Network (VLAN) frame support
- Memory management
  - Independent transmit and receive buffers memory mapped to SRAM
  - DMA managers with scatter/gather DMA and arrays of frame descriptors
  - Memory traffic optimized by buffering and pre-fetching
- Enhanced Ethernet features:
  - Receive filtering
  - Multicast and broadcast frame support for both transmit and receive
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit
  - Selectable automatic transmit frame padding
  - Over-length frame support for both transmit and receive allows any length frames
  - Promiscuous receive mode
  - Automatic collision back-off and frame retransmission
  - Includes power management by clock switching. Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter
- Physical interface
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface

7.6.3 USB interface

The LPC32x0 family supports USB in either DEVICE, HOST, or OTG configuration.

7.6.3.1 USB DEVICE controller

The USB device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. The DMA controller when enabled transfers data between the endpoint buffer and the USB RAM.

Features

- Fully compliant with USB 2.0 full-speed specification.
- Supports 32 physical (16 logical) endpoints.
- Supports control, bulk, interrupt and isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint maximum packet size selection (up to USB maximum specification) by software at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints.
- One duplex DMA channel serves all endpoints.
- Allows dynamic switching between CPU controlled and DMA modes.
- Double buffer implementation for bulk and isochronous endpoints.

7.6.3.2 USB HOST controller

The host controller enables data exchange with various USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies to the OHCI specification.

Features

- OHCI compliant.
- OHCI specifies the operation and interface of the USB host controller and SW driver.
- The host controller has four USB states visible to the SW driver:
  - USBOperational: Process lists and generate SOF tokens.
  - USBReset: Forces reset signaling on the bus, SOF disabled.
  - USBSuspend: Monitor USB for wake-up activity.
  - USBResume: Forces resume signaling on the bus.
- HCCA register points to interrupt and isochronous descriptors list.
- ControlHeadED and BulkHeadED registers point to control and bulk descriptors list.

7.6.3.3 USB OTG Controller

USB OTG (On-The-Go) is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

Features

- Fully compliant with On-The-Go supplement to the USB Specification 2.0 Revision 1.0.

- Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices under software control. HNP is partially implemented in hardware.
- Provides programmable timers required for HNP and SRP.
- Supports slave mode operation through AHB slave interface.
- Supports the OTG ATX from NXP (ISP 1301) or any external CEA-2011OTG specification compliant ATX.

7.6.4 LCD Controller

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

Features

- AHB bus master interface to access frame buffer
- Setup and control via a separate AHB slave interface
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces
- Supports single and dual-panel color STN displays
- Supports Thin Film Transistor (TFT) color displays
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768
- Hardware cursor support for single-panel displays
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT
- 16 bpp true-color non-palettized, for color STN and TFT
- 24 bpp true-color non-palettized, for color TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM
- Frame, line, and pixel clock signals
- AC bias signal for STN, data enable signal for TFT panels
- Supports little and big-endian, and Windows CE data formats
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin

7.7 System Functions

To enhance the performance of the LPC32x0 family incorporates the following System Functions, an Interrupt Controller (INTC), a Watchdog timer, a Millisecond Timer, and several Power Control Features. These functions are described in the following sections

7.7.1 Interrupt controller

The interrupt controller is comprised of three basic interrupt controller blocks, supporting a total of 73 interrupt sources. Each interrupt source can be individually enabled/disabled and configured for high or low level triggering, or rising or falling edge triggering. Each interrupt may also be steered to either the FIQ or IRQ input of the ARM9. Raw interrupt status and masked interrupt status registers allow versatile condition evaluation. In addition to peripheral functions, each of the six general purpose input/output pins and 12 general purpose input pins are connected directly to the interrupt controller.

7.7.2 Watchdog timer

The watchdog timer block is clocked by the main peripheral clock, which clocks a 32-bit counter. A match register is compared to the Timer. When configured for watchdog functionality, a match drives the match output low. The match output is gated with an enable signal that gives the opportunity to generate two type of reset signal: one that only resets chip internally, and another that goes through a programmable pulse generator before it goes to the external pin RESOUT_N and to the internal chip reset.

Features

- Programmable 32-bit timer.
- Internally resets the device if not periodically reloaded.
- Flag to indicate that a watchdog reset has occurred.
- Programmable watchdog pulse output on RESOUT_N pin.
- Can be used as a standard timer if watchdog is not used.
- Pause control to stop counting when core is in debug state.

7.7.3 Millisecond timer

The millisecond timer is clocked by 32 kHz RTC clock, so a prescaler is not needed to obtain a lower count rate.

The millisecond timer includes three match registers that are compared to the Timer/Counter value. A match can generate an interrupt and the cause the Timer/Counter either continue to run, stop, or be reset.

Features

- 32-bit Timer/Counter, running from the 32 kHz RTC clock.
- Counter or Timer operation.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

7.7.4 Clocking and Power Control Features

Clocking

Clocking in the LPC32x0 family is designed to be versatile, so that system and peripheral requirements may be met, while allowing optimization of power consumption. Clocks to most functions may be turned off if not needed and some peripherals do this automatically.

The LPC32x0 family supports three operational modes, two of which are specifically designed to reduce power consumption. The modes are: RUN mode, Direct RUN mode, and STOP mode.These three operational modes give control over processing speed and power consumption. In addition, clock rates to different functional blocks may be changed by switching clock sources, changing PLL values, or altering clock divider configurations. This allows a trade-off of power versus processing speed based on application requirements.

Crystal Oscillator

The main oscillator is the basis for the clocks most chip functions use by default. Optionally, many functions can be clocked instead by the output of a PLL (with a fixed 397x rate multiplication) which runs from the RTC oscillator. In this mode, the main oscillator may be turned off unless the USB interface is enabled. If a SYSCLK frequency other than 13 MHz is required in the application, or if the USB block is not used, the main oscillator may be used with a frequency of between 1 MHz and 20 MHz.

PLLs

The LPC32x0 family includes three PLLs: The 397x PLL allows boosting the RTC frequency to 13.008896 MHz for use as the primary system clock. The USB PLL provides the 48 MHz clock required by the USB block; and the HCLK PLL provides the basis for the CPU clock, the AHB bus clock, and the main peripheral clock.

The 397x PLL multiplies the 32768 Hz RTC clock by 397 to obtain a 13.008896 MHz clock. The 397x PLL is designed for low power operation and low jitter. This PLL requires an external RC loop filter for proper operation.

The HCLK PLL accepts an input clock from either the main oscillator or the output of the 397x PLL. The USB PLL only accepts an input clock from the main oscillator.The USB input clock runs through a divide-by-N pre-divider before entering the USB PLL.

The input to the HCLK and USB PLLs may initially be divided down by a pre-divider value 'N', which may have the values 1, 2, 3, or 4. This pre-divider can allow a greater number of possibilities for the output frequency. Following the PLL input divider is the PLL multiplier. This can multiply the pre-divider output by a value 'M', in the range of 1 through 256. The resulting frequency must be in the range of 156 MHz to 320 MHz. The multiplier works by dividing the output of a Current Controlled Oscillator (CCO) by the value of M, then using a phase detector to compare the divided CCO output to the pre-divider output. The error value is used to adjust the CCO frequency.

At the PLL output, there is a post-divider that can be used to bring the CCO frequency down to the desired PLL output frequency. The post-divider value 'P', can divide the CCO output by 1, 2, 4, 8, or 16. The post-divider can also be bypassed, allowing the PLL CCO output to be used directly. The maximum PLL output frequency supported by the CPU is 208 MHz. The only output frequency supported by the USB PLL is 48 MHz and the clock has strict requirements for nominal frequency (500 ppm) and jitter (500 ps).

Power Control Modes

The LPC32x0 family supports three operational modes, two of which are specifically designed to reduce power consumption. The modes are: Run mode, Direct Run mode, and Stop mode.

Run mode is the normal operating mode for applications that require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. In Run mode, the CPU can run at up to 208 MHz and the AHB bus can run at up to 104 MHz.

Direct Run mode allows reducing the CPU and AHB bus rates in order to save power. Direct Run mode can also be the normal operating mode for applications that do not require the CPU, AHB bus, or any peripheral function other than the USB block to run faster than the main oscillator frequency. Direct Run mode is the default mode following chip reset.

Stop mode causes all CPU and AHB operation to cease, and stops clocks to peripherals other than the USB block.

Reset

Reset is accomplished by an active low signal on the RESET_N input pin. A reset pulse with a minimum width of 10 main oscillator clocks after the oscillator is stable is required to guarantee a valid chip reset. At power-up, 10 milliseconds should be allowed for the oscillator to start up and stabilize after V_{DD} reaches operational voltage. An internal reset with a minimum duration of 10 clock pulses will also be applied if the watchdog timer generates an internal device reset.

The RESET_N pin is located in the RTC power domain. This means that the RTC power must be present for an external reset to have any effect. The RTC power domain nominally runs from 1.2 V, but the RESET_N pin can be driven as high as 1.95 V.

7.8 Communication Peripheral Interfaces

In addition to the Ethernet MAC and USB interfaces there many more available serial Communication peripheral interfaces on the LPC32x0 family. Here is a list of the available serial communication interfaces.

- 7 UARTs; 4 Standard UARTs and 3 High-speed UARTs
- 2 SPI Serial I/O Controllers
- 2 SSP Serial I/O Controllers
- 2 I2C Serial I/O Controllers
- 2 I2S Audio Controllers

A short functional description of each of these peripherals is provided in the following sections.

7.8.1 UARTs

The LPC32x0 family contains seven UARTs. Four are standard UARTs, and three are high-speed UARTs.

7.8.1.1 Standard UARTs

The four standard UARTs are compatible with the INS16Cx50. These UARTs support rates up to 460800 bit/s from a 13 MHz peripheral clock.

Features

- Each standard UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 16, 32 , 48 , and 60 Bytes.
- Transmitter FIFO trigger points at 0, 4 , 8, and 16 Bytes.
- Register locations conform to the “550” industry standard.
- Each standard UART has a fractional rate pre-divider and an internal baud rate generator.
- The standard UARTs support three clocking modes: on, off, and auto-clock. The auto-clock mode shuts off the clock to the UART when it is idle.
- UART 6 includes an IrDA mode to support infrared communication.
- The standard UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800) bit/s.
- Each UART includes an internal loopback mode.

7.8.1.2 High-speed UARTs

The three high-speed UARTs are designed to support rates up to 921600 bit/s from a 13 MHz peripheral clock, for on-board communication in low noise conditions. This is accomplished by changing the over sampling from 16× to 14×, and altering the rate generation logic.

Features

- Each high-speed UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 1, 4, 8, 16, 32, and 48 Byte.
- Transmitter FIFO trigger points at 0, 4, and 8 Byte.
- Each high-speed UART has an internal baud rate generator.
- The high-speed UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600) bit/s.
- The three high speed UARTs only support (8N1) 8-bit data word length, 1-stop bit, no parity, and no flow control as a the communications protocol.
- Each UART includes an internal loopback mode.

7.8.2 SPI serial I/O controller

The LPC32x0 family has two Serial Peripheral Interfaces (SPI). The SPI is a 3-wire serial interface that is able to interface with a large range of serial peripheral or memory devices (SPI mode 0 to 3 compatible slave devices).

Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master. The SPI implementation on the LPC32x0 family does not support operation as a slave.

Features

- Supports slaves compatible with SPI modes 0 to 3.
- Half duplex synchronous transfers.
- DMA support for data transmit and receive.
- 1-bit to 16-bit word length.
- Choice of LSB or MSB first data transmission.
- 64 × 16-bit input or output FIFO.
- Bit rates up to 52 Mbit/s.
- Busy input function.
- DMA time out interrupt to allow detection of end of reception when using DMA.
- Timed interrupt to facilitate emptying the FIFO at the end of a transmission.
- SPI clock and data pins may be used as general purpose pins if the SPI is not used.
- Slave selects can be supported using GPO or GPIO pins

7.8.3 SSP serial I/O Controller

The LPC32x0 family contains two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Maximum SPI bus data bit rate of one half (Master mode) and one twelfth (Slave mode) of the input clock rate
- DMA transfers supported by GPDMA

7.8.4 I²C-bus serial I/O controller

There are two I2C interfaces in the LPC32x0 family of controllers. These I2C blocks can be configured as a master, multi master or slave supporting up to 400 kHz. The I2C blocks also support 7 or 10 bit addressing. Each has a four word FIFO for both transmit and receive. An interrupt signal is available from each block.

There is a separate slave transmit FIFO. The slave transmit FIFO (TXS) and its level are only available when the controller is configured as a Master/Slave device and is operating in a multi-master environment. Separate TX FIFOs are needed in a multi-master because a controller might have a message queued for transmission when an external master addresses it to be come a slave-transmitter, a second source of data is needed.

Note that the I2C clock must be enabled in the I2CCLK_CTRL register before using the I2C. The I2C clock can be disabled between communications, if used as a single master I2C interface, software has full control of when I2C communication is taking place on the bus.

Features

- The two I^{2}C-bus blocks are standard I^{2}C-bus compliant interfaces that may be used in Single Master, Multi master or Slave modes.
- Programmable clock to allow adjustment of I^{2}C-bus transfer rates.
- Bidirectional data transfer.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

7.8.5 I^{2}S Audio Controller

The I^{2}S-bus provides a standard communication interface for digital audio applications The I^{2}S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. Each I^{2}S connection can act as a master or a slave. The master connection determines the frequency of the clock line and all other slaves are driven by this clock source. The two I^{2}S interfaces on the LPC32x0 family provides a separate transmit and receive channel, providing a total of two transmit channels and two receive channels. Each I^{2}S channel supports monaural or stereo formatted data.

Features

- The interface has separate input/output channels each of which can operate in master or slave mode
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes
- Mono and stereo audio data supported
- Supports standard pcm sampling frequencies (8, 11.025, 16, 22.05, 32, 44.1,48, 96) kHz
- Configurable word select period in master mode (separately for I^{2}S input and output)
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive
- Generates interrupt requests when buffer levels cross a programmable boundary
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block
- Controls include reset, stop and mute options separately for I^{2}S input and I^{2}S output

7.9 Other Peripherals

In addition to the Communication peripherals there are many general purpose peripherals available in the LPC32x0 family. Here is a list of the general purpose peripherals.

- General Purpose I/O
- Keyboard Scanner
- Touch screen controller and 10-Bit Analog-to-Digital-Converter
- Real-Time Clock
- A High-speed Timer
- 4 General Purpose 32-Bit Timer/External Event Counters
- 2 Simple Pulse-Width Modulators
- 2 Versatile Pulse-Width Modulators

A short functional description of each of these peripherals is provided in the following sections.

7.9.1 General purpose parallel I/O

Some device pins that are not dedicated to a specific peripheral function have been designed to be general purpose inputs, outputs, or I/Os. Also, some pins may be configured either as a specific peripheral function or a general purpose input, output, or I/O. A total of 55 pins can potentially be used as general purpose input/outputs, general purpose outputs, and general purpose inputs.

GPIO pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of GPIO and GPO outputs controlled by that register simultaneously. The value of the output register for standard GPIOs and GPO pins may be read back, as well as the current actual state of the port pins.

There are 12 GPI, 24 GPO, and six GPIO pins. When the SDRAM bus is configured for 16 data bits, 13 of the remaining SDRAM data pins may be used as GPIOs.

Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- A single register selects direction for pins that support both input and output modes.
- Direction control of individual bits.
- For input/output pins, both the programmed output state and the actual pin state can be read.
- There are a total of 12 general purpose inputs, 24 general purpose outputs, and six general purpose input/outputs.
- Additionally, 13 SDRAM data lines may be used as GPIOs if a 16-bit SDRAM interface is used (rather than a 32-bit interface).

7.9.2 Keyboard Scanner

The keyboard scanner function can automatically scan a keyboard of up to 64 keys in an 8×8 matrix. In operation, the keyboard scanner's internal state machine will normally be in an idle state, with all KEY_ROW[n] pins set high, waiting for a change in the column inputs to indicate that one or more keys have been pressed.

When a keypress is detected, the matrix is scanned by setting one output pin high at a time and reading the column inputs. After de-bouncing, the keypad state is stored and an interrupt is generated. The keypad is then continuously scanned waiting for 'extra key pressed' or 'key released'. Any new keypad state is scanned and stored into the matrix registers followed by a new interrupt request to the interrupt controller. It is possible to detect and separate up to 64 multiple keys pressed.

Features

- Supports up to 64 keys in 8×8 matrix.
- Programmable debounce period.
- A key press can wake up the CPU from Stop mode.

7.9.3 Touchscreen controller and 10-bit ADC

The LPC32x0 family microcontrollers includes touch screen controller (TSC) hardware, which automatically measures and determines the X and Y co-ordinates where a touch screen is pressed, in addition the TSC can measure an additional analog input signal on the AUX_IN pin.

Optionally, the TSC can operate as an Analog-to-Digital Converter (ADC). The ADC supports three channels and uses 10-bit successive approximation to produce results with a resolution of 10 bits in 11 clock cycles.

The analog portion of the ADC has its own power supply to enhance the low noise characteristics of the converter. This voltage is only supplied internally when the core has voltage. However, the ADC block is not affected by any difference in ramp-up time for VDD_AD and VDD_CORE voltage supplies.

Features

- Measurement range of 0 V to VDD_AD28 (nominally 3 V).
- Low noise ADC.
- 10-bit resolution
- Three input channels.
- Uses 32 kHz RTC clock or Peripheral clock

7.9.4 RTC

The RTC runs at 32768 Hz using a very low power oscillator. The RTC counts seconds and can generate alarm interrupts that can wake up the device from Stop mode. The RTCCLK can also clock the 397x PLL, the Millisecond Timer, the ADC, the Keyboard Scanner and the PWMs. The RTC up-counter value represents a number of seconds elapsed since second 0, which is an application determined time. The RTC counter will reach maximum value after about 136 years. The RTC down-counter is initiated with all 1's.

Two 32-bit Match registers are readable and writable by the processor. A match will result in an interrupt provided that the interrupt is enabled. The ONSW output pin can also be triggered by a match event, and cause an external power supply to turn on all of the operating voltages, as a way to startup after power has been removed.

The RTC block is implemented in a separate voltage domain. The block is supplied via a separate supply pin from a battery or other power source.

The RTC block also contains 32 words (128 Bytes) of very low voltage SRAM. This SRAM is able to hold its contents down to the minimum RTC operating voltage.

Features

- Measures the passage of time in seconds.
- 32-bit up and down seconds counters.
- Ultra low power design to support battery powered systems.
- Dedicated 32 kHz oscillator.
- An output pin is included to assist in waking up when the chip has had power removed to all functions except the RTC.
- Two 32-bit match registers with interrupt option.
- 32 words (128 Bytes) of very low voltage SRAM.
- The RTC and battery RAM power have an independent power domain and dedicated supply pins, which can be powered from a battery or power supply.

7.9.5 Enhanced 32-bit timers/external event counters

The LPC32x0 family includes four 32-bit Timer/Counters. The Timer/Counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The Timer/Counter also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

Features

- A 32-bit Timer/Counter with a programmable 32-bit prescaler
- Counter or Timer operation
- Up to four 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt
- Four 32-bit match registers that allow
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
- Up to four external outputs corresponding to match registers, with the following capabilities
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match

– Do nothing on match

7.9.6 High-speed timer

The high-speed timer block is clocked by the main peripheral clock. The clock is first divided down in a 16-bit programmable prescale counter which clocks a 32-bit Timer/Counter.

The high-speed timer includes three match registers that are compared to the Timer/Counter value. A match can generate an interrupt and cause the Timer/Counter to either continue to run, stop, or be reset. The high-speed timer also includes two capture registers that can take a snapshot of the Timer/Counter value when an input signal transitions. A capture event may also generate an interrupt.

Features

- 32-bit Timer/Counter with programmable 16-bit prescaler.
- Counter or Timer operation.
- Two 32-bit capture registers.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

7.9.7 Pulse width modulators

The LPC32x0 family provides two simple PWMs. They are clocked separately by either the main peripheral clock or the 32 kHz RTC clock. Both PWMs have a duty cycle programmable in 255 steps.

Features

- Clocked by the main peripheral clock or the 32 kHz RTC clock.
- Programmable 4-bit prescaler.
- Duty cycle programmable in 255 steps.
- Output frequency up to 50 kHz when using a 13 MHz peripheral clock.

7.9.8 Versatile PWM

The Versatile PWM is based on the Enhanced 32-bit timers/external event counters and inherits all of its features, although only the PWM function is pinned out on the LPC32x0 family. The Timer counts cycles of the system derived clock and optionally switches pins, generates an interrupt or performs other actions when specified timer values occur, based on seven match registers.The PWM function is in addition to these features and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. A dedicated match register controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, a dedicated match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

Features

- LPC32x0 family has two PWMs with the same operational features. These may be operated in a synchronized fashion by setting them both up to run at the same rate, then enabling both simultaneously. PWM0 acts as the master and PWM1 as the slave for this use
- Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source)
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses
- Pulse period and width can be any number of timer counts. This allows complete
- flexibility in the trade-off between resolution and repetition rate. All PWM outputs will

  occur at the same repetition rate
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective
- May be used as a standard timer if the PWM mode is not enabled
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler

8. Basic architecture

The LPC32x0 family is a general purpose ARM926EJ-S 32-bit microprocessor with a 32KB Instruction Cache and a 32KB Data Cache. The microcontoller offers high performance and very low power consumption. The ARM architecture is based on RISC principles, which results in the instruction set and related decode mechanism being much simpler than equivalent microprogrammed CISCs. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

The ARM926EJ-S core employs a 5-stage pipeline so processing and memory system accesses can occur continuously. At any one point in time, several operations are in progress: subsequent instruction fetch, next instruction decode, instruction execution, memory access, and write-back. The combination of architectural enhancements gives the ARM9 about 30 % better performance than an ARM7 running at the same clock rate:

- Approximately 1.3 clocks per instruction for the ARM926 compared to 1.9 clocks per instruction for ARM7TDMI.
- Approximately 1.1 Dhrystone MIPS/MHz for the ARM926 compared to 0.9 Dhrystone MIPS/MHz for ARM7TDMI.

The ARM926EJ-S processor also employs an operational state known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb state is the use of a super-reduced instruction set. Essentially, the ARM926EJ-S processor core has two instruction sets:

1. The standard 32-bit ARM set.
2. A 16-bit Thumb set.

The Thumb set’s smaller 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining many of ARM’s 32-bit performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates using the same 32-bit register set as ARM code. Thumb code size is up to 65% smaller than ARM code size, and 160% of the performance of an equivalent ARM processor connected to a 16-bit memory system. Additionally, the ARM926EJ-S core includes enhanced DSP instructions and multiplier, as well as an enhanced 32-bit MAC block.

9. Limiting values

Table 5. Limiting values for LPC32x0 family

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)		[2]	–0.5	+1.3	V
$V_{DD(EMC)}$	EMC supply voltage (2.8 V)		[3]	–0.5	+3.1	V
$V_{DDA(3V0)}$	analog supply voltage (3.0 V)		[4]	–0.5	+3.3	V
$V_{DD(IO)}$	supply voltage		[5]	–0.5	+3.6	V
V_{IA}	analog input voltage			–0.5	+3.3	V
V_I	input voltage	1.8 V pins	[6]	–0.5	+1.95	V
		3.0 V pins	[6]	–0.5	+3.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
T_{stg}	storage temperature			–40	+125	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption			<tbd>	W
V_{esd}	electrostatic discharge voltage	human body model	[7]			
		all pins		–2000	+2000	V

[1] The following applies to Table 5:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Core, PLL, oscillator, and RTC supplies; applies to pins VDD_CORE, VDD_COREFXD, VDD_OSC, VDD_PLL397, VDD_PLLHCLK, VDD_PLLUSB, VDD_RTC, VDD_RTCCORE, and VDD_RTCOSC.

[3] I/O pad supply; applies to pins VDD_EMC.

[4] Applies to VDD_AD pins.

[5] Applies to pins in the following domains VDD_IOA, VDD_IOB, VDD_IOC and VDD_IOD.

[6] Including voltage on outputs in 3-state mode.

[7] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Static characteristics

Table 6. Static characteristics for the LPC32x0 family

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)	core supply voltage for full performance; full frequency range	[2]	1.1	1.2	1.3	V
		core supply voltage for reduced power; up to 14 MHz CPU	[2]	0.9	-	1.3	V
		RTC supply voltage	[3]	0.9	-	1.3	V
		PLL and oscillator supply voltage	[4]	1.1	1.2	1.3	V
$V_{DD(EMC)}$	EMC supply voltage	in 2.8 V range	[5]	2.5	2.8	3.1	V
		in 1.8 V range		1.7	1.8	1.95	V
$V_{DD(IO)}$	IO supply voltage	in 1.8 V range	[6]	1.7	1.8	1.95	V
		in 3.0 V range		2.7	3	3.3	V
$V_{DDA(3V0)}$	analog supply voltage (3.0 V)	applies to VDD_AD pins		2.7	3	3.3	V
Run, Direct Run and Stop Modes							
$I_{DD(run)}$	Run mode supply current	VDD_CORE = 1.2 V; T_{amb} = 25 °C; I-cache enabled; CPU clock = 208 MHz; all peripherals enabled		-	80	-	mA
$I_{DD(drun)}$	direct Run mode supply current	VDD_CORE = 0.9 V; T_{amb} = 25 °C; CPU clock = 13 MHz		-	7	-	mA
$I_{DD(stop)}$	Stop mode supply current	VDD_CORE = 0.9 V; T_{amb} = 25 °C; CPU clock = stopped internally		-	-	500	µA
Input pins and I/O pins configured as input							
V_I	input voltage		[7] [9]	0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage	1.8 V inputs		0.7 x $V_{DD(IO)}$	-	-	V
		3.0 V inputs		0.7 x $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage	1.8 V inputs		-	-	0.3 x $V_{DD(IO)}$	V
		3.0 V inputs		-	-	0.3 x $V_{DD(IO)}$	V
V_{HYS}	Hysteresis voltage	1.8 V inputs		0.1 x $V_{DD(IO)}$			V
		3.0 V inputs		0.1 x $V_{DD(IO)}$			V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	1	µA
I_{IH}	HIGH-level input current	V_I = $V_{DD(IO)}$; no pull-down	[7]	-	-	1	µA
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V_I < (1.5V_{DD})$	[7]	-	-	100	mA
I_{PU}	pull-up current	1.8 V inputs with pull-up; V_{IN} = 0		6	12	22	µA
		3.0 V inputs with pull-up; V_{IN} = 0		25	50	80	µA

Table 6. Static characteristics for the LPC32x0 family *...continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{PD}	pull-down current	1.8 V inputs with pull-down; $V_{IN} = V_{DD}$		5	12	22	µA
		3.0 V inputs with pull-down; $V_{IN} = V_{DD}$		25	50	85	µA
C_{IN}	input capacitance	Excluding bonding pad capacitance		-	-	3.3	pF
Output pins and I/O pins configured as output							
V_O	output voltage		[7][8] [9][10]	0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	1.8 V outputs; I_{OH} = –1 mA	[11]	$V_{DD(IO)} - 0.4$	-	-	V
		3.0 V outputs; I_{OH} = –4 mA	[11]	$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	1.8 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
		3.0 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{DD} = 1.8 V; $V_{OH} = V_{DD}$ - 0.4V	[7][11]	-3.3	-	-	mA
		V_{DD} = 2.8 V; $V_{OH} = V_{DD}$ - 0.4V		-6.5	-	-	mA
I_{OL}	LOW-level output current	V_{DD} = 1.8 V; V_{OL} = 0.4V	[7][11]	1.5	-	-	mA
		V_{DD} = 2.8 V; V_{OL} = 0.4V		3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down	[7]	-	-	1	µA
I_{OHS}	HIGH-state short-circuit output current	V_{DD} = 1.8 V; V_{OH} = 0 V	[12]	-	-	66	mA
		V_{DD} = 2.8 V; V_{OH} =0 V		-	-	183	mA
I_{OLS}	LOW-state short-circuit output current	V_{DD} = 1.8 V; $V_{OL} = V_{DD}$	[7][12]	-	-	34	mA
		V_{DD} = 2.8 V; $V_{OL} = V_{DD}$		-	-	105	mA
Z_{OUT}	output impedance	V_{DD} = 1.8 V		40	-	60	ohm
		V_{DD} = 3.0 V		40	-	60	ohm
EMC pins							
V_I	input voltage		[7] [9]	0	-	$V_{DD(EMC)}$	V
V_{IH}	HIGH-level input voltage	1.8 V inputs		0.7 x $V_{DD(EMC)}$	-	-	V
		3.0 V inputs		0.7 x $V_{DD(EMC)}$	-	-	V
V_{IL}	LOW-level input voltage	1.8 V inputs		-	-	0.3 x $V_{DD(EMC)}$	V
		2.8 V inputs		-	-	0.3 x $V_{DD(EMC)}$	V
V_{HYS}	Hysteresis voltage	1.8 V inputs		0.4	-	0.6	V
		2.8 V inputs		0.55	-	0.85	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	0.3	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(EMC)}$; no pull-down	[7]	-	-	0.3	µA
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V_I < (1.5V_{DD})$	[7]	-	-	100	mA
I_{PU}	pull-up current	1.8 V inputs with pull-up; V_{IN} = 0		34	62	107	µA
		2.8 V inputs with pull-up; V_{IN} = 0		97	169	271	µA

Table 6. Static characteristics for the LPC32x0 family *…continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{PD}	pull-down current	1.8 V inputs with pull-down; $V_{IN} = V_{DD(EMC)}$		23	51	93	µA
		3.0 V inputs with pull-down; $V_{IN} = V_{DD(EMC)}$		73	155	266	µA
C_{IN}	input capacitance	Excluding bonding pad capacitance		-	-	2.1	pF
V_O	output voltage		[7][8] [9][10]	0	-	$V_{DD(EMC)}$	V
V_{OH}	HIGH-level output voltage	1.8 V outputs; I_{OH} = –1 mA	[11]	$V_{DD(EMC)} - 0.3$	-	-	V
		3.0 V outputs; I_{OH} = –4 mA	[11]	$V_{DD(EMC)} - 0.3$	-	-	V
V_{OL}	LOW-level output voltage	1.8 V outputs; I_{OL} = 4 mA	[11]	-	-	0.3	V
		3.0 V outputs; I_{OL} = 4 mA	[11]	-	-	0.3	V
I_{OH}	HIGH-state output current	V_{DD} = 1.8 V; $V_{OH} = V_{DD}$ - 0.4V	[7][11]	-6	-	-	mA
		V_{DD} = 2.8 V; $V_{OH} = V_{DD}$ - 0.4V		-6	-	-	mA
I_{OL}	LOW-state output current	V_{DD} = 1.8 V; V_{OL} = 0.4V	[7][11]	6	-	-	mA
		V_{DD} = 2.8 V; V_{OL} = 0.4V		6	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down	[7]	-	-	0.3	µA
I_{OHS}	HIGH-level short-circuit output current	V_{DD} = 1.8 V; V_{OH} = 0 V	[12]	-	-	-49	mA
		V_{DD} = 2.8 V; V_{OH} =0 V		-	-	-81	mA
I_{OLS}	LOW-level short-circuit output current	V_{DD} = 1.8 V; $V_{OL} = V_{DD}$	[7][11]	-	-	49	mA
		V_{DD} = 2.8 V; $V_{OL} = V_{DD}$		-	-	86	mA
Z_{OUT}	output impedance	V_{DD} = 1.8 V		35	40	58	ohm
		V_{DD} = 3.0 V		32	35	45	ohm
I²C pins							
V_I	input voltage		[7] [9]	0	-	5.5V	V
V_{IH}	HIGH-level input voltage	1.8 V inputs		0.7 x $V_{DD(IO)}$	-	-	V
		3.0 V inputs		0.7 x $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-state input voltage	1.8 V inputs		-	-	0.3 x $V_{DD(IO)}$	V
		2.8 V inputs		-	-	0.3 x $V_{DD(IO)}$	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	10	µA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; no pull-down	[7]	-	-	10	µA
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V_I < (1.5V_{DD})$	[7]	-	-	100	mA
C_{IN}	input capacitance	Excluding bonding pad capacitance		-	-	1.6	pF
V_{OL}	LOW-state output voltage	1.8 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
		3.0 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
I_{OL}	LOW-state output current	V_{DD} = 1.8 V; V_{OL} = 0.4V	[7][11]	3	-	-	mA
		V_{DD} = 2.8 V; V_{OL} = 0.4V		3	-	-	mA

Table 6. Static characteristics for the LPC32x0 family *...continued*

T_{amb} = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; no pull-up/down	[7]	-	-	10	µA
I_{OLS}	LOW-state short-circuit output current	V_{DD} = 1.8 V; V_{OL} = V_{DD}	[7][12]	-	-	40	mA
		V_{DD} = 2.8 V; V_{OL} = V_{DD}		-	-	40	mA
ONSW pin							
V_O	output voltage		[7][8] [9] [10]	0	-	$V_{DD(1V2)}$	V
V_{OH}	HIGH-level output voltage	1.2 V outputs; I_{OH} = –1 mA	[11]	$V_{DD(1V2)}$ – 0.4	-	-	V
V_{OL}	LOW-state output voltage	1.2 V outputs; I_{OL} = 4 mA	[11]	-	-	0.4	V
I_{OH}	HIGH-state output current	V_{OH} = V_{DD} – 0.4 V	[7][11]	-4	-	-	mA
I_{OL}	LOW-state output current	V_{OL} = 0.4 V	[7][11]	3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; no pull-up/down	[7]	-	-	1.5	µA
I_{OHS}	HIGH-level short-circuit output current	V_{DD} = 1.8 V; V_{OH} = 0 V	[12]	-	-	-135	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[7][12]	-	-	135	mA
Z_{OUT}	output impedance	V_{DD} = 1.2 V		40	-	60	ohm
Reset Pin							
V_I	input voltage		[7] [9]	0	-	1.95	V
V_{IH}	HIGH-state input voltage	1.2 V inputs		0.7 x $V_{DD(1V2)}$	-	-	V
V_{IL}	LOW-state input voltage	1.2 V inputs		-	-	0.7 x $V_{DD(1V2)}$	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	1	µA
I_{IH}	HIGH-level input current	V_I = V_{DD}; no pull-down	[7]	-	-	1	µA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; no pull-up/down	[7]	-	-	1	µA
I_{latch}	I/O latch-up current	$–(1.5V_{DD}) < V_I < (1.5V_{DD})$	[7]	-	-	100	mA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Applies to VDD_CORE pins.

[3] Applies to pins VDD_RTC, VDD_RTCCORE, and VDD_RTCOSC.

[4] Applies to pins VDD_COREFXD, VDD_OSC, VDD_PLL397, VDD_PLLHCLK, and VDD_PLLUSB.

[5] Applies to VDD_EMC pins.

[6] Applies to VDD_IOA, VDD_IOB, VDD_IOC and VDD_IOD pins.

[7] Referenced to the applicable V_{DD} for the pin.

[8] Including voltage on outputs in 3-state mode.

[9] 9The applicable V_{DD} voltage for the pin must be present.

[10] 3-state outputs go into 3-state mode when $V_{DD(3V0)}$ is grounded.

[11] Accounts for 100 mV voltage drop in all supply lines.

[12] Only allowed for a short time period.

11. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.[1]

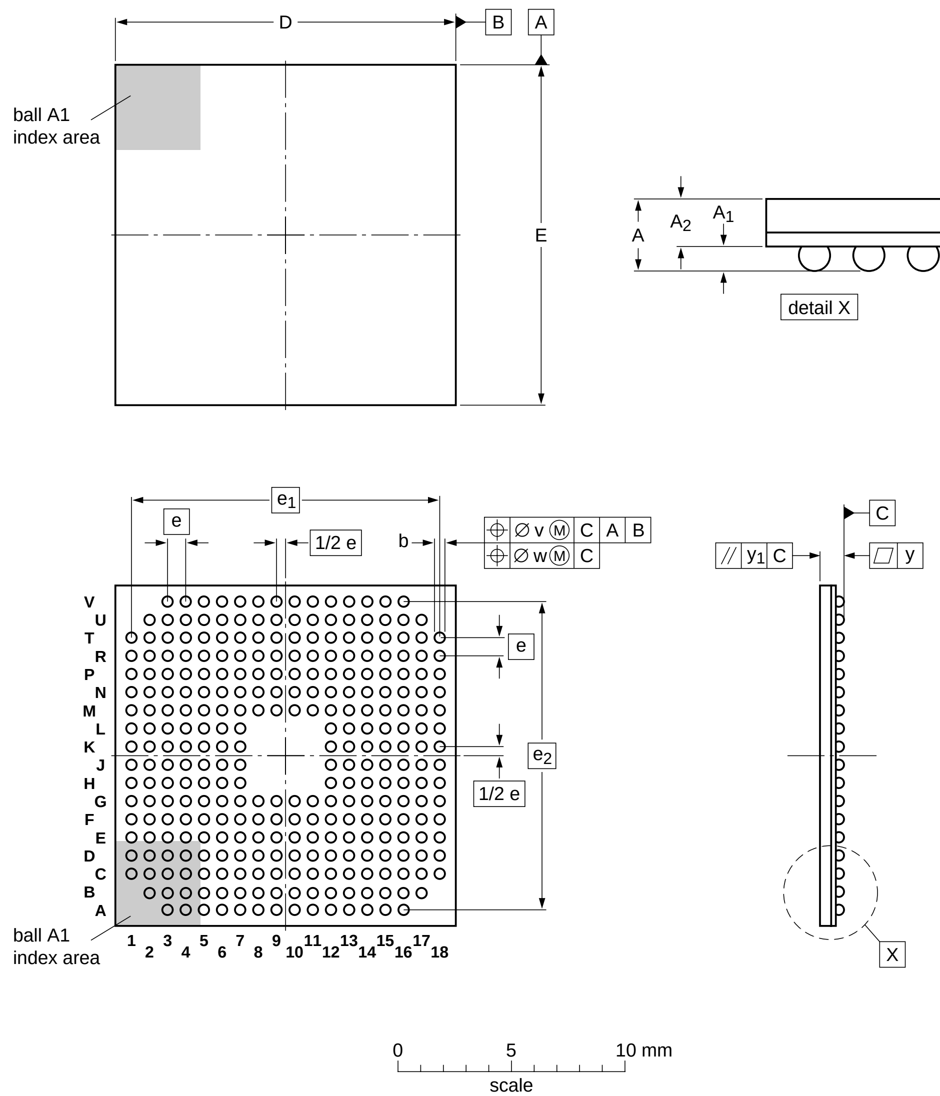
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{ext}	external clock frequency	[2]	1	13	20	MHz
Port pins						
t_r	rise time		-	5	-	ns
t_f	fall time		-	5	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Supplied by an external crystal.

12. Package outline

TFBGA296: plastic thin fine-pitch ball grid array package; 296 balls **SOT1048-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.80 0.65	0.5 0.4	15.1 14.9	15.1 14.9	0.8	13.6	13.6	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1048-1		MO-216				~~07-10-19~~ 07-11-02

Fig 4. Package outline SOT1048-1 (TFBGA296)

13. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC32x0_00	<tbd>	Preliminary data sheet		

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contents

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