ISOLATED CAN TRANSCEIVER

FEATURES

- 4000-V_{PEAK} Isolation
- Failsafe Outputs
- Low Loop Delay: 150 ns Typical
- 50 kV/μs Typical Transient Immunity
- Meets or Exceeds ISO 11898 requirements
- Bus-Fault Protection of –27 V to 40 V
- Dominant Time-Out Function
- UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2), IEC 61010-1, IEC 60950-1 and CSA Approval Pending
- 3.3-V Inputs are 5-V Tolerant

APPLICATIONS

- CAN Data Buses
- Industrial Automation
  - DeviceNet Data Buses
  - CANopen Data Buses
  - CANKingdom Data Buses
- Medical Scanning and Imaging
- Security Systems
- Telecom Base Station Status and Control
- HVAC
- Building Automation

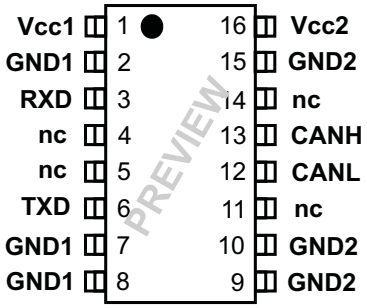
DESCRIPTION

The ISO1050 is a galvanically isolated CAN transceiver that meets or exceeds the specifications of the ISO 11898 standard. The device has the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides galvanic isolation of up to 4000 V_{PEAK}. Used in conjunction with isolated power supplies, the device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

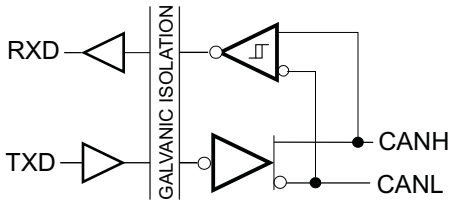
As a CAN transceiver, the device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). Designed for operation in especially harsh environments, the device features cross-wire, overvoltage and loss of ground protection from –27 V to 40 V and overtemperature shut-down, as well as a –12 V to 12 V common-mode range.

The ISO1050 is characterized for operation over the ambient temperature range of –55°C to 105°C.

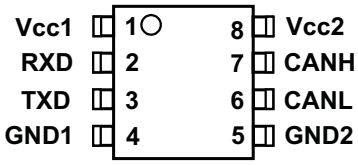
DW PACKAGE



FUNCTION DIAGRAM



DUB PACKAGE



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1) (2)

				VALUE / UNIT
V_{CC1}, V_{CC2}	Supply voltage (3)			–0.5 V to 6 V
V_I	Voltage input (TXD)			–0.5 V to 6 V
V_{CANH} or V_{CANH}	Voltage range at any bus terminal (CANH, CANL)			–27 V to 40 V
I_O	Receiver output current			±15 mA
ESD	Human Body Model	JEDEC Standard 22, Method A114-C.01	Bus pins and GND2(4)	±4 kV
			All pins	±4 kV
	Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1.5 kV
	Machine Model	ANSI/ESDS5.2-1996	All pins	±200 V
T_J	Junction temperature			–55°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This isolator is suitable for basic isolation within the safety limiting data. Maintenance of the safety data must be ensured by means of protective circuitry.
(3) All input and output logic voltage values are measured with respect to the GND1 logic side ground. Differential bus-side voltages are measured to the respective bus-side GND2 ground terminal.
(4) Tested while connected between Vcc2 and GND2.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage, controller side		3		5.5	V
V_{CC2}	Supply voltage, bus side		4.75	5	5.25	V
V_I or V_{IC}	Voltage at bus pins (separately or common mode)		–12(1)		12	V
V_{IH}	High-level input voltage	TXD	2		5.25	V
V_{IL}	Low-level input voltage	TXD	0		0.8	V
V_{ID}	Differential input voltage		–7		7	V
I_{OH}	High-level output current	Driver	–70			mA
		Receiver	–4			
I_{OL}	Low-level output current	Driver			70	mA
		Receiver			4	
T_J	Junction temperature (see THERMAL CHARACTERISTICS)		-55		125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC1}	V_{CC1} Supply current		V_I = 0 V or V_{CC1} , V_{CC1} = 3.3V		1	2	mA
			V_I = 0 V or V_{CC1} , V_{CC1} = 5V		2	3	
I_{CC2}	V_{CC2} Supply current	Dominant	V_I = 0 V, 60-Ω Load		52	73	mA
		Recessive	V_I = V_{CC1}		8	12	

(1) All typical values are at 25°C with V_{CC1} = V_{CC2} = 5V.

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input to receiver output, Recessive to Dominant	See Figure 9	112	150	210	ns
t_{loop2}	Total loop delay, driver input to receiver output, Dominant to Recessive	See Figure 9	112	150	210	ns

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(D)}$	Bus output voltage (Dominant)	CANH	See Figure 1 and Figure 2, V_I = 0 V, R_L = 60Ω	2.9	3.5	4.5	V
		CANL		0.8	1.2	1.5	
$V_{O(R)}$	Bus output voltage (Recessive)		See Figure 1 and Figure 2, V_I = 2 V, R_L= 60Ω	2	2.3	3	V
$V_{OD(D)}$	Differential output voltage (Dominant)		See Figure 1, Figure 2 and Figure 3, V_I = 0 V, R_L = 60Ω	1.5		3	V
			See Figure 1, Figure 2, and Figure 3 V_I = 0 V, R_L = 45Ω, Vcc > 4.8V	1.4		3	
$V_{OD(R)}$	Differential output voltage (Recessive)		See Figure 1 and Figure 2, V_I = 3 V, R_L = 60Ω	–0.12		0.012	V
			V_I = 3 V, No Load	–0.5		0.05	
$V_{OC(D)}$	Common-mode output voltage (Dominant)		See Figure 8	2	2.3	3	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage				0.3		
I_{IH}	High-level input current, TXD input		V_I at 2 V			5	µA
I_{IL}	Low-level input current, TXD input		V_I at 0.8 V	–5			µA
$I_{O(off)}$	Power-off TXD leakage current		V_{CC1}, V_{CC2} at 0 V, TXD at 5 V			10	µA
$I_{OS(ss)}$	Short-circuit steady-state output current		See Figure 11, V_{CANH} = –12 V, CANL Open	–105	–72		mA
			See Figure 11, V_{CANH} = 12 V, CANL Open		0.36	1	
			See Figure 11, V_{CANL} =–12 V, CANH Open	–1	–0.5		
			See Figure 11, V_{CANL} = 12 V, CANH Open		71	105	
C_O	Output capacitance		See receiver input capacitance				
CMTI	Common-mode transient immunity		See Figure 13, V_I = V_{CC} or 0 V	25	50		kV/µs

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, recessive-to-dominant output	See Figure 4	31	74	110	ns
t_{PHL}	Propagation delay time, dominant-to-recessive output		25	44	75	
t_r	Differential output signal rise time			20	50	
t_f	Differential output signal fall time			20	50	
t_{dom}	Dominant time-out	↓ C_L=100 pF, See Figure 10	300	450	700	µs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going bus input threshold voltage	See Table 1		750	900	mV
V_{IT-}	Negative-going bus input threshold voltage		500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			150		mV
V_{OH}	High-level output voltage with Vcc = 5V	I_{OH} = –4 mA, See Figure 6	V_{CC} – 0.8	4.6		V
		I_{OH} = –20 µA, See Figure 6	V_{CC} – 0.1	5		
V_{OH}	High-level output voltage with Vcc1 = 3.3V	I_{OL} = 4 mA, See Figure 6	V_{CC} – 0.8	3.1		V
		I_{OL} = 20 µA, See Figure 6	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6		0.2	0.4	V
		I_{OL} = 20 µA, See Figure 6		0	0.1	
C_I	Input capacitance to ground, (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5V		6		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		3		pF
R_{ID}	Differential input resistance	TXD at 3 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching $(1 - [R_{IN\ (CANH)} / R_{IN\ (CANL)}]) \times 100\%$	$V_{CANH} = V_{CANL}$	–3%	0%	3%	
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 13	25	50		kV/µs

(1) All typical values are at 25°C with $V_{CC1} = V_{CC2}$ = 5V.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	TXD at 3 V, See Figure 6	66	90	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		51	80	105	
t_r	Output signal rise time			3	6	
t_f	Output signal fall time			3	6	
t_{fs}	Failsafe output delay time from bus-side power loss	VCC1 at 5 V, See Figure 12		6		µs

PARAMETER MEASUREMENT INFORMATION

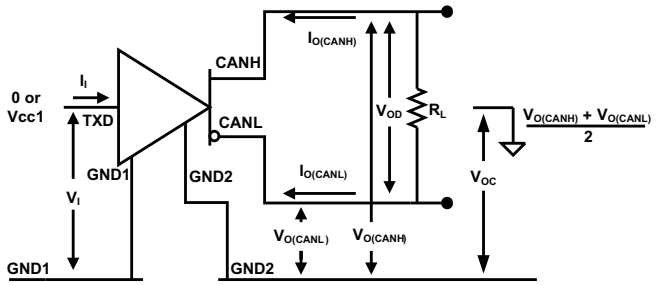


Figure 1. Driver Voltage, Current and Test Definitions

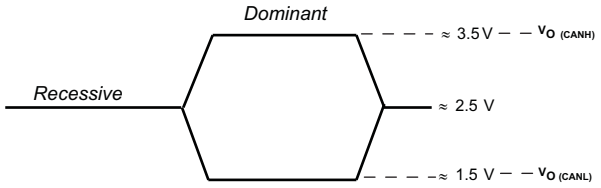


Figure 2. Bus Logic State Voltage Definitions

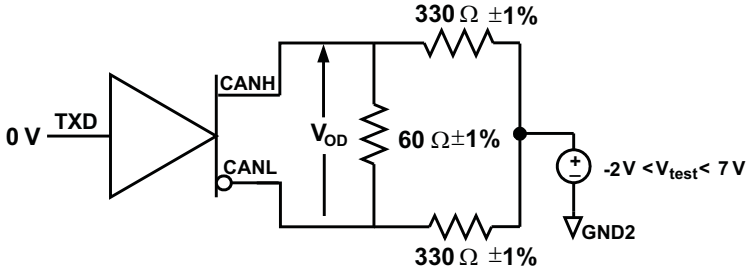
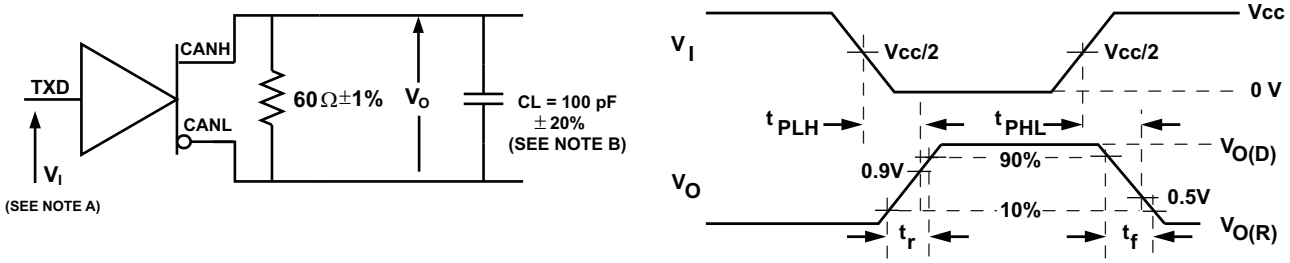


Figure 3. Driver V_{OD} with Common-mode Loading Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 4. Driver Test Circuit and Voltage Waveforms

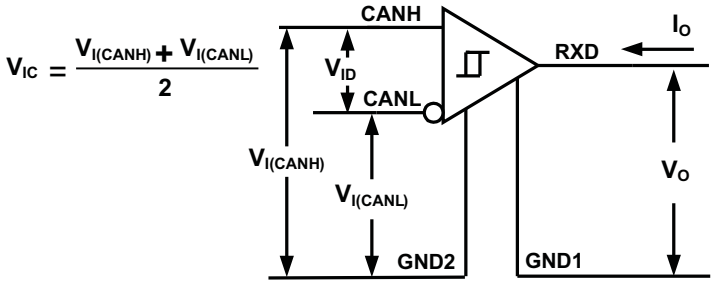
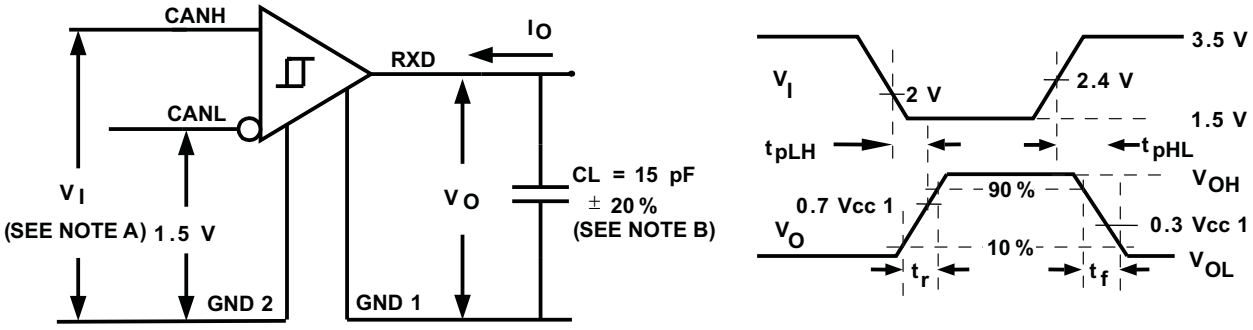


Figure 5. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



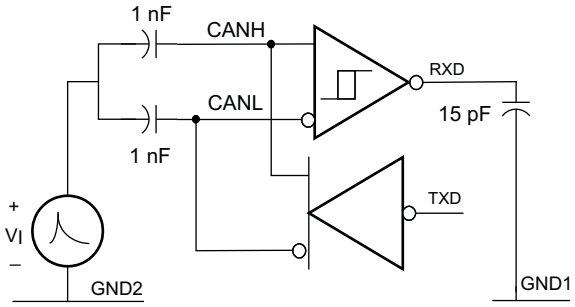
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	–6 V	H	
6 V	12 V	–6 V	H	
Open	Open	X	H	



The waveforms of the applied transients are in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b.

Figure 7. Transient Over-Voltage Test Circuit

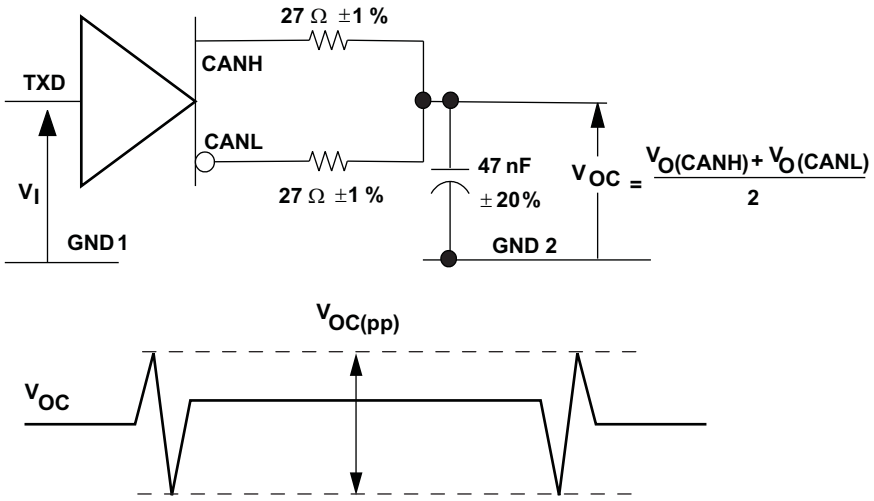


Figure 8. Peak-to-Peak Output Voltage Test Circuit and Waveform

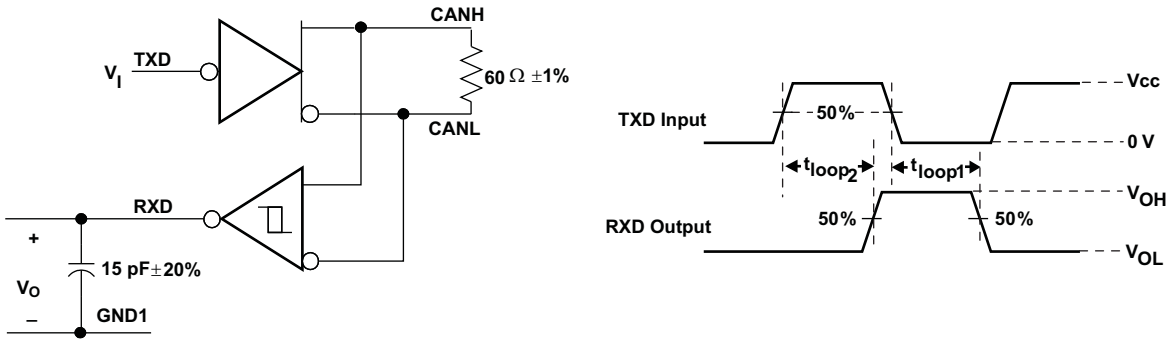
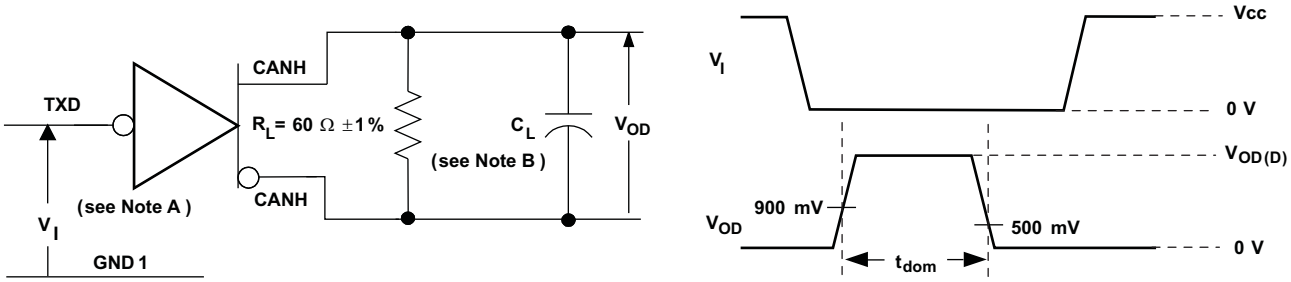


Figure 9. t_{LOOP} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 10. Dominant Timeout Test Circuit and Voltage Waveforms

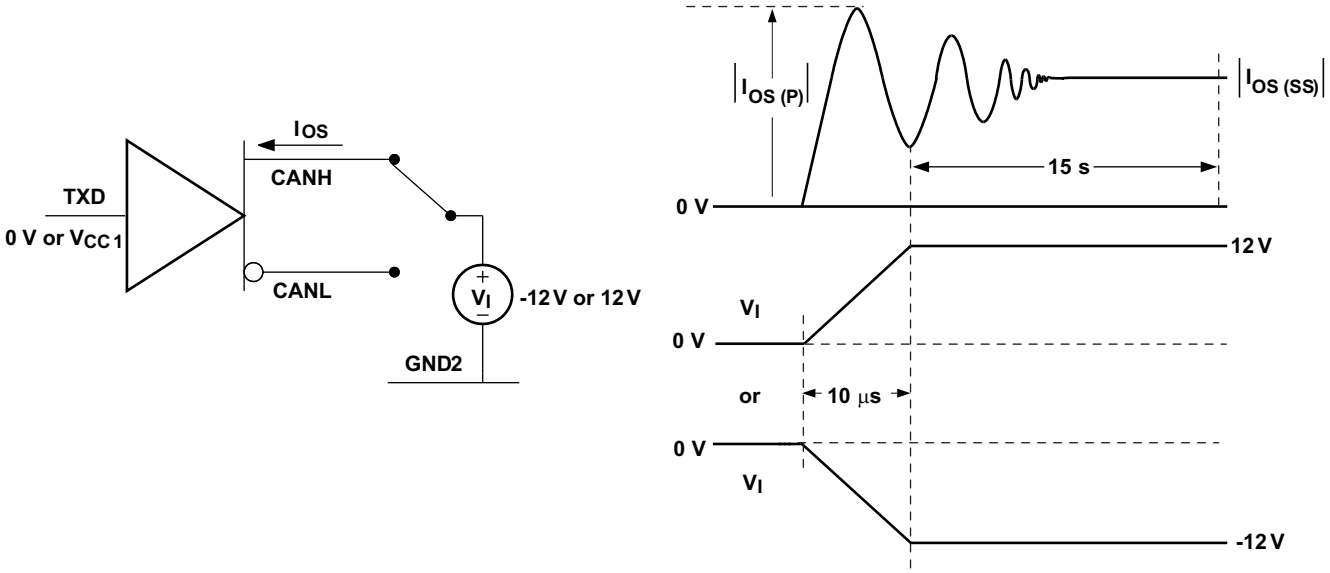


Figure 11. Driver Short-Circuit Current Test Circuit and Waveforms

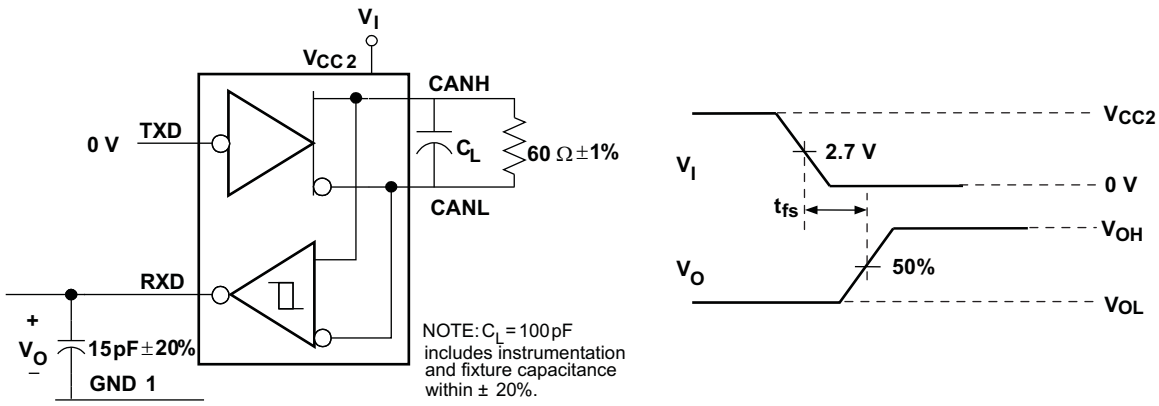


Figure 12. Failsafe Delay Time Test Circuit and Voltage Waveforms

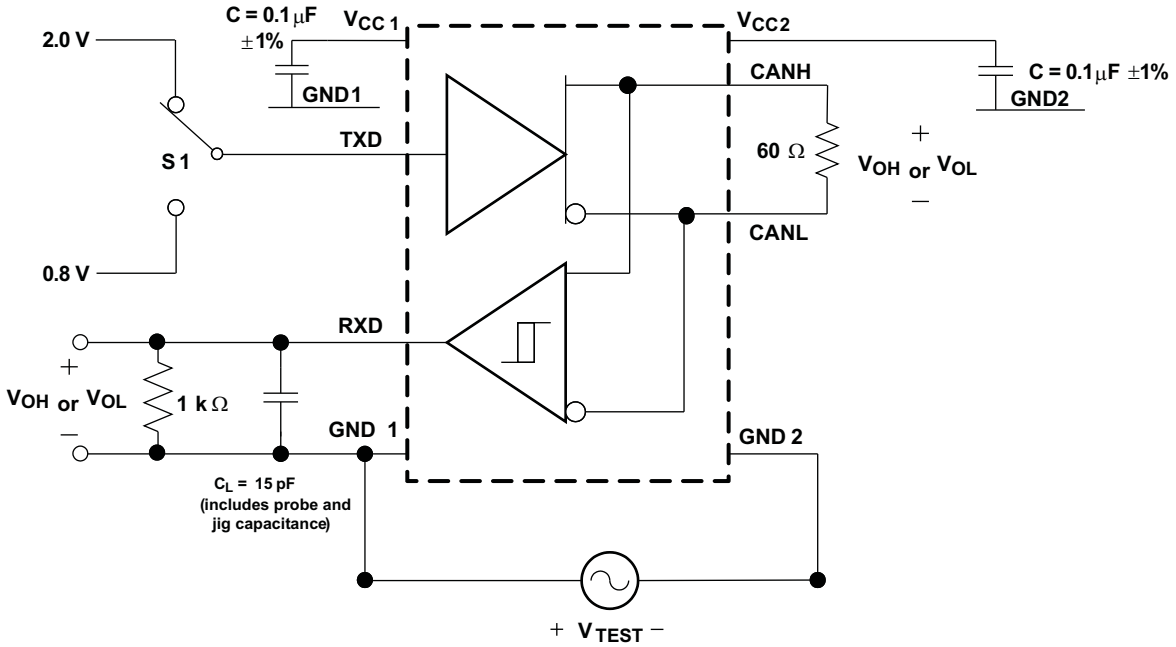


Figure 13. Common-Mode Transient Immunity Test Circuit

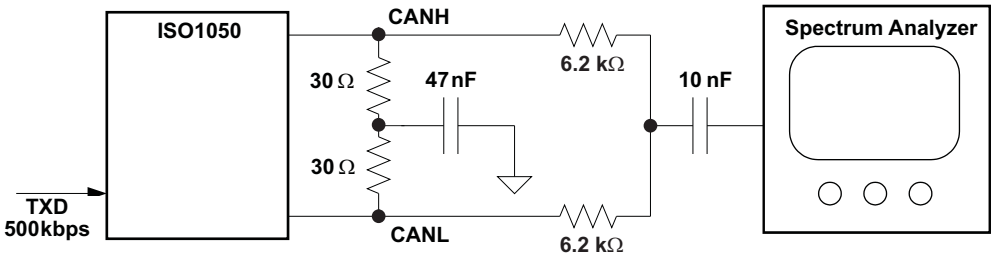


Figure 14. Electromagnetic Emissions Measurement Setup

DEVICE INFORMATION

FUNCTION TABLE(1)

DRIVER					RECEIVER		
INPUTS	OUTPUTS		BUS STATE		DIFFERENTIAL INPUTS V_{ID} = CANH–CANL	OUTPUT RXD	BUS STATE
TXD	CANH	CANL					
L(2)	H	L	DOMINANT		$V_{ID} \geq 0.9$ V	L	DOMINANT
H	Z	Z	RECESSIVE		0.5 V < V_{ID} < 0.9 V	?	?
Open	Z	Z	RECESSIVE		$V_{ID} \leq 0.5$ V	H	RECESSIVE
X	Z	Z	RECESSIVE		Open	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance
(2) Logic low pulses to prevent dominant time-out.

DEVICE INFORMATION

ISOLATOR CHARACTERISTICS (1) (2)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	DUB-8	6.1			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	DUB-8	6.8			mm
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	DW-16	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	DW-16	8.10			mm
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation		0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, Tamb < 100°C			$>10^{12}$		Ω
		Input to output V_{IO} = 500 V, 100°C ≤Tamb <≤Tamb max			$>10^{11}$		Ω
C_{IO}	Barrier capacitance	V_I = 0.4 sin (4E6πt)			1.9		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)			1.3		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

(2) Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

IEC SAFETY LIMITING VALUES

safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	SOIC-8	θ_{JA} = 212 °C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			124	mA
			θ_{JA} = 212 °C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			190	
T_S	Maximum case temperature	SOIC-8				150	°C

The safety-limiting constraint is the absolute maimum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assured junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program(1)
File Number: pending	File Number: pending	File Number: pending

(1) Production tested ≥ 3000 VRMS for 1 second in accordance with UL 1577.

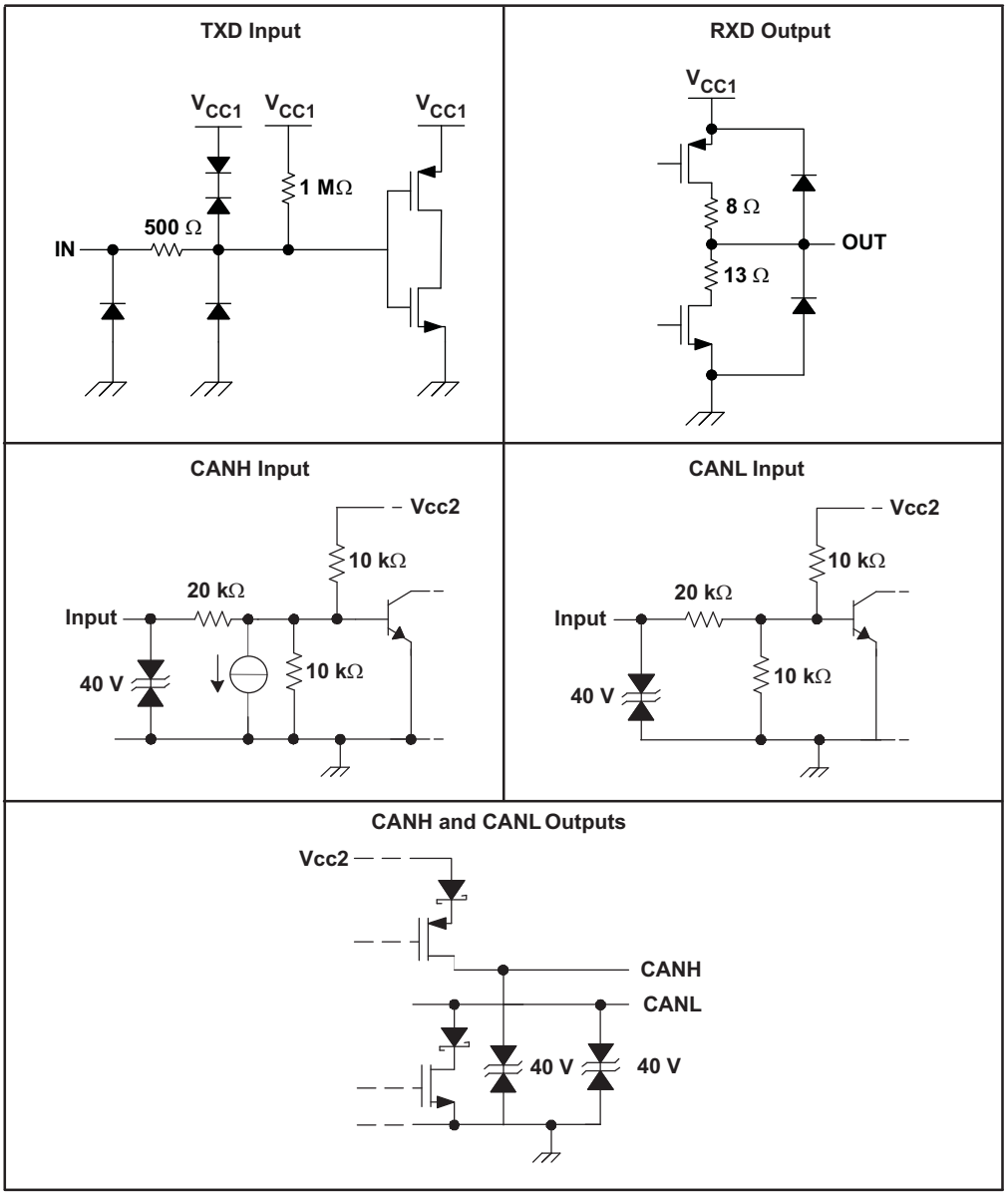
THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance(1)		120		°C/W
		High-K Thermal Resistance		73.3		°C/W
θ_{JB}	Junction-to-board thermal resistance	Low-K Thermal Resistance		10.2		°C/W
θ_{JC}	Junction-to-case thermal resistance	Low-K Thermal Resistance		14.5		°C/W
P_D	Device power dissipation	V_{CC1}=5.5V, V_{CC2}=5.25V, T_A=105°C, R_L= 60Ω, TXD input is a 500kHz 50% duty-cycle square wave			200	mW
$T_{j\ shutdown}$	Thermal shutdown temperature(2)			190		°C

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.
(2) Extended operation in thermal shutdown may affect device reliability.

EQUIVALENT I/O SCHEMATICS



TYPICAL CHARACTERISTICS

RECESSIVE-TO-DOMINANT LOOP TIME
vs
FREE-AIR TEMPERATURE (across Vcc)

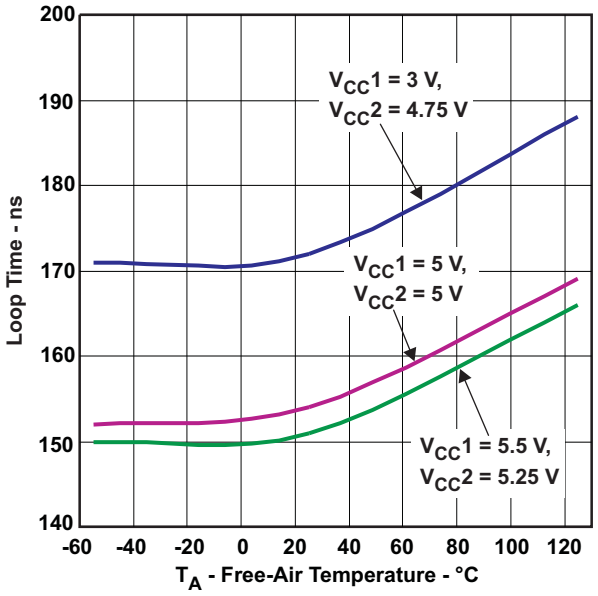


Figure 15.

DOMINANT-TO-RECESSIVE LOOP TIME
vs
FREE-AIR TEMPERATURE (across Vcc)

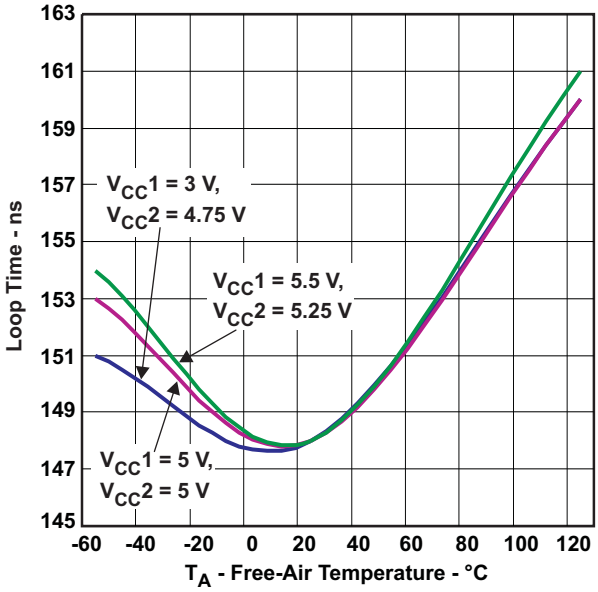


Figure 16.

SUPPLY CURRENT (RMS)
vs
SIGNALING RATE (kbps)

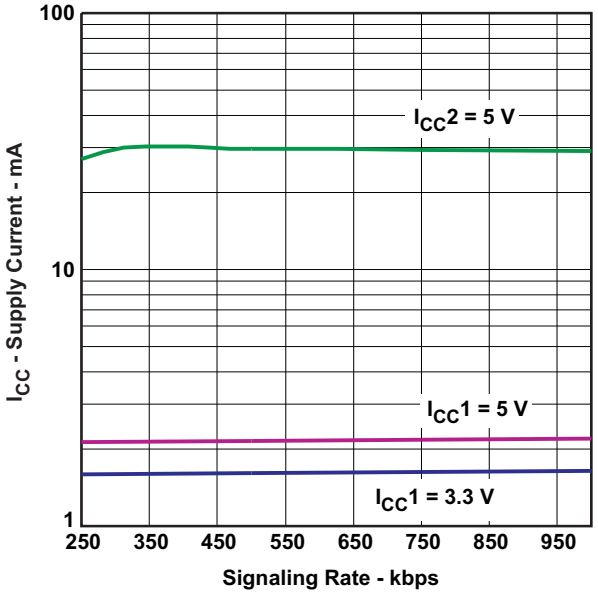


Figure 17.

DRIVER OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

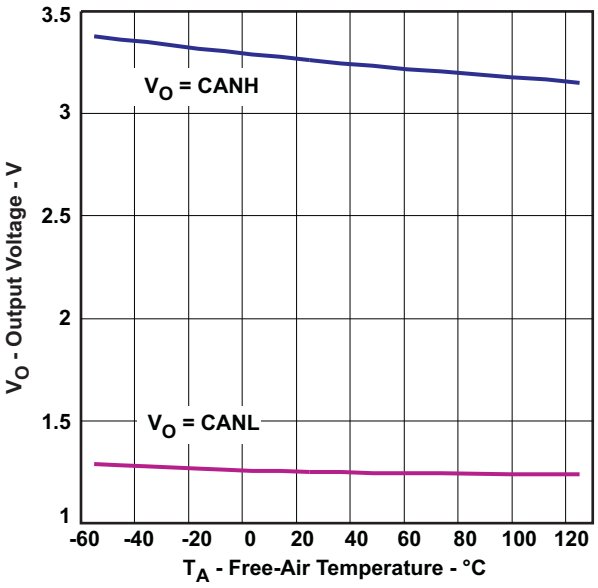


Figure 18.

TYPICAL CHARACTERISTICS (continued)

EMISSIONS SPECTRUM TO 10 MHz

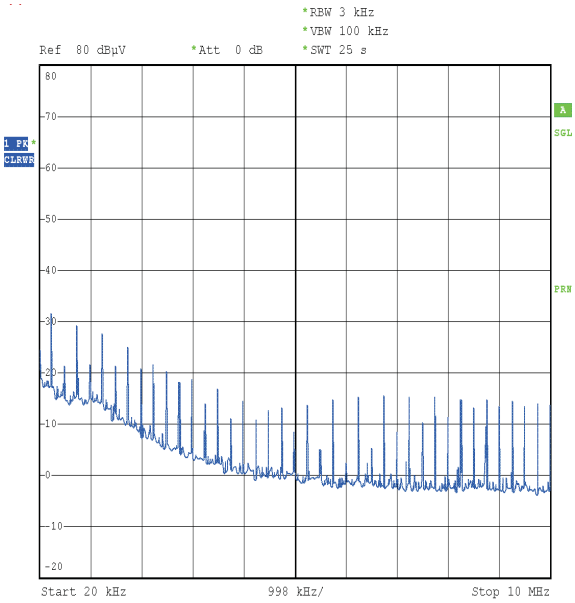


Figure 19.

EMISSIONS SPECTRUM TO 50 MHz

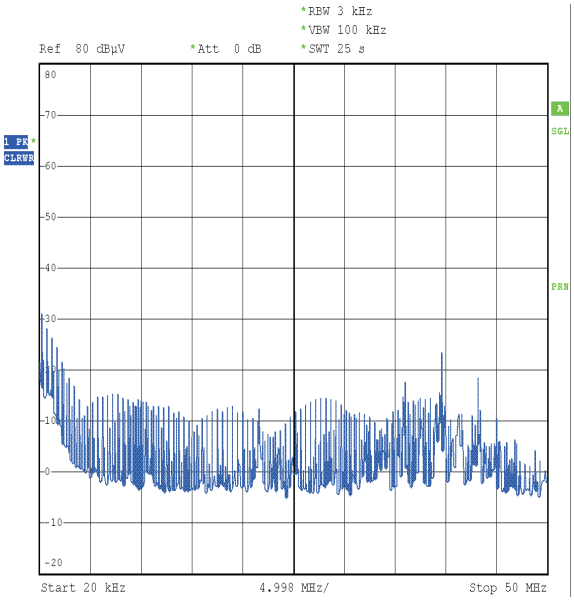


Figure 20.

APPLICATION INFORMATION

DOMINANT TIME-OUT

A dominant time-out circuit in the ISO1050 prevents the driver from blocking network communications if a local controller fault occurs. The time-out circuit is triggered by a falling edge on TXD. If no rising edge occurs on TXD before the time-out of the circuits expires, the driver is disabled to prevent the local node from continuously transmitting a Dominant bit. If a rising edge occurs on TXD, commanding a Recessive bit, the timer will be reset and the driver will be re-enabled. The time-out value is set so that normal CAN communication will not cause the Dominant time-out circuit to expire.

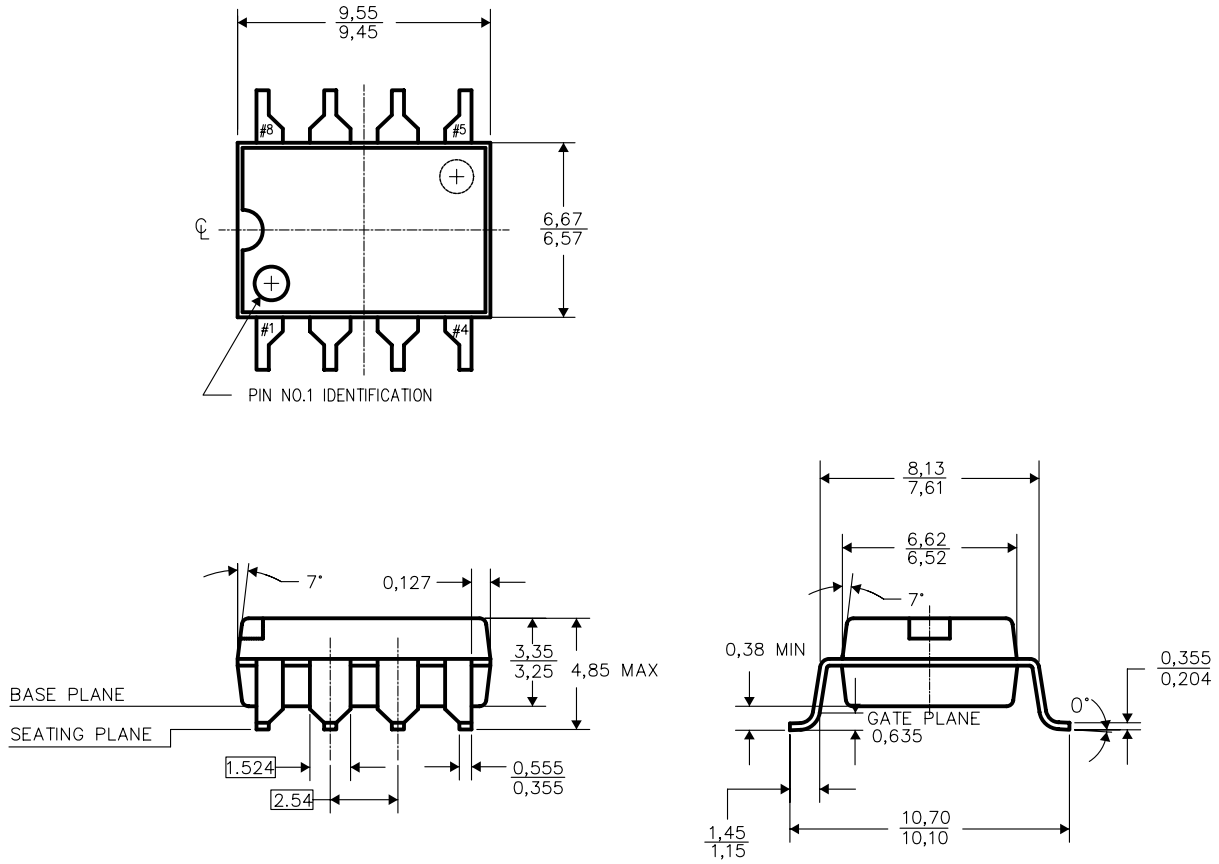
FAILSAFE

If the bus-side power supply Vcc2 is lower than about 2.7V, the power shutdown circuits in the ISO1050 will disable the transceiver to prevent spurious transitions due to an unstable supply. If Vcc1 is still active when this occurs, the receiver output will go to a failsafe HIGH value in about 6 microseconds.

THERMAL SHUTDOWN

The ISO1050 has an internal thermal shutdown circuit that turns off the driver outputs when the internal temperature becomes too high for normal operation. This shutdown circuit prevents catastrophic failure due to short-circuit faults on the bus lines. If the device cools sufficiently after thermal shutdown, it will automatically re-enable, and may again rise in temperature if the bus fault is still present. Prolonged operation with thermal shutdown conditions may affect device reliability.

DUB (R–PDSO–G8) PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ANSI Y14.5 M–1982.
B. This drawing is subject to change without notice.
C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.254mm.

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