APDS-9120

Integrated Optical Proximity Sensors

Data Sheet

Description

Avago's APDS-9120 is an integrated optical proximity sensor that combines built-in signal conditioning and space-saving packaging technology.

This integrated sensor provides ease of use, as it eliminates design efforts required in implementing external LED drivers, signal filtering and amplification, sunlight and ambient light immunity and LED stuck high protection circuit.

APDS-9120 is designed to be a robust proximity sensor. It has artificial light immunity and operates in sunlight exposure. Both analog and/or digital output options are available.

To maximize power savings and battery life in applications such as portable or battery-operated devices, APDS-9120 has a shutdown mode feature. With an external limiting resistor, the LED current of the optical proximity sensors can be configured to various levels. The pulse width, burst rate, duty cycle and frequency can be controlled to minimize power consumption. These features make it ideal for low power mobile and handheld devices.

Application Support Information

The Application Engineering Group is available to assist you with the application design associated with APDS-9120 module. You can contact them through your local sales representatives for additional details.

Features

- Small form factor with conditioning IC, emitter and detector integrated into one single package
  - H1.1mm x W4.4mm x L4.4mm
- Low power consumption
  - LED pulse width control
  - Low shut down current
  - External LED drive-current control
- Shutdown current 1uA max
- Supply voltage : 2.4 V to 3.6 V
- Typical detection distance 30mm based on Kodak 18% grey card
- Artificial light immunity
- Operational in sunlight conditions
- Analog & Digital output available
  - Built in hysteresis comparator for digital output
- LED stuck Hi protection

Applications

- PDA and mobile phones
- Portable and Handheld devices
- Personal Computers/Notebooks
- Contactless Switches

Ordering Information

Part Number	Package Type	Shipping Option
APDS-9120-020	Tape & Reel	2500

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Min.	Max.	Units	Conditions
Supply Voltage	V_{CC}	0	4.0	V	
Peak LED Current	ILEDpk	0	500	mA	Pulsed at 12.5% Duty-cycle
Reflow Soldering Temperature			260	°C	
Input Logic Voltage	VI	0	4.0	V	

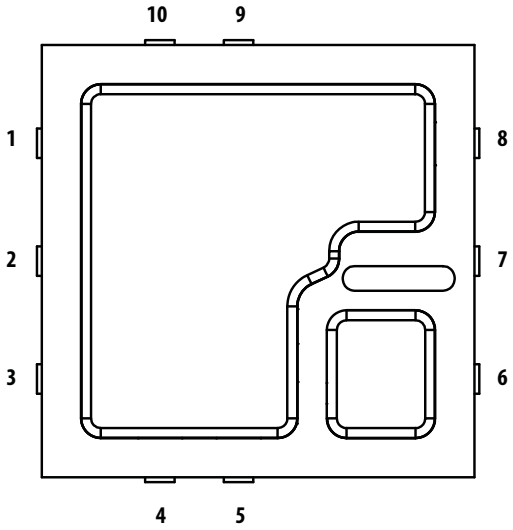
Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Conditions
Operating Temperature	T_A	-40	85	°C	
Storage Temperature	T_S	-40	100	°C	
Supply Voltage	V_{CC}	2.4	3.6	V	

Electrical & Optical Specifications (Ta=25°C)

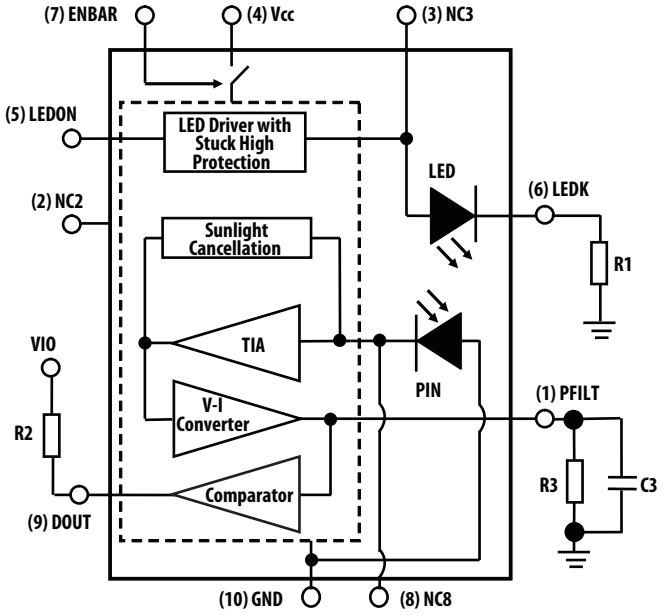
Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input						
Logic High Voltage, LEDON	V_{IH}	1.6	–	V_{CC}	V	
Logic High Voltage, ENB	V_{IH}	1.4	–	V_{CC}	V	For V_{CC} = 2.4V
		1.5	–	V_{CC}	V	For 2.4 < V_{CC} ≤ 3V
		1.7	–	V_{CC}	V	For 3 < V_{CC} ≤ 3.6V
Logic Low Voltage, LEDON	V_{IL}	0	–	0.3	V	
Logic Low Voltage, ENB	V_{IL}	0	–	0.3	V	
Logic High Input Current, LEDON	I_{IH}	–	0.1	1	uA	$V_I \geq V_{IH}$
Logic High Input Current, ENB	I_{IH}	–	0.1	1	µA	$V_I \geq V_{IH}$
Logic Low Input Current, LEDON	I_{IL}	–	0.1	1	µA	$V_I \leq V_{IL}$
Logic Low Input Current, ENB	I_{IL}	–	0.1	1	µA	$V_I \leq V_{IL}$
Shutdown Current	I_{SD}	–	0.3	1	uA	V_{CC} = 3V, ENB = 3V
Idle Current	I_{CC}	–	500	650	µA	V_{CC} = 3V, ENB = 0V
Output						
Analog Output	V_{PFILT}	1.25	1.9	2.55	V	V_{CC} = 3V, ENB = 0V, LEDON = 10 kHz, 50% DC, Continuous pulses; R3 = 1Mohm, C3 = 3.3nF; Kodak 18% grey card at detectable distance = 10mm from the APDS-9120
Digital Output	V_{OL}	0	–	0.3	V	$I_{DOUT(Low)}$ = 2mA, V_{CC} = 3V
Rise Time(DOUT)	T_R	–	1	–	us	V_{CC} = 3V, R2 = 10kΩ, Frequency = 10kHz
Fall Time(DOUT)	T_F	–	1	–	us	V_{CC} = 3V, R2 = 10kΩ, Frequency = 10kHz
Transmitter						
Max I_{LED} Pulse Width	Max-PW	–	120	–	µs	V_{CC} = 3V, ENB = 0V
I_{LED} Peak Pulse Current	ILEDpk	85	120	155	mA	V_{CC} = 3V, R1 = 10Ω
Hysterisis Comparator						
Hysterisis	V_{HYS}	–	40	–	mV	V_{CC} = 3V
Threshold Voltage	V_{TH}	–	655	–	mV	V_{CC} = 3V
Ambient light tolerance			100k	-	lux	Sun light
			10K	-		Incandescent
			5K	-		Fluorescent
			10K	-		Halogen

APDS-9120 I/O Pins Configuration Table



Pin	Symbol	Type	Description
1	PFILT	Analog O/P	Analog Output Connect to integration circuit (R3 & C3)
2	NC2	–	No Connection
3	NC3	–	No Connection
4	V_{CC}	Supply	Voltage Supply
5	LEDON	Digital I/P	LED Driver Input LEDA will turn off when LEDON is stuck in high state for more than Max-PW
6	LEDK	LED Cathode	Connect to a current limiting resistor
7	ENBAR	Digital I/P	Power Down Enable ENB = 0 Normal mode operation ENB = 1 Shut down mode
8	NC8	–	No Connection
9	DOUT	Digital O/P	Digital Output An open drain output that requires a pull-up resistor of recommended value 10kΩ DOUT = 0 when VPFILT > VTH DOUT = V_{CC} when VPFILT < VTH
10	GND	Ground	Ground

APDS-9120 Internal Block Diagram



Typical Characteristics

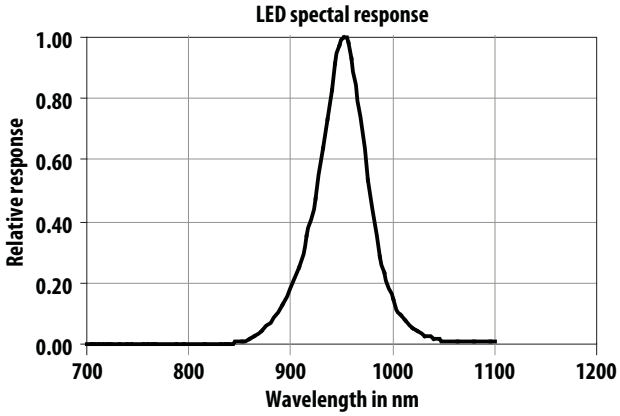


Figure 1. LED emitting spectrum

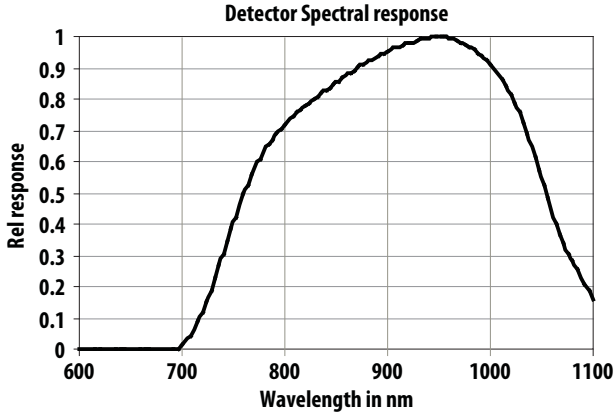


Figure 2. PIN spectral sensitivity

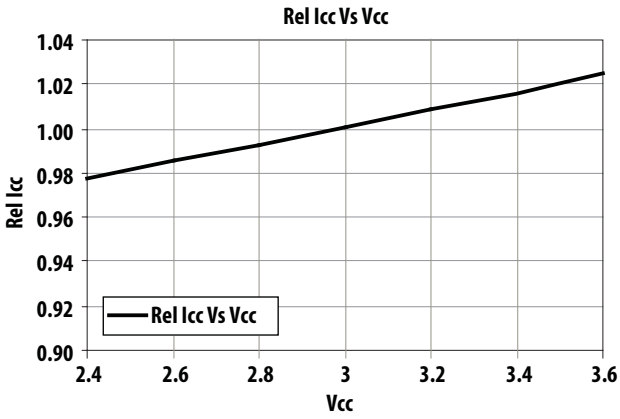


Figure 3. Relative supply current over supply voltage

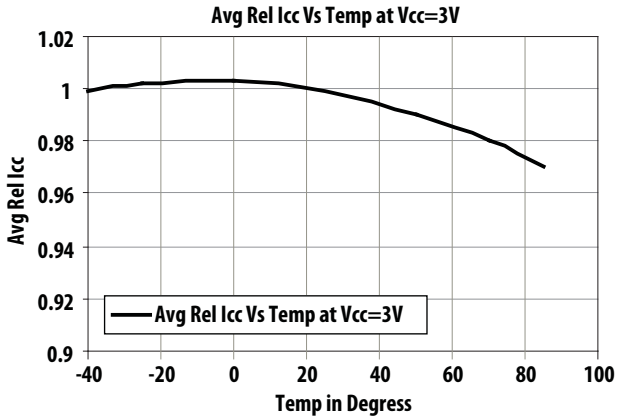


Figure 4. Average relative supply current over temperature

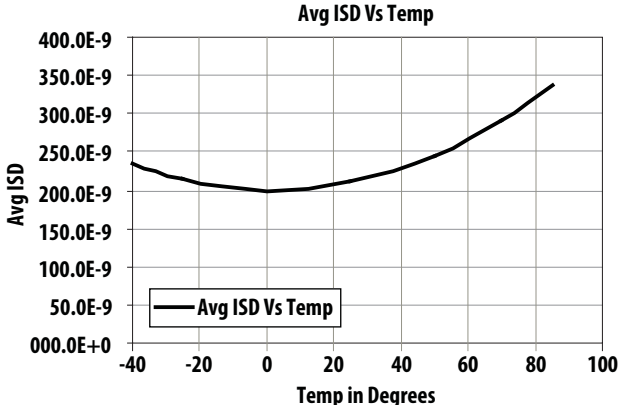


Figure 5. Average shutdown current over temperature

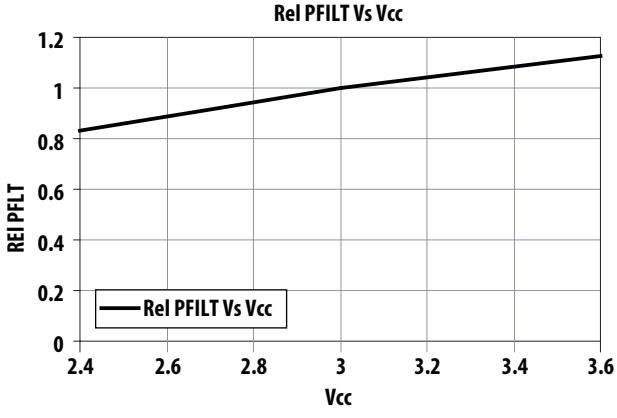


Figure 6. Relative output PFILT over supply voltage

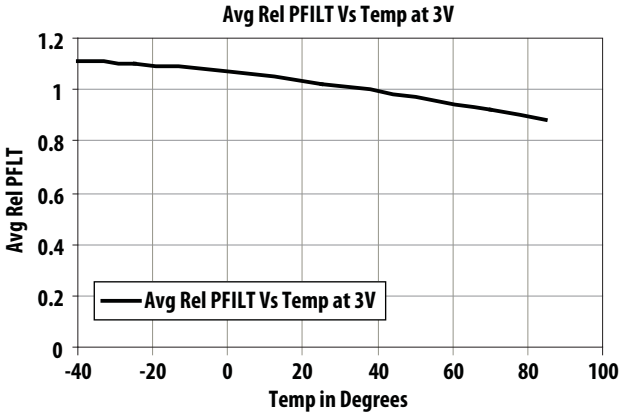


Figure 7. Average relative output PFILT over temperature

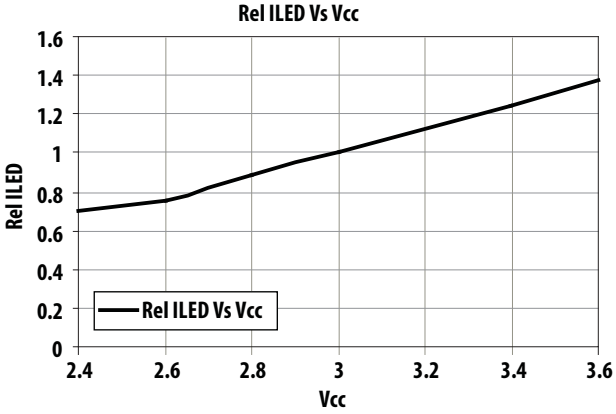


Figure 8. Relative ILED current over temperature

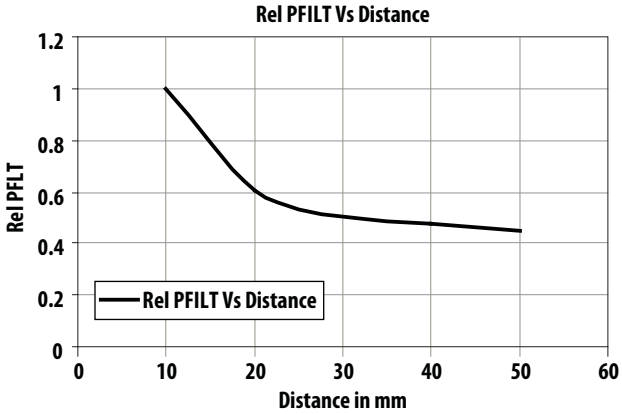


Figure 9. Relative output PFILT over detection distance

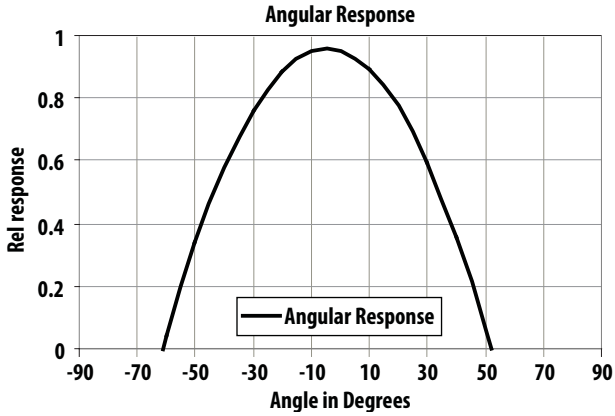
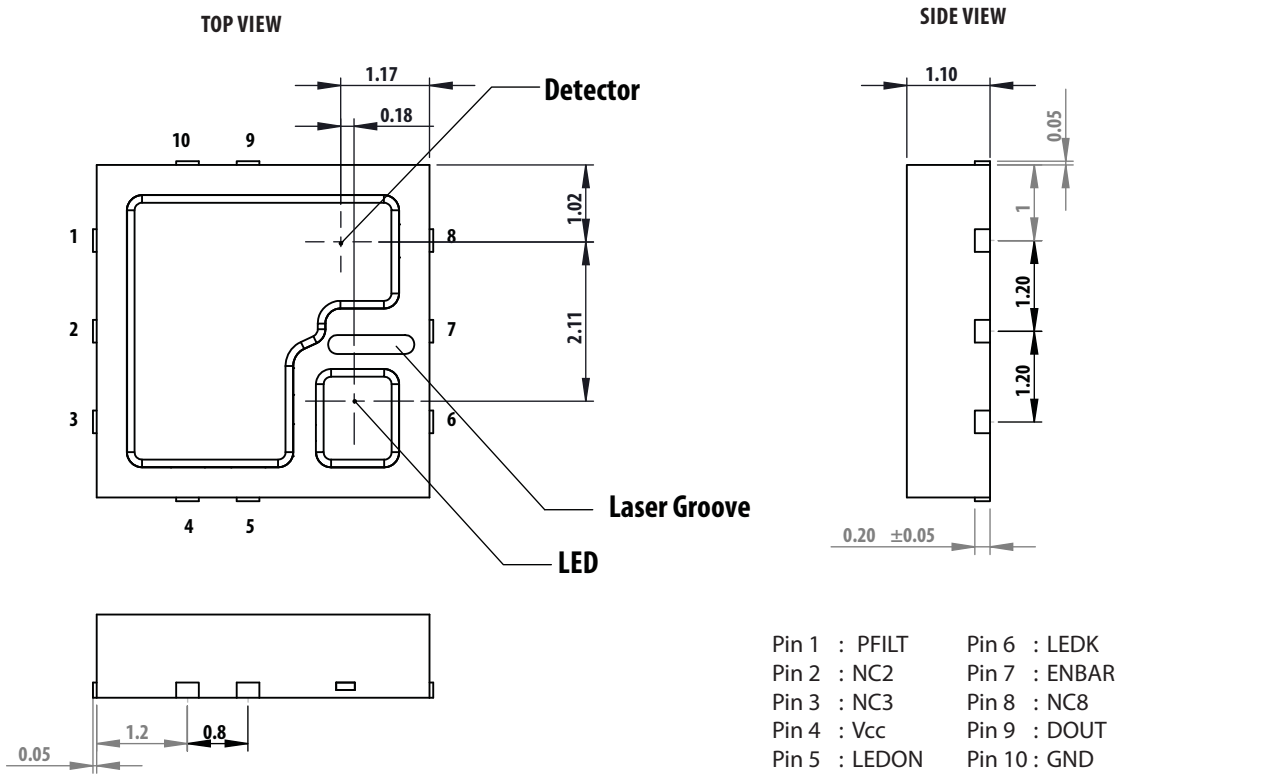
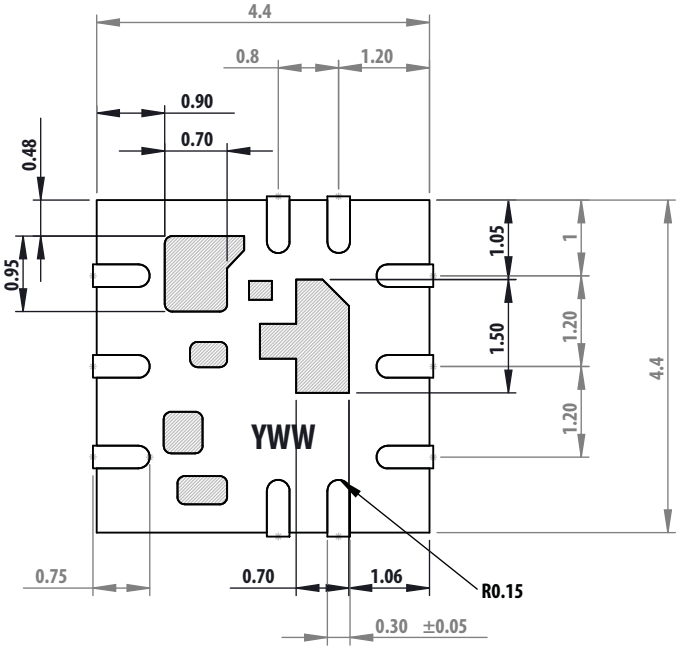


Figure 10. Angular response

APDS-9120 Package Dimensions



Pin 1	: PFILT	Pin 6	: LEDK
Pin 2	: NC2	Pin 7	: ENBAR
Pin 3	: NC3	Pin 8	: NC8
Pin 4	: Vcc	Pin 9	: DOUT
Pin 5	: LEDON	Pin 10	: GND

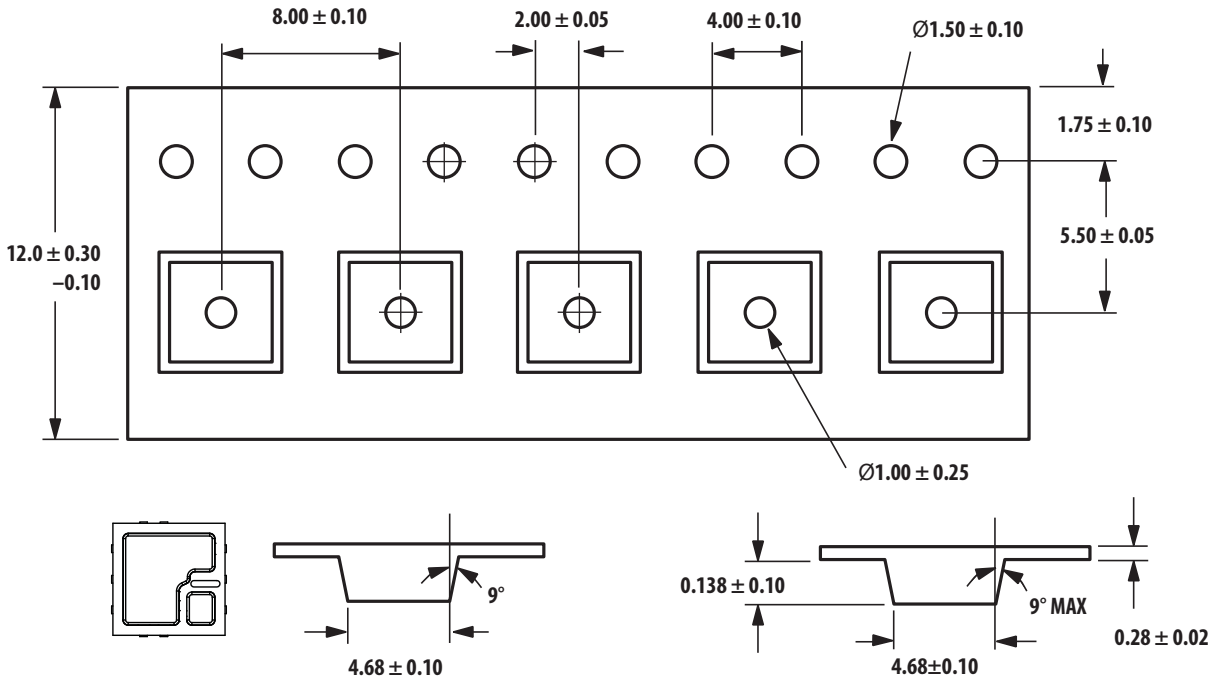


MARKING DETAILS

Font type	: Stroke Roman
Font size	: 0.3mm
Marking type	: Laser
Format	: YWW
	Y = Year (last digit)
	WW = Week number (two digits)

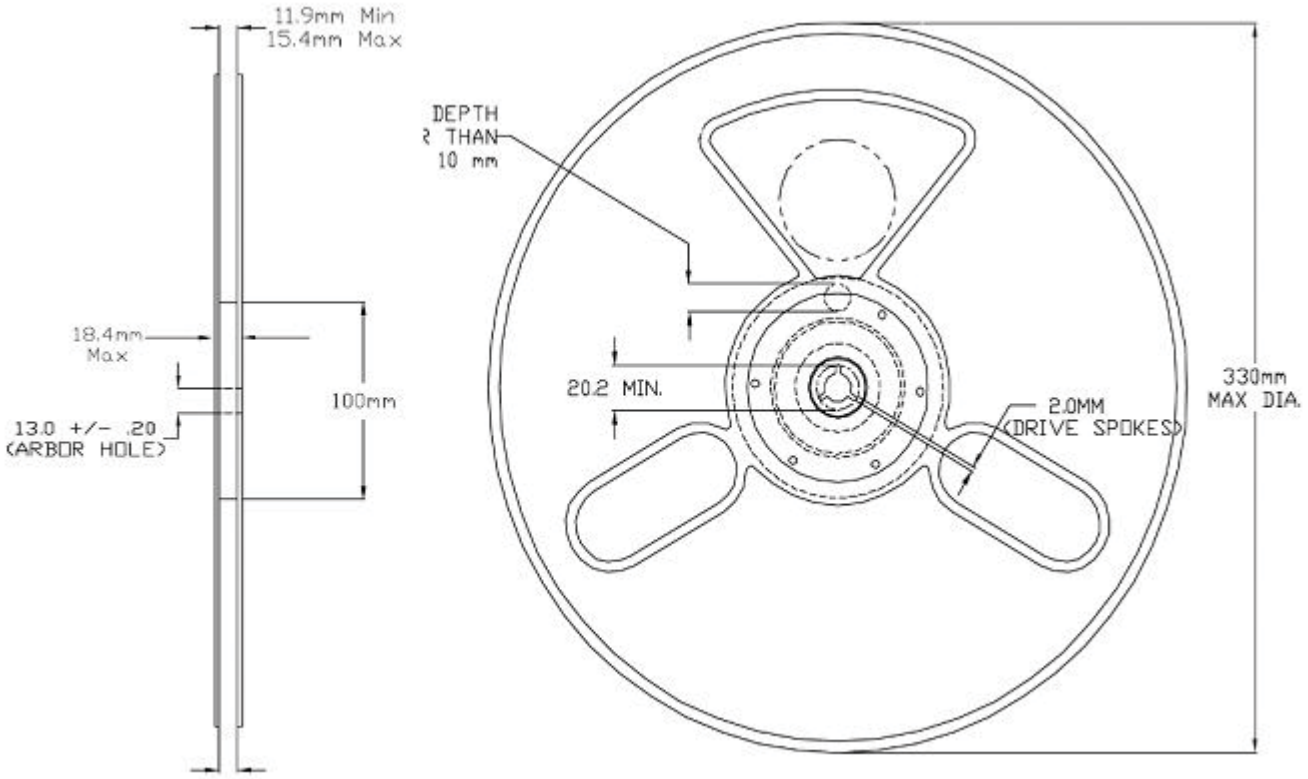
Notes:
1. All dimensions are in millimeters. Dimension tolerance is ±0.1 mm unless otherwise stated.
2. This package contains no lead.
3. Do NOT connect the bottom exposed pads.
4. No PCB circuitry under the device.

Tape and Reel Dimensions

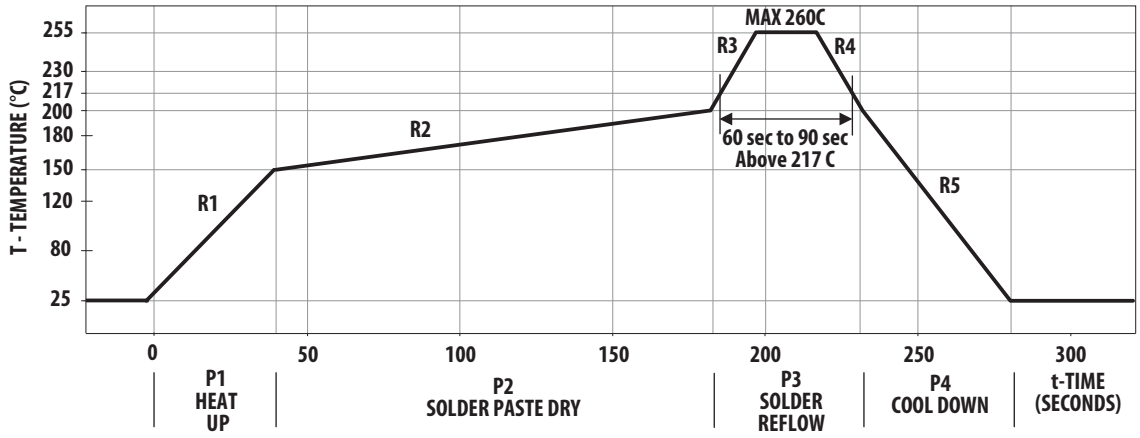


Dimensions in mm

Reel Drawings



Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime or Duration
Heat Up	P1, R1	25°C to 150°C	3°C/s
Solder Paste Dry	P2, R2	150°C to 200°C	100s to 180s
Solder Reflow	P3, R3 P3, R4	200°C to 260°C 260°C to 200°C	3°C/s -6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s
Time maintained above liquidus point, 217°C		> 217°C	60s to 120s
Peak Temperature		260°C	–
Time within 5°C of actual Peak Temperature		–	20s to 40s
Time 25°C to Peak Temperature		25°C to 260°C	8mins

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates or duration. The ΔT/Δtime rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and component pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 260°C (500°F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 90 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

SMT Assembly Application Note

1.1 Solder Pad, Mask and Metal Stencil Aperture

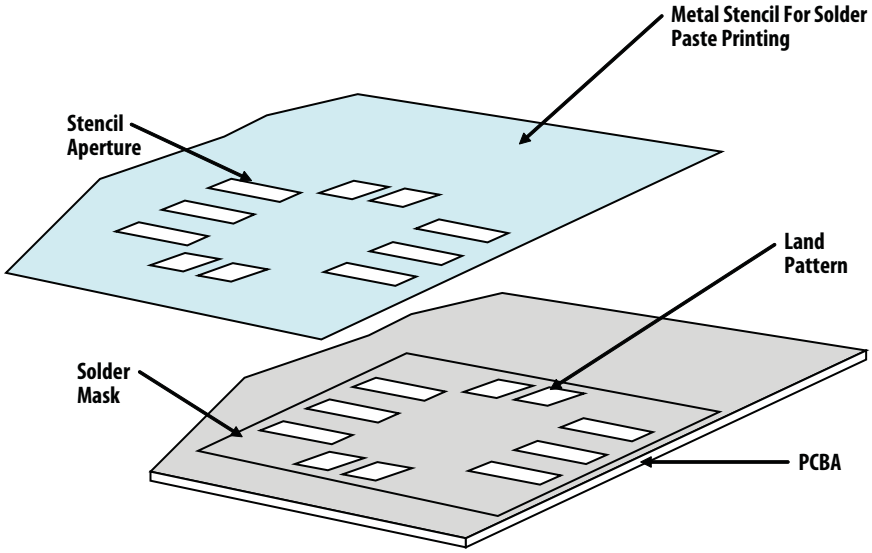
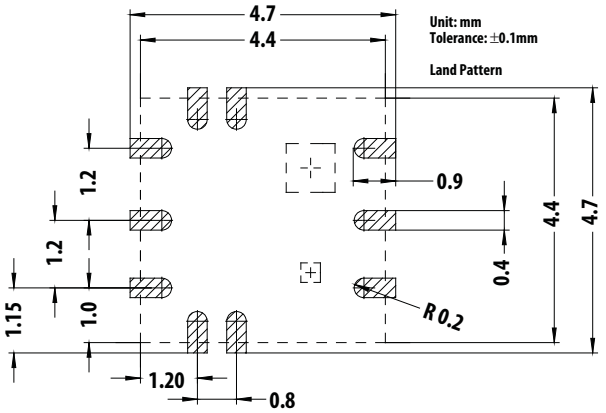


Figure 11. Stencil and PCBA

1.2 Recommended Land Pattern



Notes:
1. Do NOT connect the NC (no connect) pins.
2. Manual soldering on APDS-9120 is not recommended. Please refer to Recommended Reflow Profile for soldering.

Figure 12. Recommended Land Pattern

1.3 Recommended Metal Solder Stencil Aperture

It is recommended that a 0.11 mm thick stencil be used for solder paste printing. Aperture opening for shield pad is 0.8mm x 0.4mm (as per land pattern). This is to ensure adequate printed solder paste volume and no shorting.

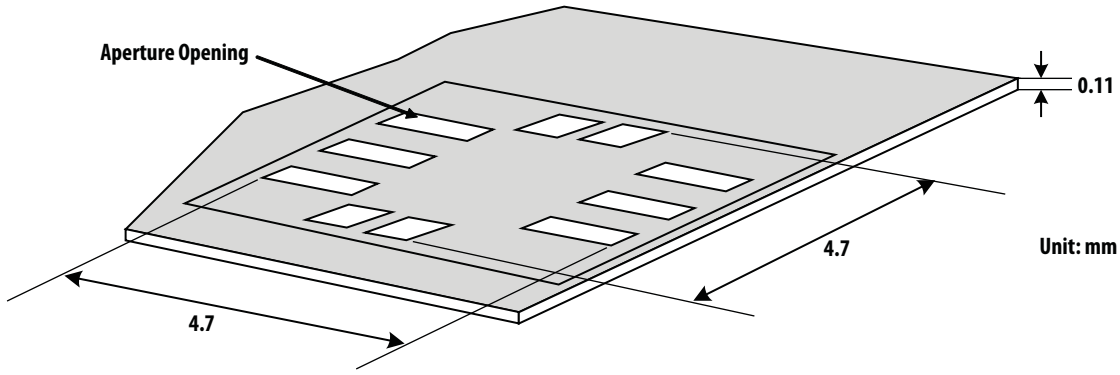


Figure 13. Solder Stencil Aperture

1.4 Adjacent Land Keepout and Solder Mask Areas

Adjacent land keep-out is the maximum space occupied by the unit relative to the land pattern. There should be no other SMD components within this area.

The minimum solder resist strip width required to avoid solder bridging adjacent pads is 0.2 mm.

Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.

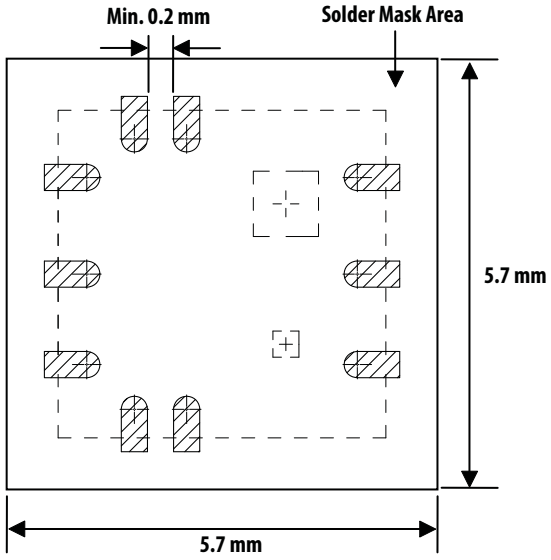
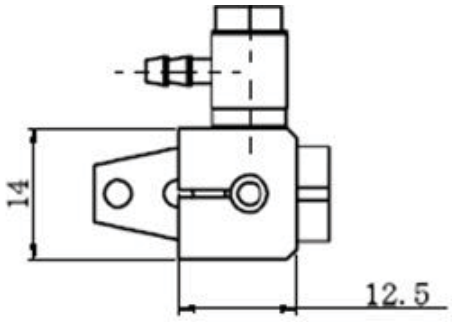


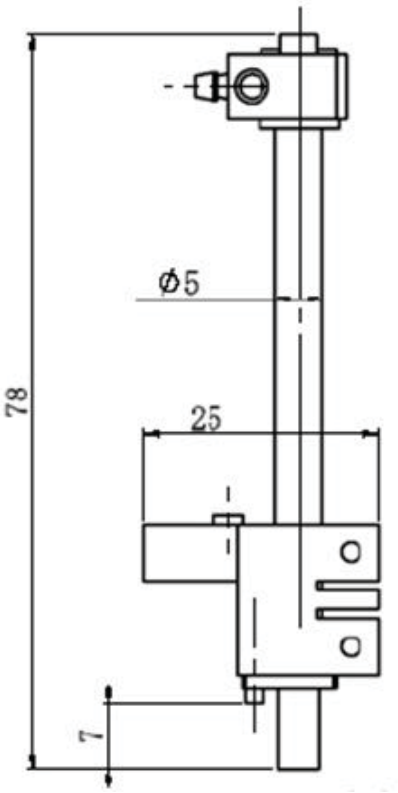
Figure 14. Adjacent Land Keepout and Solder Mask Areas

Recommended Pickup Nozzle

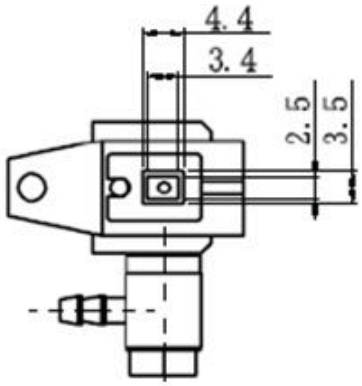
TOP VIEW



SIDE VIEW

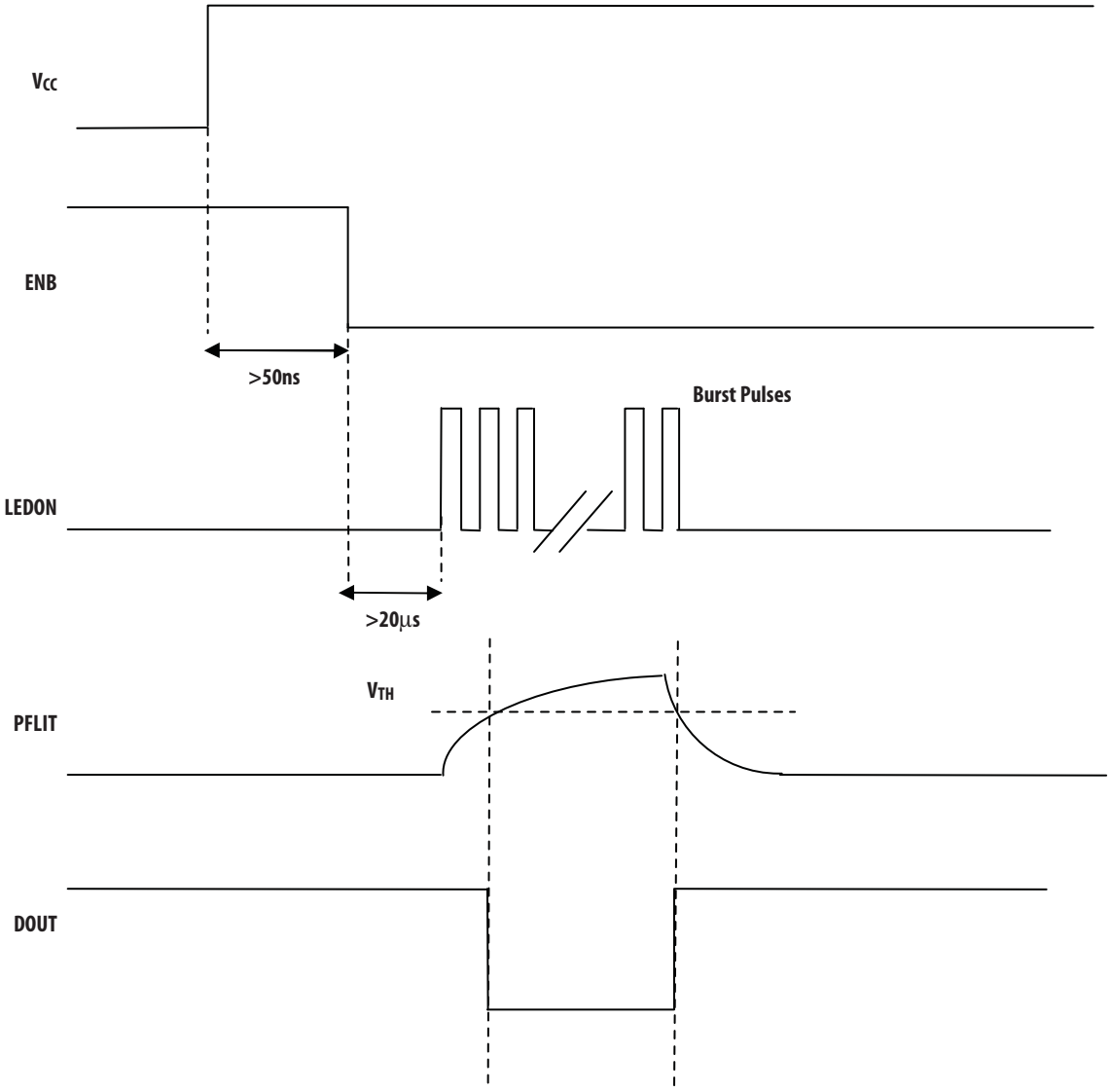


BOTTOM VIEW



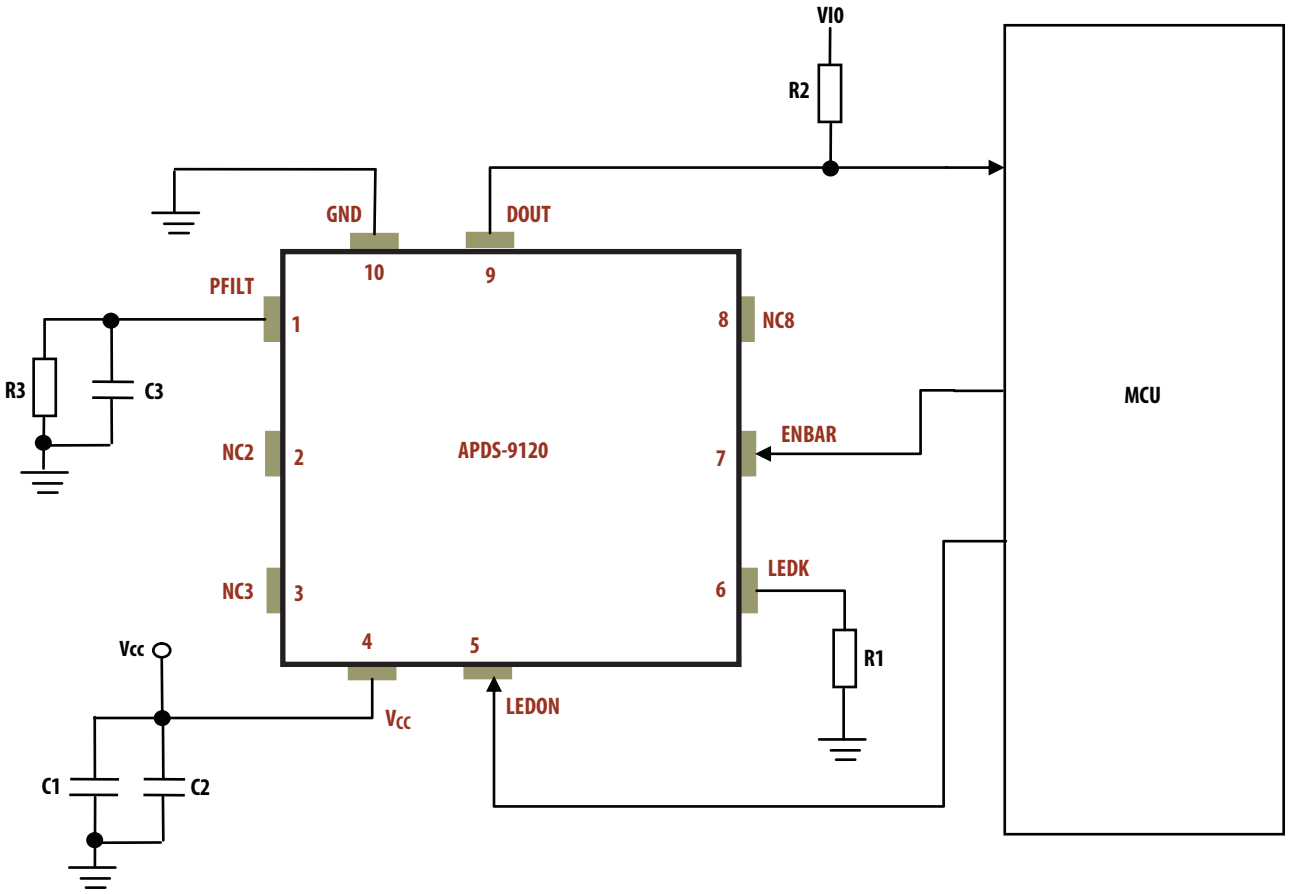
Dimension in mm

APDS-9120 Typical Timing Waveforms



Note:
Pulses at LEDON can only be activated at least 20us after ENB turn from high to low.

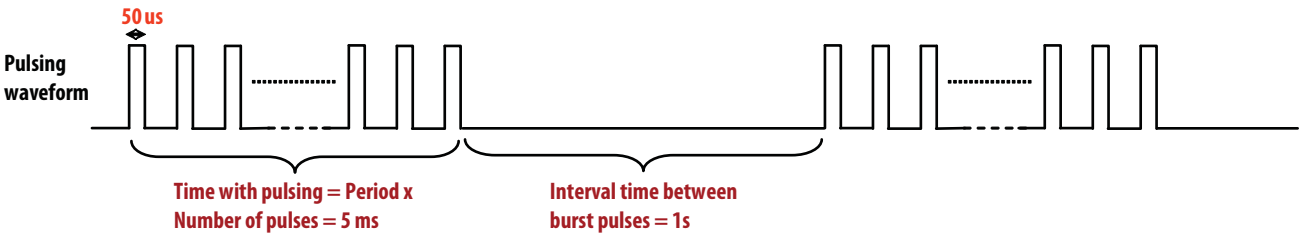
Typical Application Circuit



Note:
1. Do NOT connect the NC (no connect) pins

Recommended Operating Condition

(a) Recommended burst pulse to drive LEDON (pin5) :



R1	10 ohm
Iled (typ)	120mA
Number of Burst Pulse	50
Period of Burst Pulse	100us
Duty Cycle of Burst Pulse	50%
Interval Between Burst Pulse	1 sec

(b) Recommended components used:

Component	Recommended Values
R1	10 ohm
R2	10k ohm
R3	1M ohm
C1	100nF, Ceramic
C2	6.8uF, Tantalum
C3	3.3nF, Ceramic

Note:

1. R3 and C3 are integrated circuit that can be adjusted to meet desired detectable distance
2. Detectable distance is the distance when the object is first detected to trigger a "LOW" at DOUT (pin9).

Appendix A1: Window and Light Guide Design Guide

To ensure that the performance of the APDS-9120 will not be affected by improper window design, there are some criteria requested on the dimensions and design of the window.

It is recommended that two separate light guides being put on top of APDS-9120, one for the emitter and one for the photodiode to reduce the crosstalk level between the emitter and detector. Take note that the light guide centers must coincide with the holes opening at the emitter and the photodiode of APDS-9120. To have better performance, an opaque baffle is suggested to add in between the two light guides. A typical configuration of light guide is shown below, Fig. A1.

Both rectangular and round shape light guide can be used. The width of rectangular or diameter of round light guide is recommended as 1.2 mm for emitter side, and 1.3mm for detector side. The light guide can have a latch structure for mounting purpose. The length of light guide is recommended to be less than 5mm.

A thin transparent layer can also be added on the cover, for cosmetic purpose. This layer can be the ITO thin film also for resistive touch panel purpose. It is recommended that this layer to be <0.5mm. Adding the light guide and window, the detected signal at a given LED driving setting will be reduced, the value of which will be dependant to the light guide dimensions and configurations, as well as the transparency of the materials. It is recommended to use high transparency epoxy (T>85%), for example, GE 121R for the light guide.

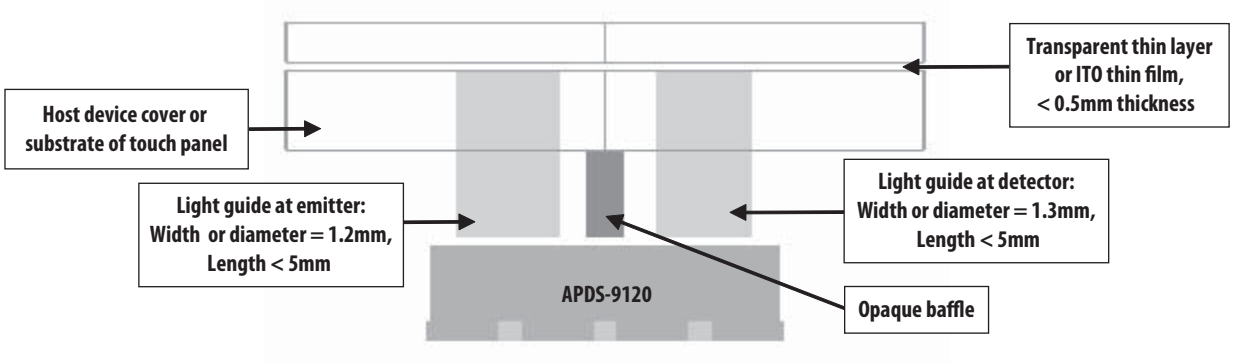


Figure A1. Recommended Window Design (Side view)

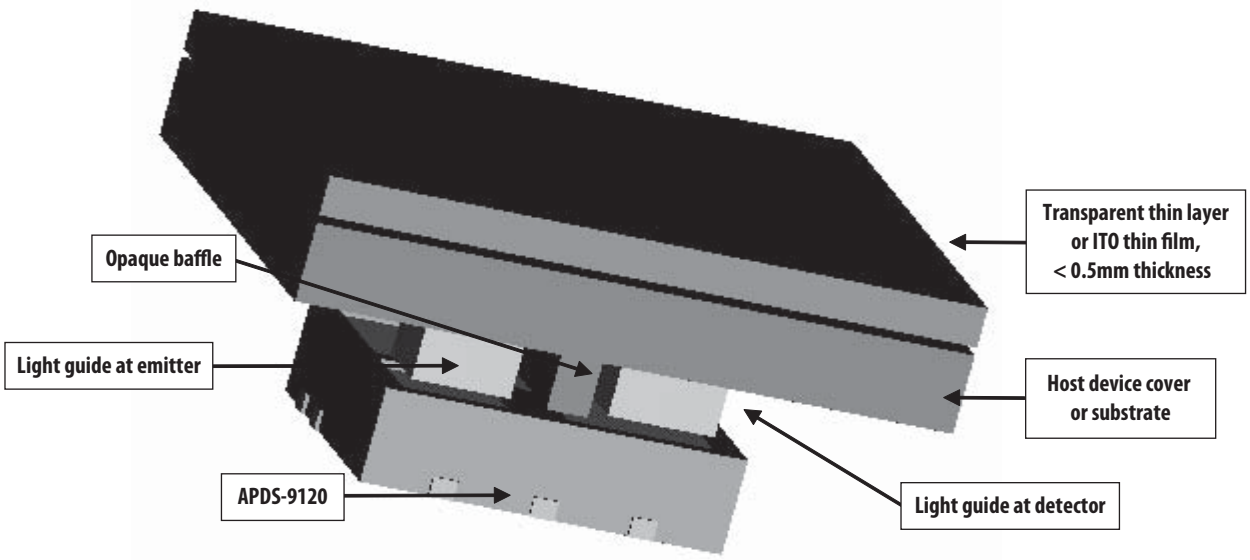


Figure A2. 3-D view of APDS-9120

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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