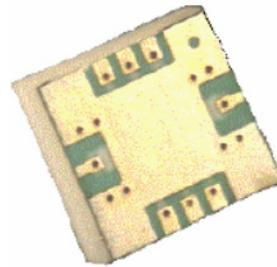


# AMMP-6333

18 – 33 GHz 0.2 W Driver Amplifier in SMT Package



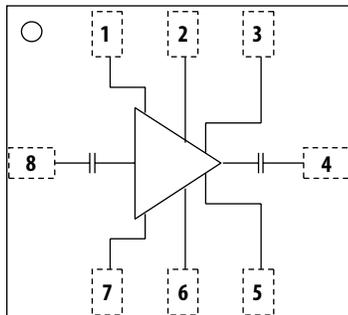
## Data Sheet



### Description

The AMMP-6333 is a broadband 0.2 W driver amplifier designed for use in transmitters operating in various frequency bands from 18 GHz to 33 GHz. This small, easy to use device provides over 23 dBm of output power ( $P_{-1dB}$ ) and more than 20 dB of gain at 25 GHz. It was optimized for linear operation with an output power at the third order intercept point (OIP3) of 30dBm. The AMMP-6333 features a temperature compensated RF power detection circuit that enables power detection sensitivity of 0.3 V/W at 25GHz. It is fabricated using Avago Technologies unique 0.25 $\mu$ m E-mode PHEMT technology which eliminates the need for negative gate biasing voltage.

### Pin Connections (Top View)



Pin	Function
1	Vg
2	Vd
3	DET_O
4	RF_out
5	DET_R
6	Vd
7	Vg
8	RF_in

### Features

- Frequency range: 18 to 33 GHz
- Small signal gain: 20 dB
- P-1dB : 23dBm
- Return Loss (In/Out): -10 dB

### Applications

- Microwave Radio systems
- Satellite VSAT, Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops



**Attention: Observe precautions for handling electrostatic sensitive devices.**  
ESD Machine Model (Class A) = 90 V  
ESD Human Body Model (Class 1A) = 300 V  
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

**Table 1. Absolute Maximum Ratings**

Symbols	Parameters	Unit	Maximum Values	Notes
V <sub>d</sub>	Positive Supply Voltage	V	5.5	2
V <sub>g</sub>	Gate Supply Voltage	V	0 to 5	
I <sub>d</sub>	Drain Current	mA	TBD	
P <sub>D</sub>	Power Dissipation	W	2	2 and 3
P <sub>in</sub>	CW Input Power	dBm	20	2
T <sub>ch</sub>	Operating Channel Temp	°C	+150	4
T <sub>stg</sub>	Storage Case Temp.	°C	-65 to +155	
T <sub>max</sub>	Maximum Assembly Temp (30 sec max)	°C	+320	

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Dissipated power P<sub>D</sub> depends on the DC voltage and power, input power and power delivered to the load
3. When operate at maximum P<sub>D</sub> with a base plate temperature of 85 °C, the median time to failure (MTTF) is significantly reduced.
4. These ratings apply to each individual FET. The operating channel temperature will directly affect the device MTTF.  
For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

**Table 2. DC Specifications/ Physical Properties**

Symbols	Parameters and Test Conditions	Units	Values
I <sub>d</sub>	Drain Supply Current (V <sub>d</sub> =5 V, V <sub>g</sub> set for typical I <sub>dQ</sub> – quiescent current)	mA	230
V <sub>g</sub>	Gate Supply Operating Voltage (I <sub>dQ</sub> = 230 mA)	V	2
I <sub>g</sub>	Gate Supply Current	mA	7
R <sub>θjc</sub>	Thermal Resistance (Channel-to-Backside)	°C/W	27
T <sub>ch</sub>	Channel Temperature	°C	115

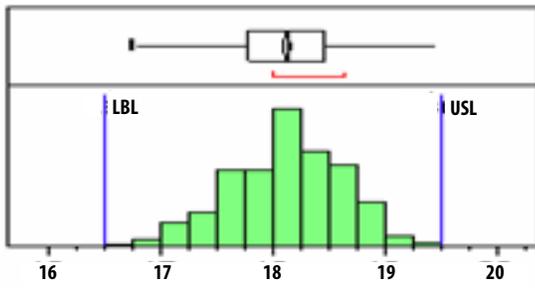
**Table 3. RF Specifications**T<sub>A</sub>= 25°C, V<sub>d</sub>=5, I<sub>d(Q)</sub>=230 mA, Z<sub>0</sub>=50 Ω

Symbols	Parameters	Units	17 – 20 GHz			20 – 30 GHz			30 – 33 GHz		
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
G	Small signal Gain	dB	16.5	18		19	22		20	23	
P <sub>-1dB</sub>	Output Power at 1dB Gain Compression	dBm	19	20.5		25	25.5		24	25.5	
P <sub>-3dB</sub>	Output Power at 3dB Gain Compression	dBm		21.5			24.5			23.5	
OIP3	Third Order Intercept	dBm		30			30			30	
RL <sub>in</sub>	Input Return Loss	dB		10			10			8	
RL <sub>out</sub>	Output Return Loss	dB		10			14			10	
	Reverse Isolation	dB		45			45			45	

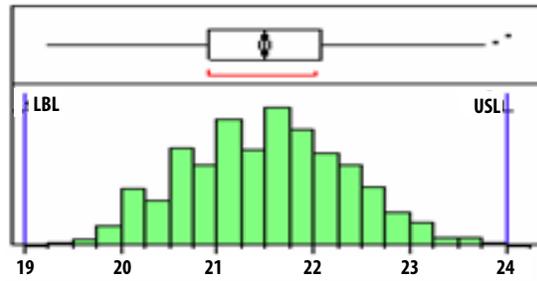
Note:

1. Measurements done on device attached to an evaluation board equipped with 2.4 mm connectors.
2. All tested parameters guaranteed with measurement accuracy ±2dB for P1dB of 17,25 and 32GHz, ±0.5 for Gain of 17GHz, ±1 for Gain of 25 and 32GHz.

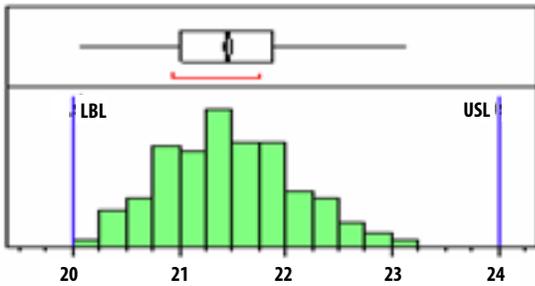
## Typical Distribution Charts



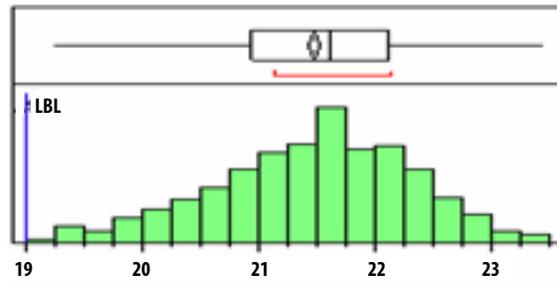
Gain at 17GHz



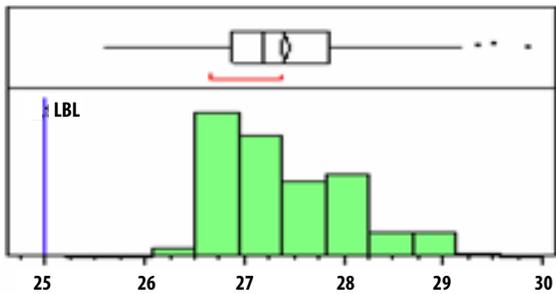
Gain at 25GHz



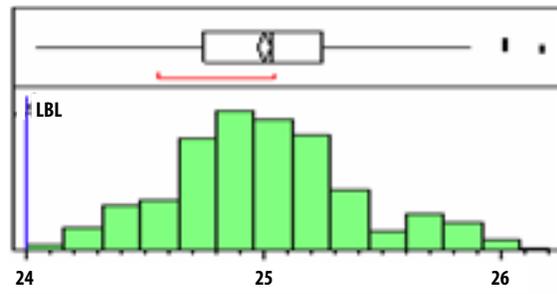
Gain at 32GHz



P1dB at 17GHz



P1dB at 25GHz



P1dB at 32GHz

## Typical Performance

( $T_A = 25^\circ\text{C}$ ,  $V_d = 5\text{ V}$ ,  $I_{dQ} = 230\text{ mA}$ ,  $Z_{in} = Z_{out} = 50\ \Omega$ )

(Data obtained from a test fixture with 2.4 mm connectors. Effects of the test fixture – losses and mismatch – have not been removed from the data)

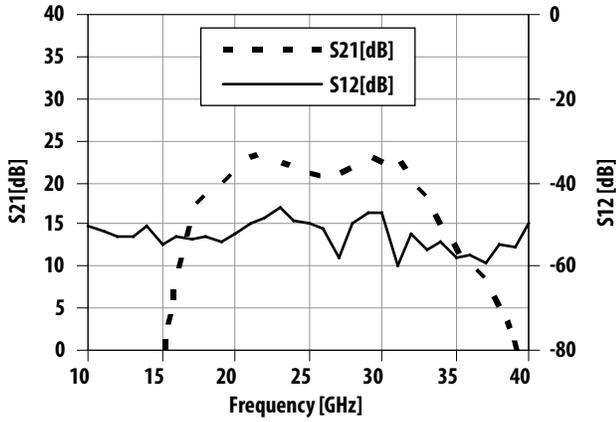


Figure 1. Gain and Reverse Isolation vs Frequency

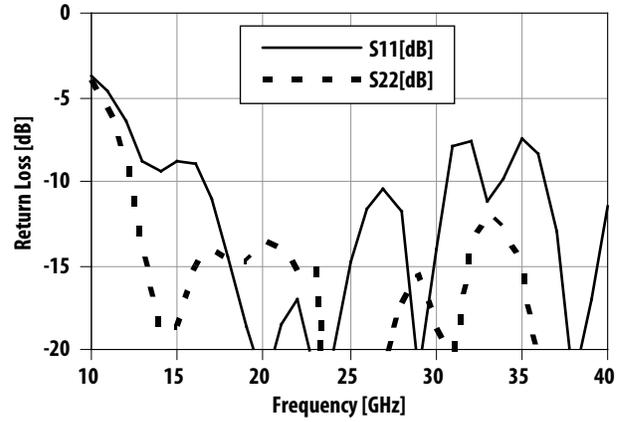


Figure 2. Return Loss vs Frequency

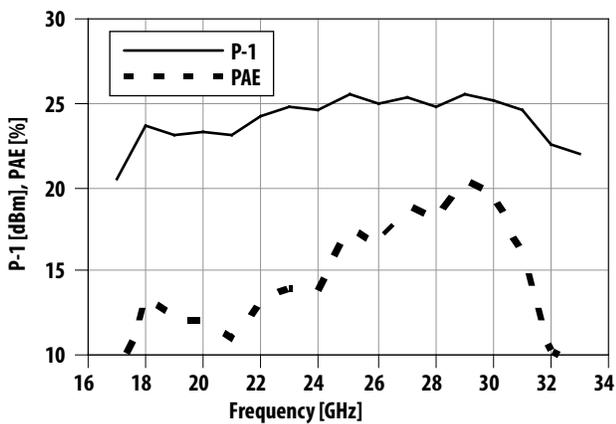


Figure 3. P-1dB and PAE vs Frequency

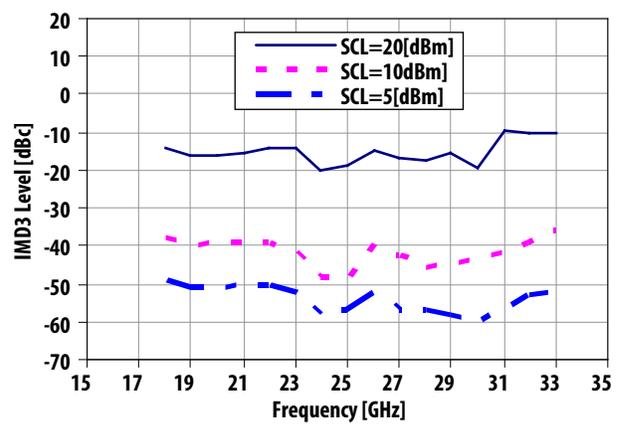


Figure 4. Typical IMD3 vs Frequency (SCL = Single Carrier level)

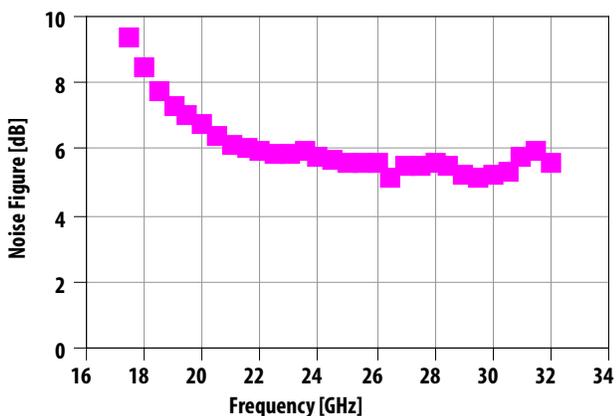


Figure 5. Typical Noise Figure vs Frequency

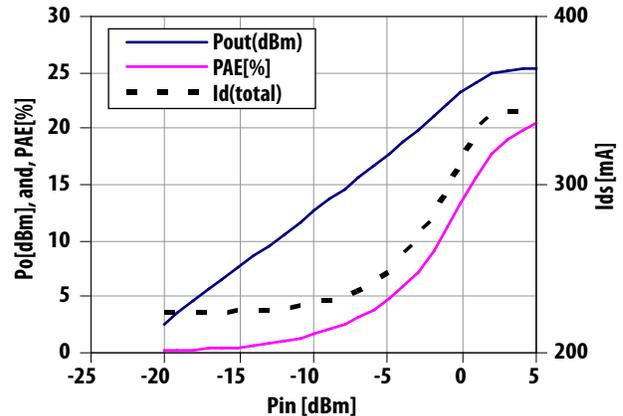


Figure 6. Output Power, PAE, and Drain Current vs Input Power at 30GHz

## Typical Performance (continued)

( $T_A = 25^\circ\text{C}$ ,  $Z_{in} = Z_{out} = 50 \Omega$ )

(Data obtained from a test fixture with 2.4 mm connectors. Effects of the test fixture – losses and mismatch – have not been removed from the data)

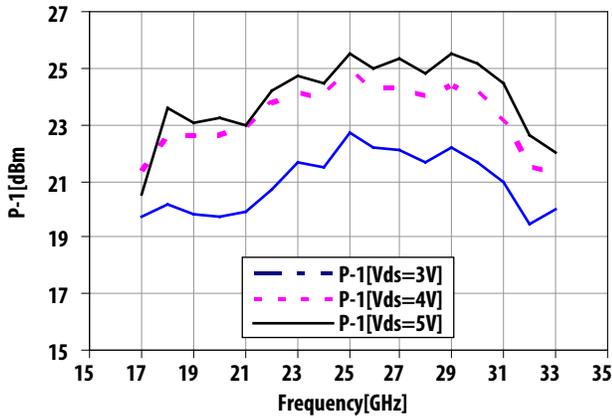


Figure 7. P-1dB vs Frequency and Vds, ( $I_{dQ}=230\text{mA}$ )

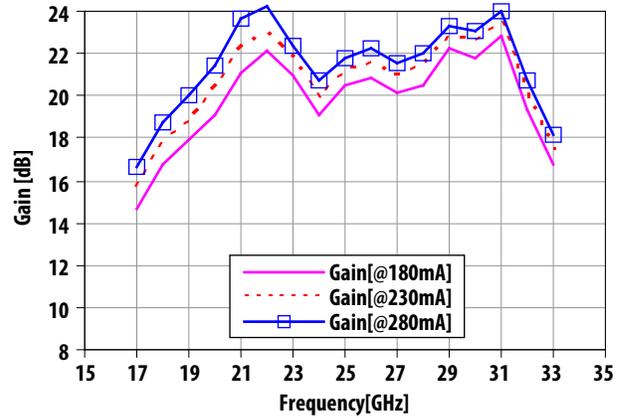


Figure 8. Small signal gain vs Frequency and  $I_{dQ}$ , ( $V_{ds}=5\text{V}$ )

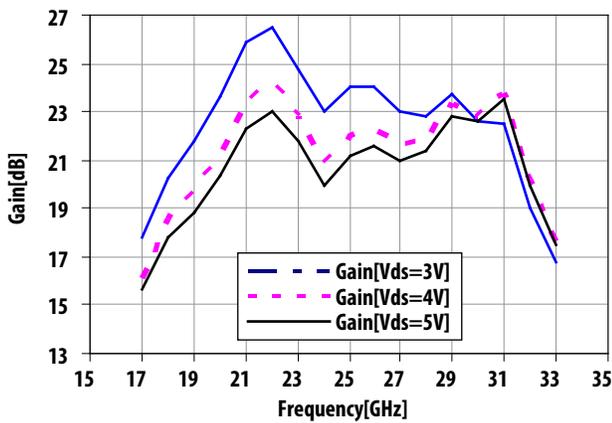


Figure 9. Small signal gain vs Frequency and Vds, ( $I_{dQ}=230\text{mA}$ )

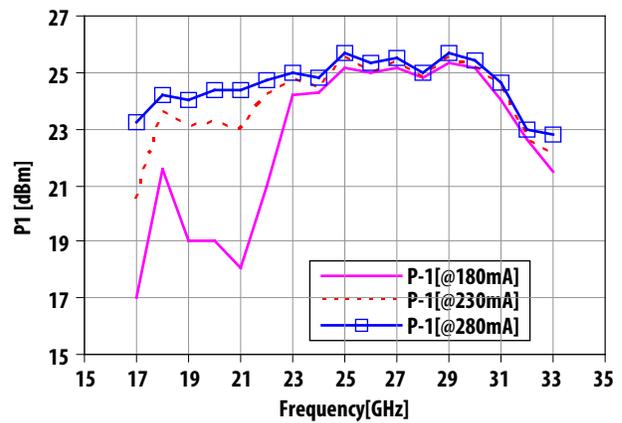


Figure 10. P-1dB vs Frequency and  $I_{dQ}$ , ( $V_{ds}=5\text{V}$ )

## Typical Performance (continued)

( $V_d = 5\text{ V}$ ,  $I_{dQ} = 230\text{ mA}$ ,  $Z_{in} = Z_{out} = 50\ \Omega$ )

(Data obtained from a test fixture with 2.4 mm connectors. Effects of the test fixture – losses and mismatch – have not been removed from the data)

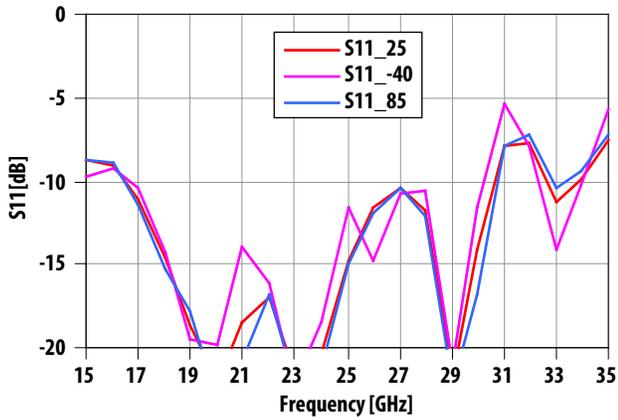


Figure 11.  $|S_{11}|$  vs Frequency and Temperature

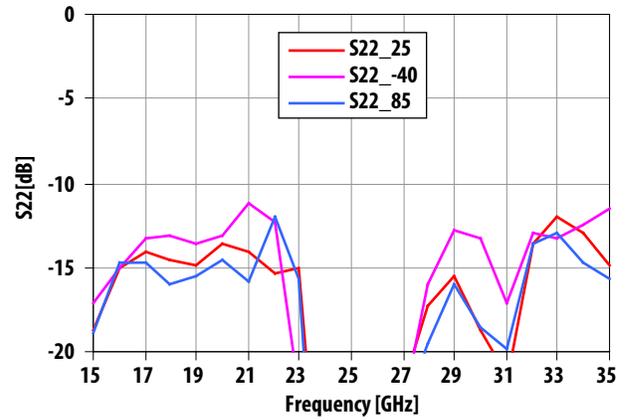


Figure 12.  $|S_{22}|$  vs Frequency and Temperature

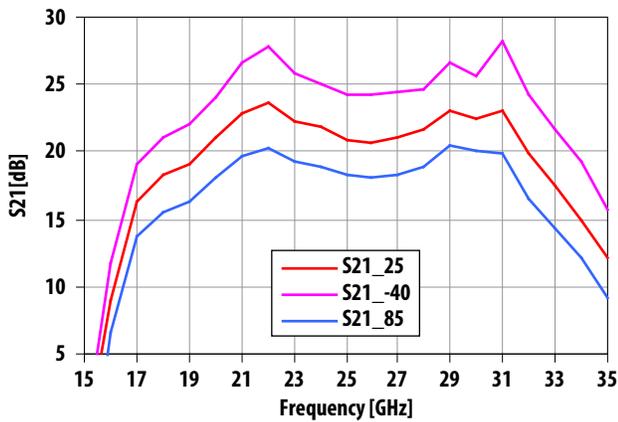


Figure 13.  $|S_{21}|$  vs Frequency and Temperature

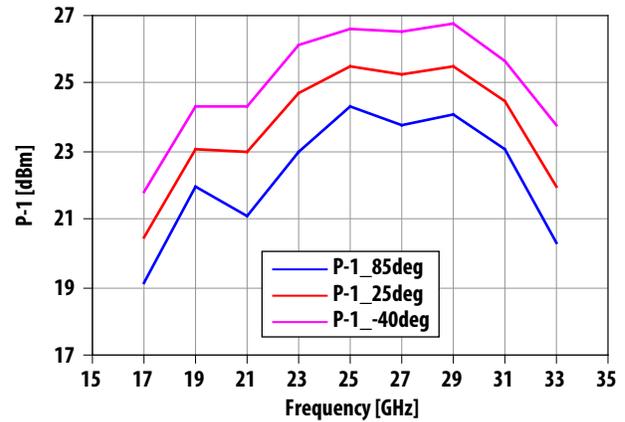


Figure 14.  $P_{-1dB}$  vs Frequency and Temperature

## Typical Scattering Parameters

( $T_A = 25^\circ\text{C}$ ,  $V_d = 5\text{ V}$ ,  $I_{dQ} = 230\text{ mA}$ ,  $Z_{in} = Z_{out} = 50\ \Omega$ )

(Data obtained from a test fixture with 2.4 mm connectors. Effects of the test fixture – losses and mismatch – have not been removed from the data)

Freq [GHz]	S11			S21			S12			S22		
	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
1	-0.09	0.99	-29.69	-61.68	8.24E-04	-156.52	-74.94	1.79E-04	93.45	-0.04	1.00	-30.54
2	-0.21	0.98	-58.75	-62.42	7.57E-04	131.13	-75.71	1.64E-04	-169.39	-0.19	0.98	-60.60
3	-0.40	0.96	-87.26	-51.00	2.82E-03	168.57	-68.11	3.93E-04	-95.11	-0.36	0.96	-89.53
4	-0.62	0.93	-114.69	-43.30	6.84E-03	88.68	-68.43	3.79E-04	-158.98	-0.62	0.93	-117.73
5	-0.93	0.90	-141.31	-40.16	9.82E-03	5.41	-65.79	5.14E-04	25.67	-1.03	0.89	-144.48
6	-1.29	0.86	-167.10	-41.68	8.24E-03	-78.42	-65.52	5.30E-04	-35.15	-1.37	0.85	-169.24
7	-1.73	0.82	167.76	-45.57	5.27E-03	-149.14	-66.93	4.50E-04	-154.44	-1.58	0.83	165.77
8	-2.25	0.77	143.07	-49.01	3.55E-03	158.06	-68.49	3.76E-04	143.83	-1.91	0.80	139.71
9	-2.87	0.72	118.59	-49.10	3.51E-03	107.41	-64.77	5.78E-04	116.44	-2.48	0.75	112.49
10	-3.63	0.66	94.19	-46.23	4.88E-03	48.79	-70.01	3.16E-04	68.82	-3.45	0.67	83.78
11	-4.55	0.59	69.78	-42.00	7.95E-03	-20.63	-63.93	6.36E-04	49.76	-5.09	0.56	53.17
12	-5.61	0.52	45.24	-39.79	1.02E-02	-101.95	-64.23	6.15E-04	52.98	-8.00	0.40	21.22
13	-6.85	0.45	20.08	-34.11	1.97E-02	78.11	-60.92	8.99E-04	-7.19	-13.27	0.22	-7.62
14	-8.29	0.39	-5.71	-16.16	1.56E-01	-23.46	-63.66	6.56E-04	-56.79	-23.00	0.07	-3.22
15	-10.01	0.32	-32.27	-2.65	7.37E-01	-108.03	-63.00	7.08E-04	-50.23	-19.86	0.10	48.72
16	-12.03	0.25	-59.72	9.44	2.96E+00	153.54	-60.55	9.39E-04	-89.59	-16.32	0.15	28.64
17	-14.03	0.20	-88.64	16.73	6.86E+00	31.01	-61.13	8.78E-04	-103.49	-16.43	0.15	0.70
18	-16.79	0.14	-122.72	18.66	8.57E+00	-75.10	-63.16	6.95E-04	-110.27	-17.77	0.13	-19.50
19	-20.86	0.09	-160.05	19.73	9.69E+00	-163.11	-64.91	5.68E-04	-112.32	-19.30	0.11	-39.48
20	-29.82	0.03	145.81	20.99	1.12E+01	117.11	-64.95	5.65E-04	-141.17	-21.19	0.09	-58.65
21	-27.11	0.04	-48.50	22.51	1.33E+01	38.03	-60.68	9.24E-04	-139.52	-22.45	0.08	-81.58
22	-19.78	0.10	-107.29	23.49	1.49E+01	-43.64	-59.37	1.07E-03	-162.33	-24.73	0.06	-111.04
23	-18.27	0.12	-155.02	23.19	1.44E+01	-124.10	-60.46	9.49E-04	149.72	-27.65	0.04	-154.00
24	-18.15	0.12	177.67	22.23	1.29E+01	162.96	-61.45	8.47E-04	158.39	-29.14	0.03	161.91
25	-17.83	0.13	159.39	21.42	1.18E+01	96.55	-58.32	1.21E-03	95.33	-30.75	0.03	123.21
26	-16.47	0.15	139.16	21.05	1.13E+01	33.27	-62.91	7.15E-04	105.45	-30.08	0.03	93.59
27	-14.72	0.18	120.37	21.38	1.17E+01	-29.45	-58.56	1.18E-03	69.65	-28.08	0.04	81.36
28	-13.05	0.22	97.21	22.12	1.28E+01	-95.77	-63.17	6.95E-04	45.47	-28.05	0.04	59.13
29	-11.74	0.26	70.76	22.92	1.40E+01	-166.44	-61.85	8.08E-04	20.46	-28.05	0.04	67.93
30	-11.13	0.28	41.32	23.41	1.48E+01	117.79	-65.00	5.62E-04	-6.17	-23.27	0.07	77.10
31	-11.49	0.27	8.10	23.15	1.44E+01	37.91	-74.82	1.82E-04	-44.79	-18.25	0.12	59.56
32	-14.37	0.19	-31.52	21.97	1.26E+01	-43.19	-61.48	8.43E-04	75.40	-15.66	0.16	34.68
33	-24.65	0.06	-78.94	19.86	9.84E+00	-123.15	-61.39	8.53E-04	53.33	-13.89	0.20	10.07
34	-21.69	0.08	83.55	17.10	7.16E+00	160.84	-64.51	5.95E-04	12.54	-12.87	0.23	-14.43
35	-14.26	0.19	51.47	14.30	5.19E+00	88.12	-65.86	5.10E-04	22.04	-12.62	0.23	-37.95
36	-11.08	0.28	25.84	11.55	3.78E+00	16.24	-62.41	7.58E-04	-15.61	-12.90	0.23	-61.34

## Biasing Considerations

The AMMP-6333 is a balanced amplifier consisting of two four stage single-ended amplifiers, two Lange couplers, a power monitoring detector, a reference detector for temperature compensation, and a current mirror for the gate biasing (Figure 15).

The recommended quiescent DC bias conditions for optimum gain, output power, efficiency, and reliability are:  $V_d = 5\text{ V}$  with  $V_g$  set for  $I_{dQ} = 230\text{ mA}$ . The drain bias voltage range is from 3 to 5 V. Drain current range is from 200 mA to 350 mA. The AMMC-6333 can be biased with a dual or single positive DC source (Figure 16).

The output power detection network provides a way to monitor output power. The differential voltage between the DET\_R and DET\_O outputs can be correlated with the RF power emerging from the RF output port. This voltage is given by:

$$V = (V_{\text{DET\_R}} - V_{\text{DET\_O}}) - V_{\text{OFFS}}$$

Where:

$V_{\text{DET\_R}}$  is the voltage at the DET\_R port

$V_{\text{DET\_O}}$  is a voltage at the DET\_O port

$V_{\text{OFFS}}$  is the offset voltage at zero input power

The offset voltage ( $V_{\text{OFFS}}$ ) can be at each power level by turning off the input power and measuring  $V$ . The error due to temperature drift should be less than 0.01dB/50°C. When  $V_{\text{OFFS}}$  is determined at a single reference temperature the drift error should be less than 0.25dB. Finally,  $V_{\text{OFFS}}$  be characterized over a range of temperatures and stored in a lookup table, or it can be measured at two temperatures and a linear fit used to calculate  $V_{\text{OFFS}}$  at any temperature.

The RF ports are AC coupled at the RF input to the first stage and the RF output of the final stage. No ground wires are needed since ground connections are made with plated through-holes to the backside of the device.

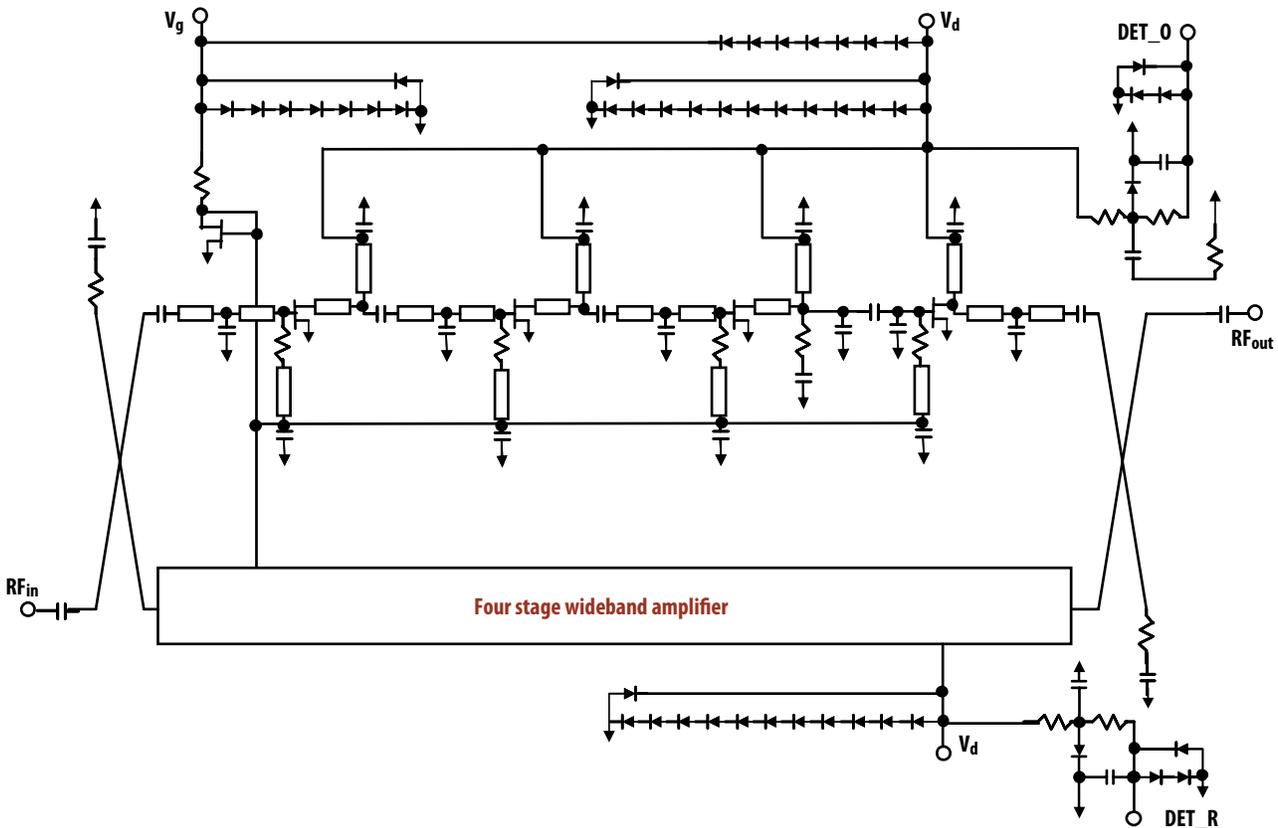
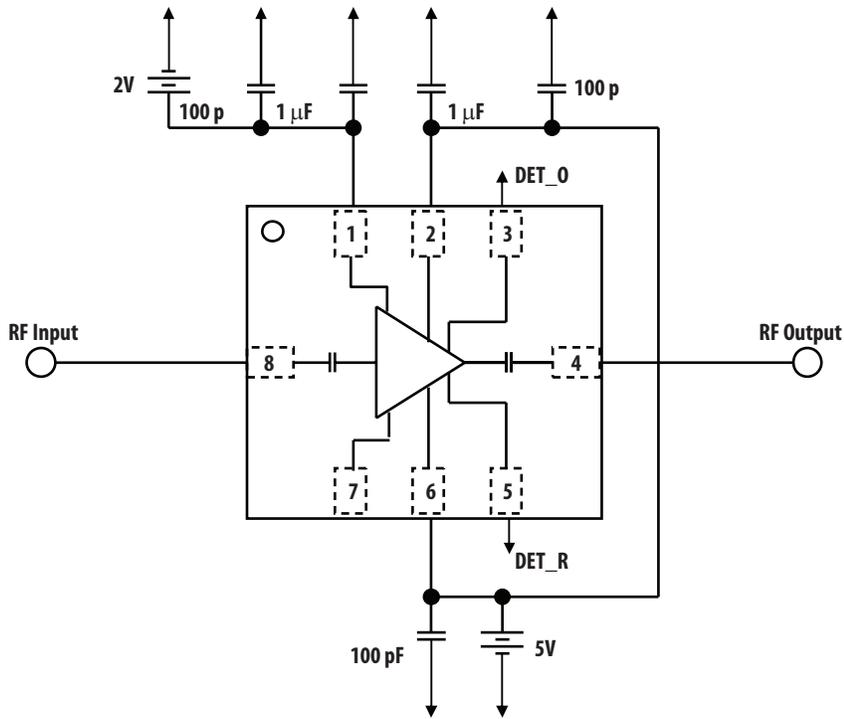
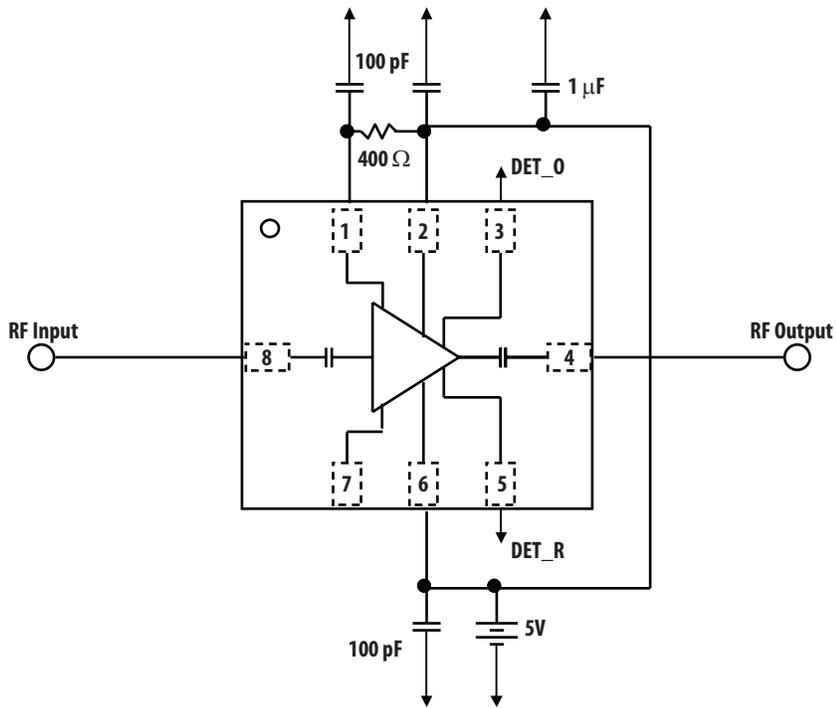


Figure 15. AMMC-6333 schematic



**1. Dual positive DC power supply**



**2. Single positive DC power supply**

Figure 16. AMMC-6333 biasing circuits. Both sides of the part must be biased.

## Recommended SMT Attachment

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in Figure 19, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available upon request from Avago Sales & Application Engineering.

## Manual Assembly

1. Follow ESD precautions while handling packages.
2. Handling should be be along the edges with tweezers.
3. Recommended attachment is conductive solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
4. Apply solder paste using a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance.
5. Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temperature to avoid damage due to thermal shock.
6. Packages have been qualified to withstand a peak temperature of 260°C for 20 seconds. Verify that the profile will not expose device beyond this limit.

## Solder Reflow Profile

A commonly used solder reflow method is accomplished in a belt furnace using convection heat. The suggested reflow profile Figure 17. This profile will vary among different solder pastes from different manufacturers and is shown here for reference only.

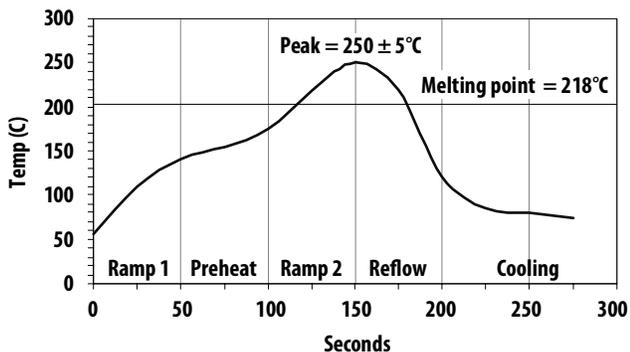
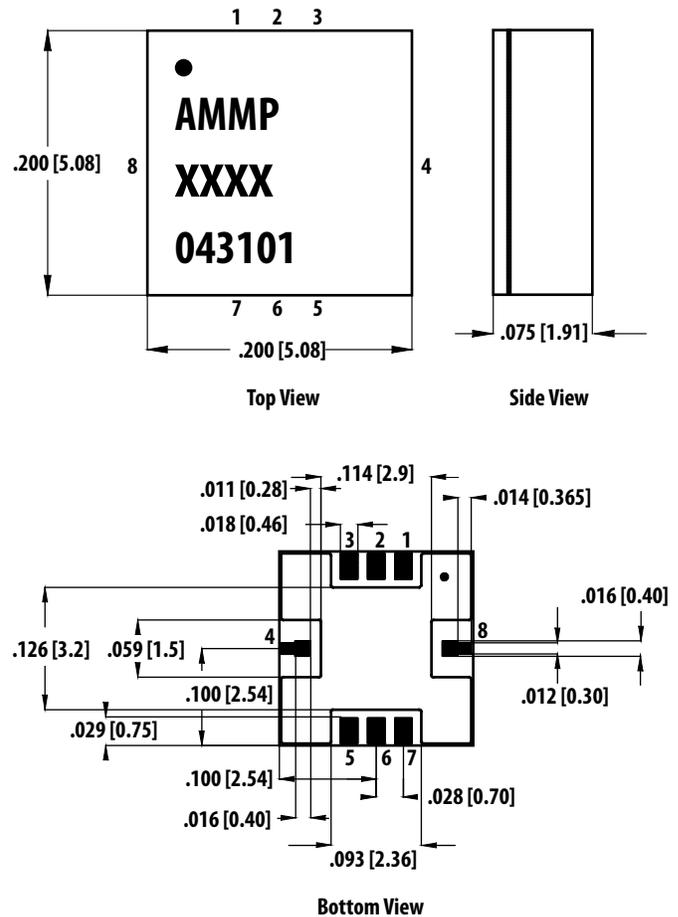


Figure 17. Suggested lead free reflow profile for SnAgCu Solder paste

## Package Outline Drawing



Dimensional Tolerances: 0.002" [0.05mm]

### Notes:

1. • Indicates Pin 1 (Backside of the Package)
2. Dimensions are in inches [millimeters]
3. All grounds must be soldered to PCB RF ground

## Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 18. The stencil has a solder paste deposition opening approximately 70% to 90% of the PCB pad. Reducing stencil opening can potentially generate more voids underneath.

On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads.

Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use a laser cut stencil composed of 0.127 mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

Recommended PCB Land Pattern for Rogers R04350 is shown in Figure 19.

The combined PCB and stencil layout is shown in Figure 20.

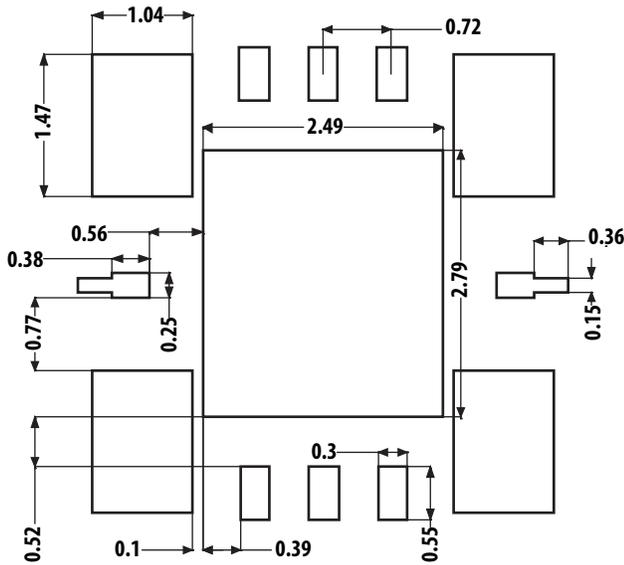


Figure 18. Stencil Outline Drawing (mm).

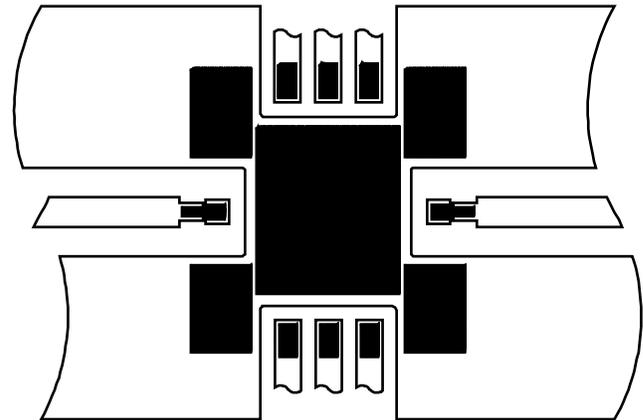


Figure 20. Combined PCB and Stencil Layouts

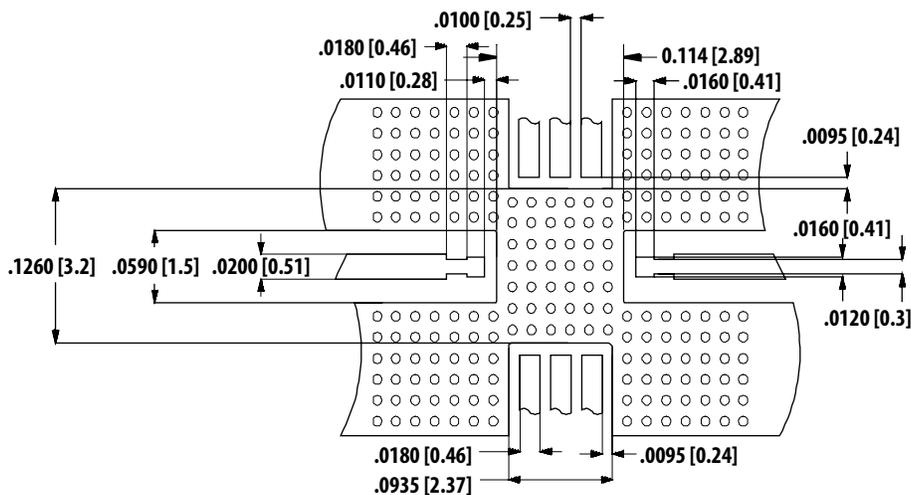
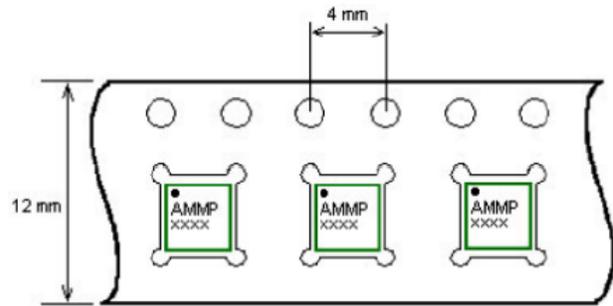


Figure 19. Recommended PCB Land Pattern for Rogers R04350, 0.010" thick. Dimensions are in inches [mm].

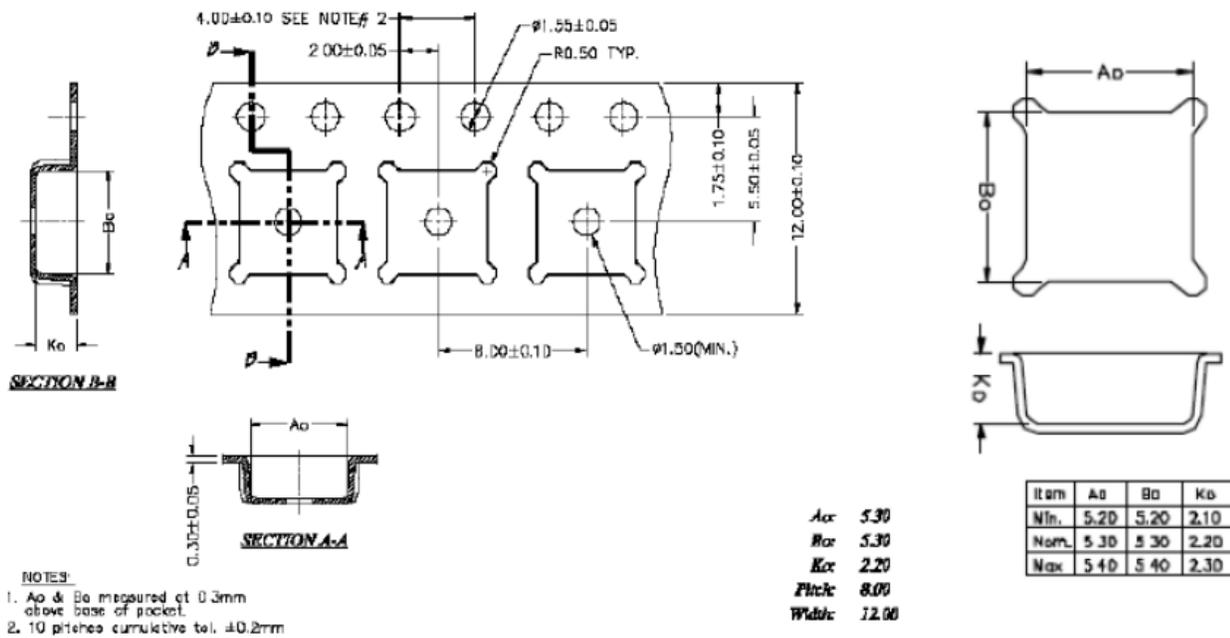
## Ordering Information

Part Number	Devices Per Container	Container
AMMP-6333-BLKG	10	Antistatic bag
AMMP-6333-TRG1	100	7" Reel
AMMP-6333-TRG2	500	7" Reel

## Device Orientation (Top View)



## Carrier Tape and Pocket Dimensions



For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)

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