16-BIT 250-KSPS SAMPLING CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **Standard ±10-V Input Range**
- **90-dB Min SNR with 20-kHz Input**
- **±2.0 LSB Max INL**
- **±1 LSB Max DNL, 16-Bits No Missing Code**
- **5-V Analog Supply, Flexible I/O Supply Voltage at 1.65 V to 5.25 V**
- **Pin-Compatible With ADS7805/10 (Low Speed), and 12-Bit ADS7804/8504**
- **Uses Internal or External Reference**
- **Full Parallel Data Output**
- **100-mW Typ Power Dissipation at 250 KSPS**
- **28-Pin SSOP Package**

APPLICATIONS

- **Industrial Process Control**
- **Data Acquisition Systems**
- **Digital Signal Processing**
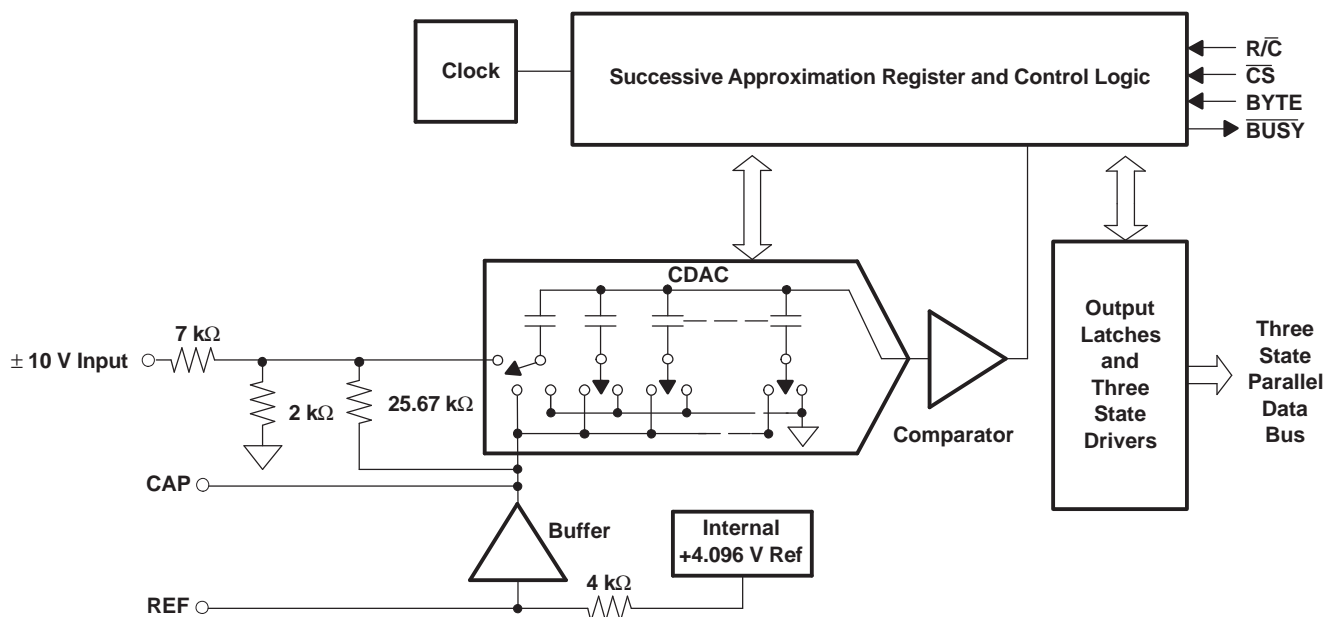- **Medical Equipment**
- **Instrumentation**

DESCRIPTION

The ADS8515 is a complete 16-bit sampling A/D converter using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and 3-state output drivers.

The ADS8515 is specified at a 250-kHz sampling rate over the full temperature range. Precision resistors provide an industry standard ±10-V input range, while the innovative design allows operation from a single +5-V supply, with power dissipation under 100 mW.

The ADS8515 is available in a 28-pin SSOP package and is fully specified for operation over the industrial -40°C to 85°C temperature range.

ADS8515

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MINIMUM INL (LSB)	NO MISSING CODE	MINIMUM SINAD (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8515IB	±2	16	89	-40°C to 85°C	SSOP-28	DB	ADS8515IBDB	Tube, 50
							ADS8515IBDBR	Tape and Reel, 2000
ADS8515I	±3	16	87	-40°C to 85°C	SSOP-28	DB	ADS8515IDB	Tube, 50
							ADS8515IDBR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)[2]

		ADS8515
Analog inputs	V_{IN}	±25V
	CAP	+V_{ANA} + 0.3 V to AGND2 - 0.3 V
	REF	Indefinite short to AGND2, momentary short to V_{ANA}
Ground voltage differences	DGND, AGND1, AGND2	±0.3 V
	V_{ANA}	6 V
	V_{DIG} to V_{ANA}	0.3 V
	V_{DIG}	6 V
Digital inputs		-0.3 V to +V_{DIG} + 0.3 V
Maximum junction temperature		165°C
Internal power dissipation		825 mW
Lead temperature (soldering, 10s)		300°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C, f_s = 250 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS8515I			ADS8515IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Resolution				16			16	Bits
ANALOG INPUT									
	Voltage range			±10			±10		V
	Impedance			8.885			8.885		kΩ
	Capacitance			75			75		pF
THROUGHPUT SPEED									
	Conversion cycle time	Acquire and convert			4			4	μs
	Throughput rate		250			250			kHz
DC ACCURACY									
INL	Integral linearity error		-3		3	-2		2	LSB[1]
DNL	Differential linearity error		-1		2	-1		1	LSB[1]
	No missing codes		16			16			Bits
	Transition noise[2]			0.67			0.67		LSB

(1) LSB means least significant bit. For the 16-bit, ±10-V input ADS8515, one LSB is 305 μV.
(2) Typical rms noise at worst case transitions and temperatures.

Product Folder Link(s): *ADS8515*

ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to 85°C, f_s = 250 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS8515I			ADS8515IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Full-scale error[3][4]	Int. Ref.	-0.5		0.5	-0.25		0.25	%FSR
	Full-scale error drift	Int. Ref.		±7			±7		ppm/°C
	Full-scale error[3][4]	Ext. 4.096-V Ref.	-0.25		0.25	-0.1		0.1	%FSR
	Full-scale error drift	Ext. 4.096-V Ref.		±2			±2		ppm/°C
	Bipolar zero error[3]		-4		4	-2		2	mV
	Bipolar zero error drift			±2			±2		ppm/°C
	Power supply sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75 V < V_D < +5.25 V	-8		8	-8		8	LSB
AC ACCURACY									
SFDR	Spurious-free dynamic range	f_I = 20 kHz	95	102		97	102		dB[5]
THD	Total harmonic distortion	f_I = 20 kHz		-100	-94		-100	-96	dB
SINAD	Signal-to-(noise+distortion)	f_I = 20 kHz	87	91		89	91		dB
		−60-dB Input		30			32		dB
SNR	Signal-to-noise ratio	f_I = 20 kHz	88	92		90	92		dB
	Full-power bandwidth[6]			500			500		kHz
SAMPLING DYNAMICS									
	Aperture delay			5			5		ns
	Transient response	FS Step			2			2	μs
	Overvoltage recovery[7]			150			150		ns
REFERENCE									
	Internal reference voltage		4.076	4.096	4.116	4.076	4.096	4.116	V
	Internal reference source current (must use external buffer)			1			1		μA
	Internal reference drift			8			8		ppm/°C
	External reference voltage range for specified linearity		3.9	4.096	4.2	3.9	4.096	4.2	V
	External reference current drain	Ext. 4.096-V Ref.			100			100	μA
DIGITAL INPUTS									
	Logic levels								
V_{IL}	Low-level input voltage	V_{DIG} = 1.65 V − 5.25 V	-0.3		0.8	-0.3		0.35*V_{DIG}	V
V_{IH}	High-level input voltage	V_{DIG} = 1.65 V − 5.25 V	0.65*V_{DIG}		V_{DIG}+0.3 V	0.65*V_{DIG}		V_{DIG}+0.3 V	V
I_{IL}	Low-level input current	V_{IL} = 0 V			±10			±10	μA
I_{IH}	High-level input current	V_{IH} = 5 V			±10			±10	μA
DIGITAL OUTPUTS									
	Data format (Parallel 16-bits)								
	Data coding (Binary 2's complement)								
V_{OL}	Low-level output voltage	I_{SINK} = 1.6 mA			0.4			0.4	V
V_{OH}	High-level output voltage	I_{SOURCE} = 500 μA	0.8×V_{DIG}			0.8×V_{DIG}			V
	Leakage current	Hi-Z state, V_{OUT} = 0 V to V_{DIG}			±5			±5	μA
	Output capacitance	Hi-Z state			15			15	pF
DIGITAL TIMING									
	Bus access timing				83			83	ns
	Bus relinquish timing				83			83	ns
POWER SUPPLIES									

(3) As measured with fixed resistors shown in Figure 22. Adjustable to zero with external potentiometer.
(4) Full-scale error is the worst case of -full-scale or +full-scale deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.
(5) All specifications in dB are referred to a full-scale ±10-V input.
(6) Full-power bandwidth is defined as the full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB, or 10 bits of accuracy.
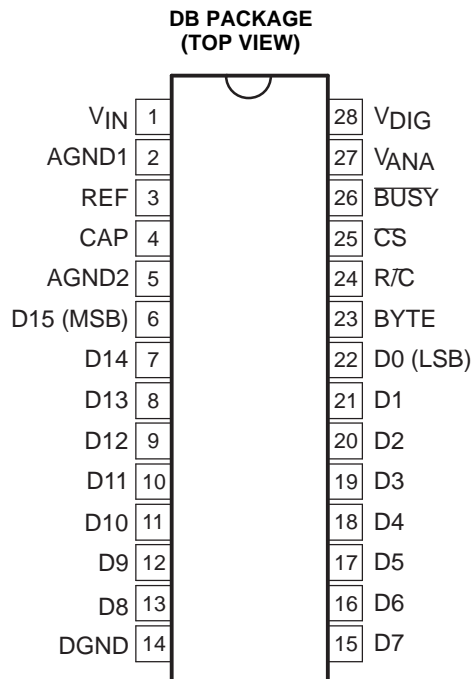(7) Recovers to specified performance after 2 x FS input overvoltage.

ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to 85°C, f_s = 250 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS8515I			ADS8515IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{DIG}	Digital input voltage	Must be ≤ V_{ANA}	1.65		5.25	1.65		5.25	V
V_{ANA}	Analog input voltage		4.75	5	5.25	4.75	5	5.25	V
I_{DIG}	Digital input current			0.1	1		0.1	1	mA
I_{ANA}	Analog input current			20	25		20	25	mA
	Power dissipation	f_S = 250 kHz		100	125		100	125	mW
TEMPERATURE RANGE									
	Specified performance		-40		85	-40		85	°C
	Derated performance[8]		-55		125	-55		125	°C
	Storage		-65		150	-65		150	°C
THERMAL RESISTANCE (Θ_{JA})									
	SSOP			67			67		°C/W

(8) The internal reference may not be started correctly beyond the industrial temperature range (-40°C to 85°C), therefore use of an external reference is recommended.

DEVICE INFORMATION

DB PACKAGE
(TOP VIEW)

Left Pin	No.		No.	Right Pin
V_{IN}	1		28	V_{DIG}
AGND1	2		27	V_{ANA}
REF	3		26	$\overline{BUSY}$
CAP	4		25	$\overline{CS}$
AGND2	5		24	R/$\overline{C}$
D15 (MSB)	6		23	BYTE
D14	7		22	D0 (LSB)
D13	8		21	D1
D12	9		20	D2
D11	10		19	D3
D10	11		18	D4
D9	12		17	D5
D8	13		16	D6
DGND	14		15	D7

Terminal Functions

TERMINAL		DIGITAL I/O	DESCRIPTION
NAME	SSOP NO.		
AGND1	2		Analog ground. Used internally as ground reference point.
AGND2	5		Analog ground.
$\overline{BUSY}$	26	O	At the start of a conversion, $\overline{BUSY}$ goes low and stays low until the conversion is completed and the digital outputs have been updated.
BYTE	23	I	Selects 8 most significant bits (low) or 8 least significant bits (high).
CAP	4		Reference buffer capacitor. 2.2-µF tantalum capacitor to ground.
$\overline{CS}$	25	I	Internally ORed with R/$\overline{C}$. If R/$\overline{C}$ low, a falling edge on $\overline{CS}$ initiates a new conversion.
DGND	14		Digital ground.
D15 (MSB)	6	O	Data bit 15. Most significant bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D14	7	O	Data bit 14. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D13	8	O	Data bit 13. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D12	9	O	Data bit 12. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D11	10	O	Data bit 11. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D10	11	O	Data bit 10. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D9	12	O	Data bit 9. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D8	13	O	Data bit 8. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D7	15	O	Data bit 7. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D6	16	O	Data bit 6. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D5	17	O	Data bit 5. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D4	18	O	Data bit 4. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D3	19	O	Data bit 3. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D2	20	O	Data bit 2. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D1	21	O	Data bit 1. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.

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Product Folder Link(s): ADS8515

Terminal Functions (continued)

D0 (LSB)	22	O	Data bit 0. Least significant bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
R/$\overline{C}$	24	I	With $\overline{CS}$ low and $\overline{BUSY}$ high, a falling edge on R/$\overline{C}$ initiates a new conversion. With $\overline{CS}$ low, a rising edge on R/$\overline{C}$ enables the parallel output.
REF	3		Reference input/output. 2.2-µF tantalum capacitor to ground.
V_{ANA}	27		Analog supply input. Nominally +5 V. Decouple to ground with 0.1-µF ceramic and 10-µF tantalum capacitors.
V_{DIG}	28		Digital supply input. Nominally +5 V. Connect directly to pin 27. Must be ≤ V_{ANA}.
V_{IN}	1		Analog input. See Figure 24

TYPICAL CHARACTERISTICS
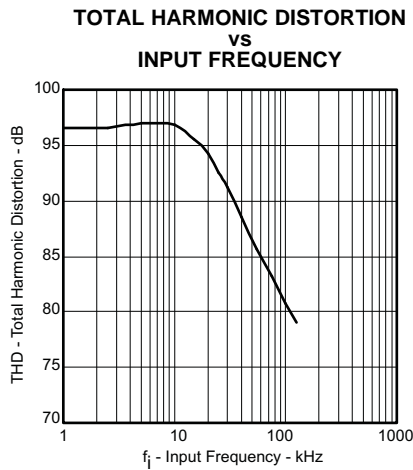
**TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY**

Figure 1.

**SIGNAL-TO-NOISE RATIO
vs
INPUT FREQUENCY**

Figure 2.

**SIGNAL-TO-NOISE AND DISTORTION
vs
INPUT FREQUENCY**

Figure 3.

**SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY**

Figure 4.

**SIGNAL-TO-NOISE RATIO
vs
FREE-AIR TEMPERATURE**

Figure 5.

**SIGNAL-TO-NOISE AND DISTORTION
vs
FREE-AIR TEMPERATURE**

Figure 6.

Product Folder Link(s): *ADS8515*
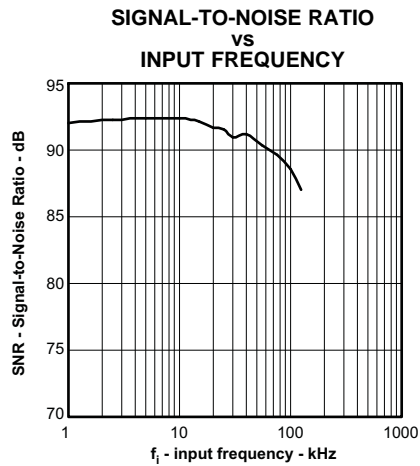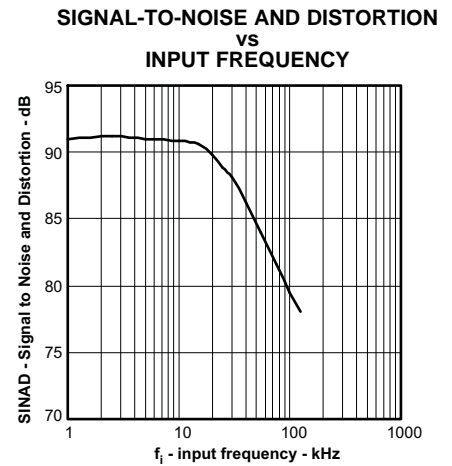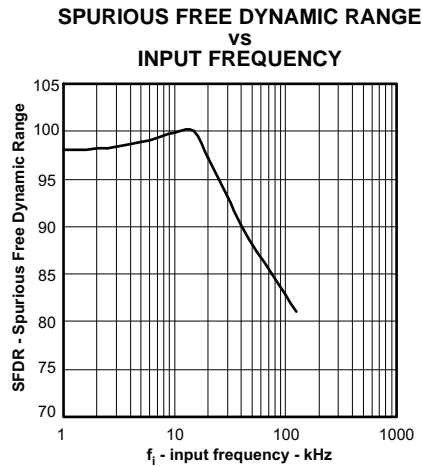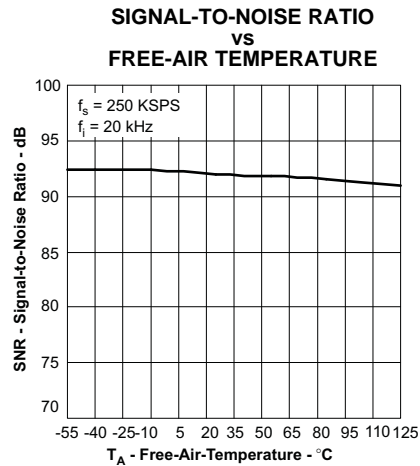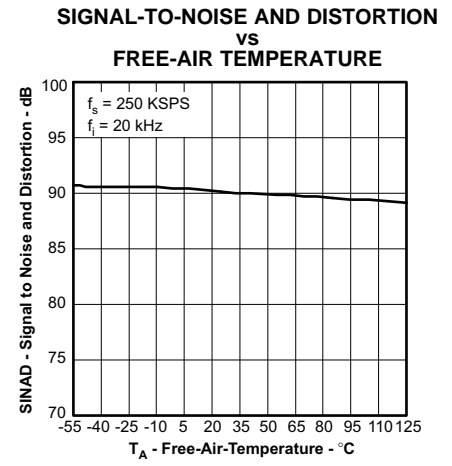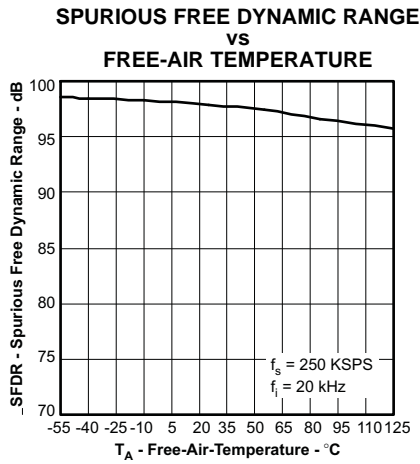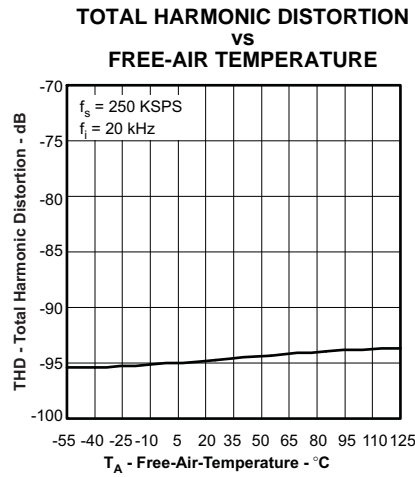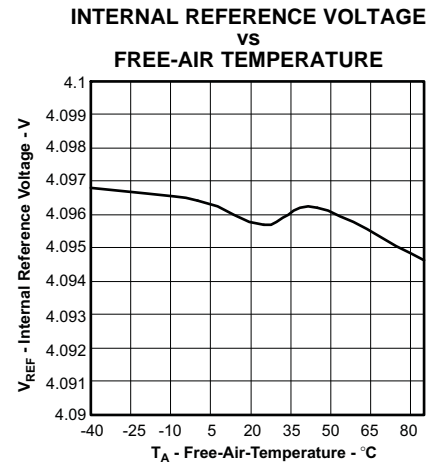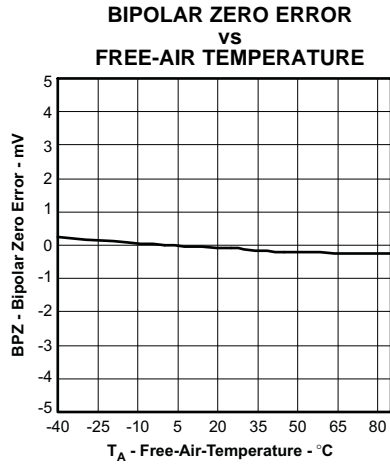
TYPICAL CHARACTERISTICS (continued)
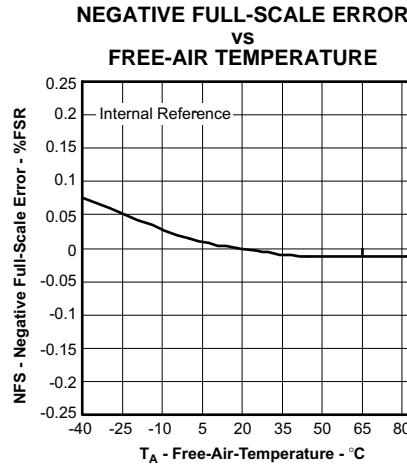

Figure 7.

Figure 8.

Figure 9.

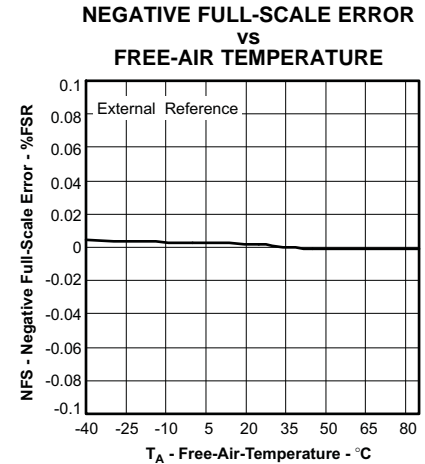Figure 10.

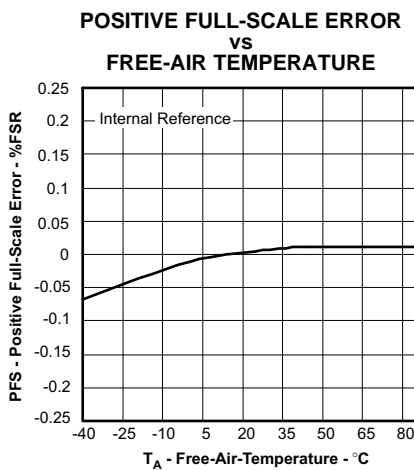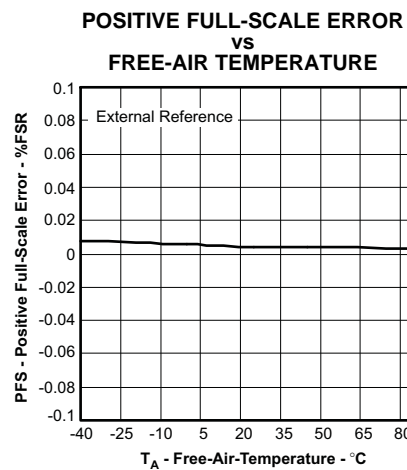
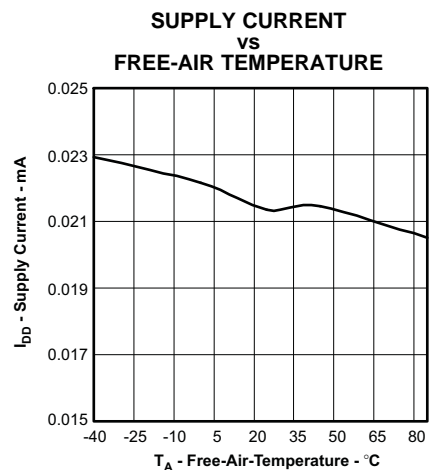Figure 11.

Figure 12.

Figure 13.

Figure 14.

Figure 15.

TYPICAL CHARACTERISTICS (continued)
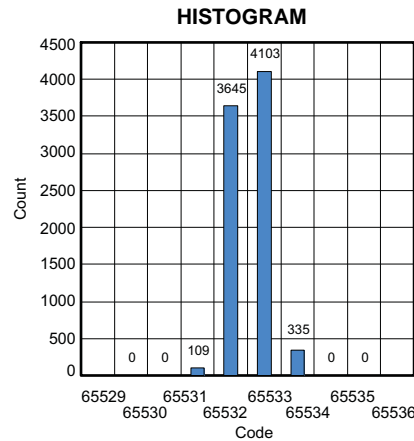
Figure 16.
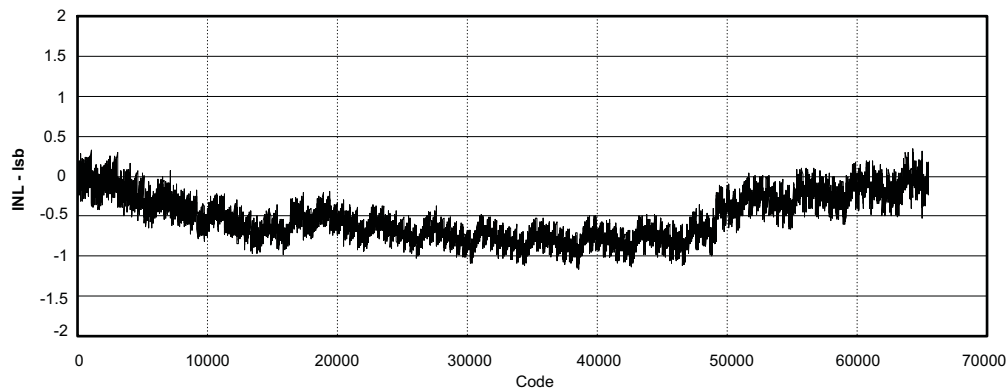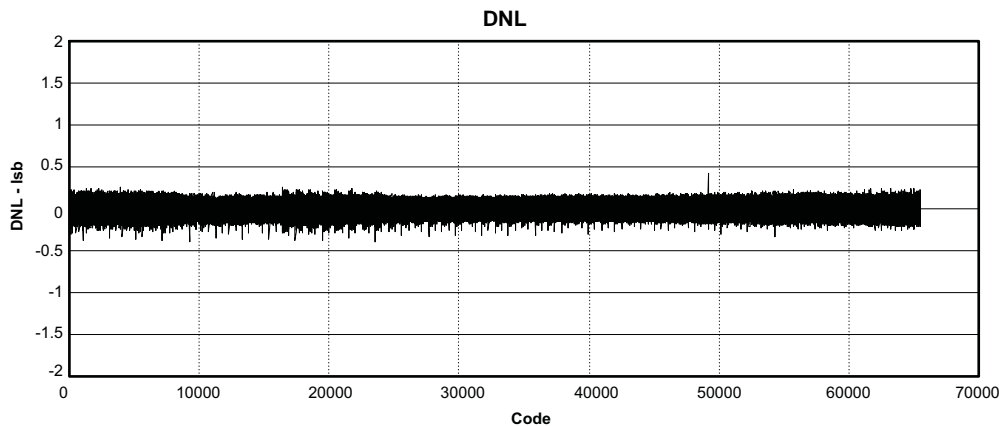
Figure 17.

Figure 18.

BASIC OPERATION

Figure 19 shows a basic circuit to operate the ADS8515 with a full parallel data output. Taking R/$\overline{\text{C}}$ (pin 24) low for a minimum of 40 ns initiates a conversion. $\overline{\text{BUSY}}$ (pin 26) goes low and stays low until the conversion is completed and the output registers are updated. Data is output in binary 2's complement with the MSB on pin 6. $\overline{\text{BUSY}}$ going high can be used to latch the data.

Product Folder Link(s): *ADS8515*

The ADS8515 begins tracking the input signal at the end of the conversion. Allowing 4 μs between convert commands assures accurate acquisition of a new signal.

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 25) and R/$\overline{C}$ (pin 24) low for a minimum of 40 ns immediately puts the sample/hold of the ADS8515 in the hold state and starts conversion n. $\overline{BUSY}$ (pin 26) goes low and stays low until conversion n is completed and the internal output register has been updated.

The ADS8515 begins tracking the input signal at the end of the conversion. Allowing 4 μs between convert commands assures accurate acquisition of a new signal. Refer to Table 1 for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figure 21, Figure 22, and Figure 23 for the timing diagrams.

$\overline{CS}$ and R/$\overline{C}$ are internally ORed and level triggered. There is not a requirement which input goes low first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion n, be sure the less critical input is low at least 10 ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied low using R/$\overline{C}$ to control the read and convert modes. The parallel output becomes active whenever R/$\overline{C}$ goes high. Refer to the Reading Data section.

Table 1. Control Line Functions for Read and Convert

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion n. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion n. Databus enters Hi-Z state.
0	1	↑	Conversion n completed. Valid data from conversion n on the databus.
↓	1	1	Enables databus with valid data from conversion n.
↓	1	0	Enables databus with valid data from conversion -1[1]. Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion -1[1]. Conversion n in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data is invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be high when $\overline{BUSY}$ goes high.
X	X	0	Conversion n in progress.

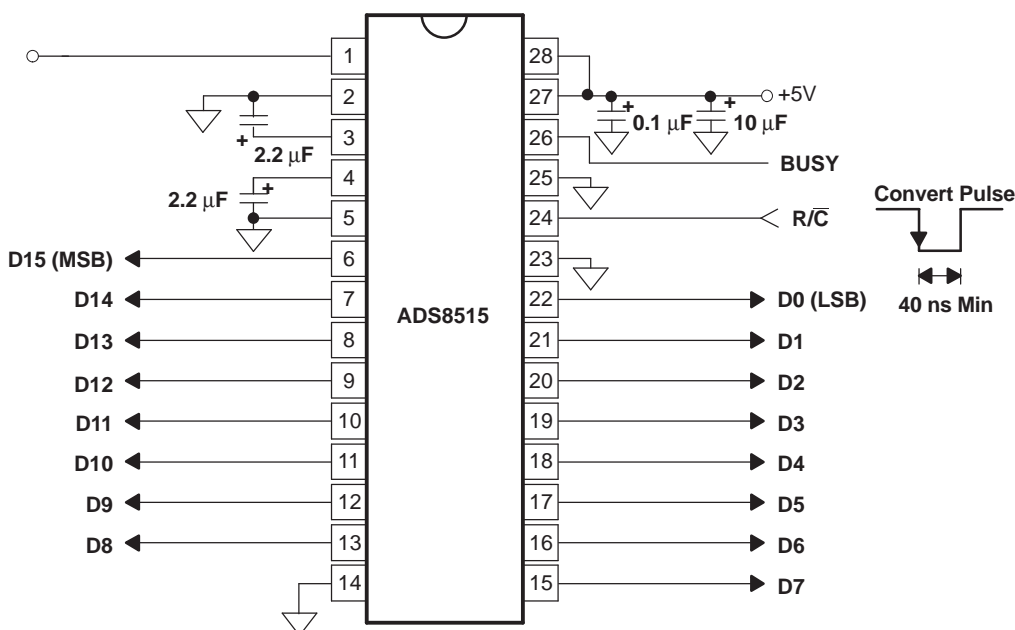(1)   See Figure 21 and Figure 22 for constraints on data valid from conversion n-1.

Figure 19. Basic Operation

Product Folder Link(s): ADS8515

READING DATA

The ADS8515 outputs full or byte-reading parallel data in binary 2's complement data output format. The parallel output is active when R/$\overline{\text{C}}$ (pin 24) is high and $\overline{\text{CS}}$ (pin 25) is low. Any other combination of $\overline{\text{CS}}$ and R/$\overline{\text{C}}$ 3-states the parallel output. Valid conversion data can be read in a full parallel, 16-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table 2 for ideal output codes and Figure 20 for bit locations relative to the state of BYTE.

Table 2. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY 2's COMPLEMENT	
		BINARY CODE	HEX CODE
Full-scale range	±10 V		
Least significant bit (LSB)	305 µV		
Full scale (10 V-1 LSB)	9.999695 V	0111 1111 1111 1111	7FFF
Midscale	0 V	0000 0000 0000 0000	0000
One LSB below midscale	-305 µV	1111 1111 1111 1111	FFFF
-Full scale	-10 V	1000 0000 0000 0000	8000

PARALLEL OUTPUT (After a Conversion)

After conversion *n* is completed and the output registers have been updated, $\overline{\text{BUSY}}$ (pin 26) goes high. Valid data from conversion *n* is available on D15-D0 (pins 6-13 and 15-22). $\overline{\text{BUSY}}$ going high can be used to latch the data. Refer to Table 3 and Figure 21, Figure 22, and Figure 23 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion *n* has been initiated, valid data from conversion −1 can be read and is valid up to t_2 after the start of conversion *n*. Do not attempt to read data from t_2 after the start of conversion *n* until $\overline{\text{BUSY}}$ (pin 26) goes high; this may result in reading invalid data. Refer to Table 3 and Figure 21, Figure 22, and Figure 23 for timing specifications.

Note: For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tying $\overline{\text{CS}}$ low while using the falling edge of R/$\overline{\text{C}}$ to initiate conversions and the rising edge of R/$\overline{\text{C}}$ to activate the output mode of the converter. See Figure 21.

Table 3. Conversion Timing

| SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{w1}	Pulse duration, convert	40			ns
t_a	Access time, data valid after R/$\overline{\text{C}}$ low		0.8	1.2	µs
t_{pd}	Propagation delay time, $\overline{\text{BUSY}}$ from R/$\overline{\text{C}}$ low		6	20	ns
t_{w2}	Pulse duration, $\overline{\text{BUSY}}$ low			2	µs
t_{d1}	Delay time, $\overline{\text{BUSY}}$ after end of conversion		5		ns
t_{d2}	Delay time, aperture		5		ns
t_{conv}	Conversion time			2	µs
t_{acq}	Acquisition time	2			µs
t_{dis}	Disable time, bus	10	15	83	ns
t_{d3}	Delay time, $\overline{\text{BUSY}}$ after data valid	35	50		ns
t_v	Valid time, previous data remains valid after R/$\overline{\text{C}}$ low	1.5	2		µs
$t_{conv} + t_{acq}$	Throughput time			4	µs
t_{su}	Setup time, R/$\overline{\text{C}}$ to $\overline{\text{CS}}$	10			ns
t_c	Cycle time between conversions	4			µs
t_{en}	Enable time, bus	10	15	30	ns
t_{d4}	Delay time, BYTE	10	15	30	ns

Product Folder Link(s): *ADS8515*
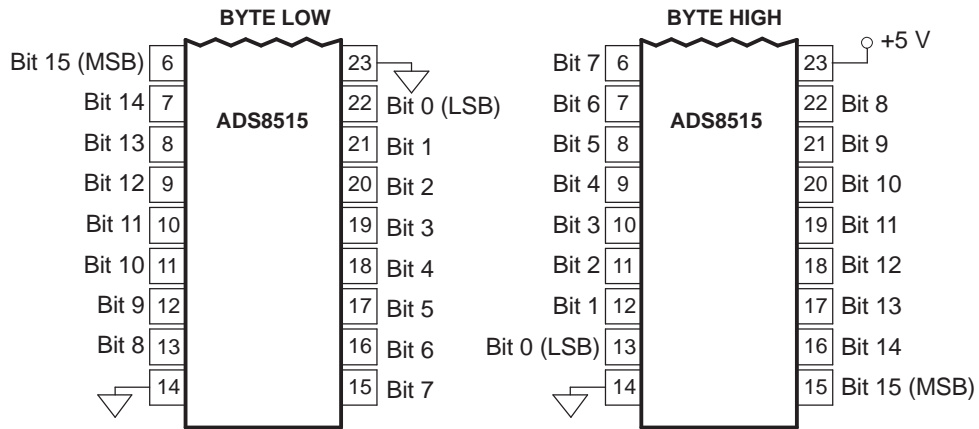
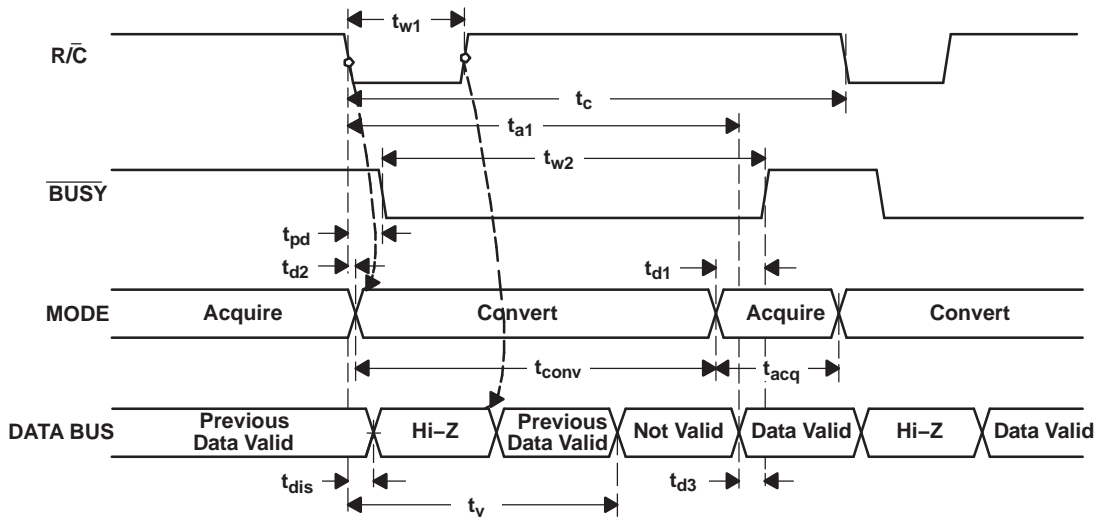**Figure 20. Bit Locations Relative to State of BYTE (Pin 23)**

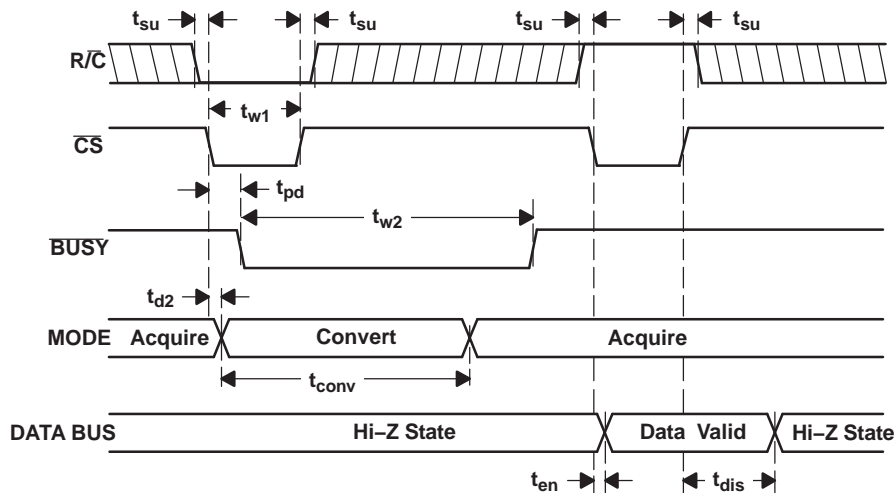**Figure 21. Conversion Timing with Outputs Enabled after Conversion ($\overline{\text{CS}}$ Tied Low)**

Figure 22. Using $\overline{\text{CS}}$ to Control Conversion and Read Timing

Submit Documentation Feedback
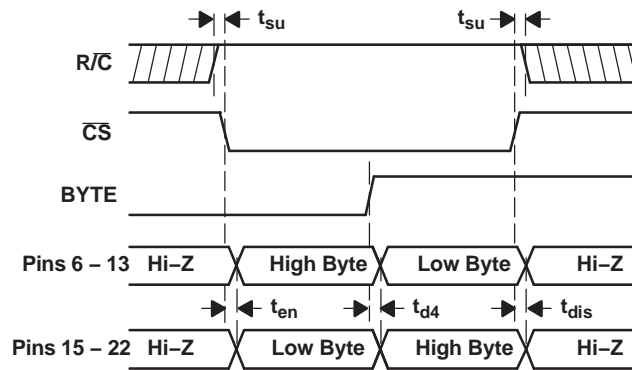
Product Folder Link(s): *ADS8515*

Figure 23. Using $\overline{\text{CS}}$ and BYTE to Control Data Bus

ADC RESET

The ADC reset function of the ADS8515 can be used to terminate the current conversion cycle. Bringing R/$\overline{\text{C}}$ low for at least 40 ns while BUSY is low will initiate the ADC reset. To initiate a new conversion, R/$\overline{\text{C}}$ must return to the high state and remain high long enough to acquire a new sample (see Table 3, t_c) before going low to initiate the next conversion sequence. In applications that do not monitor the BUSY signal, it is recommended that the ADC reset function be implemented as part of a system initialization sequence.

INPUT RANGES

The ADS8515 offers a standard ±10-V input range. Figure 24 shows the necessary circuit connections for the ADS8515 with and without hardware trim. Offset and full-scale error specifications are tested and specified with the fixed resistors shown in Figure 25(b). Full-scale error includes offset and gain errors measured at both +FS and -FS. Adjustments for offset and gain are described in the Calibration section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain are corrected in software (refer to the Calibration section).

The nominal input impedance of 6.35 kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet. The input resistor divider network provides inherent overvoltage protection assured to at least ±25 V. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

The input signal must be referenced to AGND1. This minimizes the ground loop problem typical to analog designs. The analog signal should be driven by a low impedance source. A typical driving circuit using an OPA627 or OPA132 is shown in Figure 24.
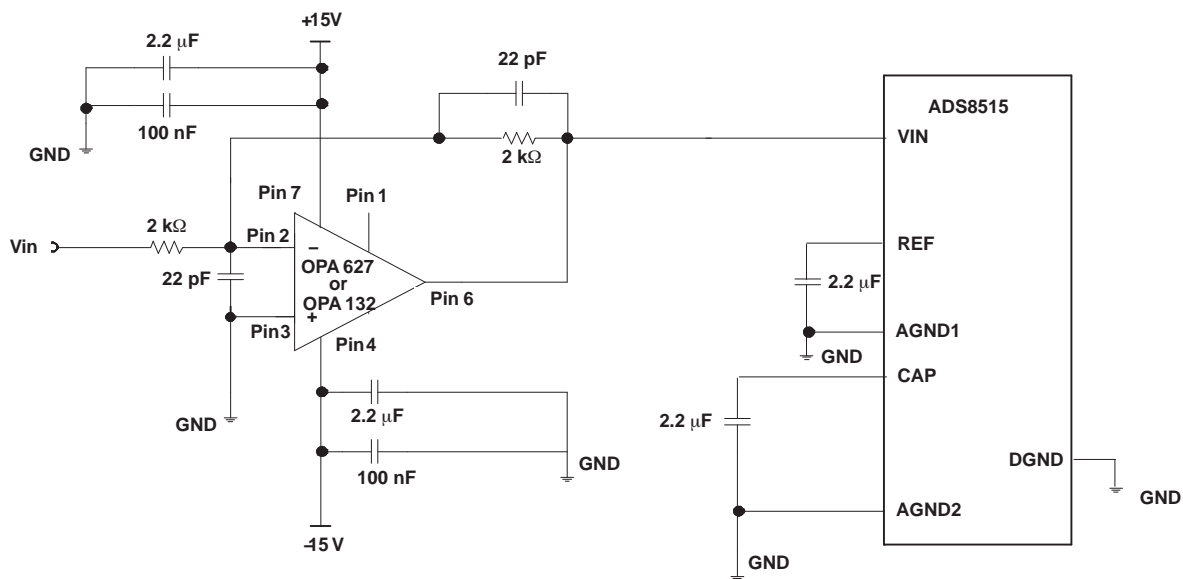
Product Folder Link(s): *ADS8515*

Figure 24. Typical Driving Circuit (±10 V, No Trim)

APPLICATION INFORMATION

CALIBRATION

The gain of the ADS8515 can be trimmed in software. To achieve optimum performance, several iterations may be required.

Hardware Calibration

To calibrate the gain of the ADS8515, install the resistors and potentiometer as shown in Figure 25(a). The calibration range is approximately ±100 mV.

Software Calibration

The offset and gain of the ADS8515 is calibrated with software. See Figure 25(b) for the circuit connections.

(a) ±10 V With Hardware Trim

(b) ±10 V Without Hardware Trim
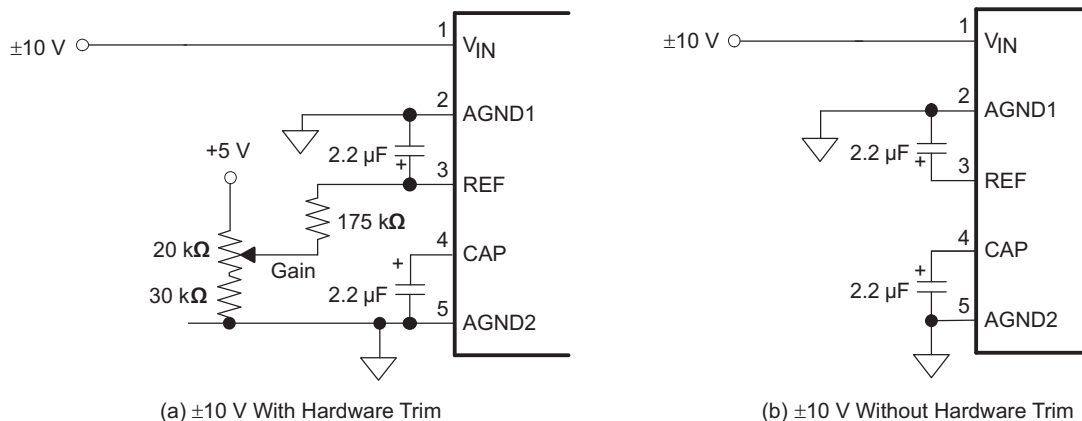
Note: Use 1% metal film resistors.

Figure 25. Circuit Diagram For Software Trim

REFERENCE

The ADS8515 can operate with its internal 4.096-V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full-scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 4.096-V reference. A 2.2-µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low-pass filter to bandlimit noise on the reference. Using a smaller value capacitor introduces more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external ac or dc loads.

The range for the external reference is 3.9 V to 4.2 V and determines the actual LSB size. Increasing the reference voltage increases the full-scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2-µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1 µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2 µF have little affect on improving performance. The ESR (equivalent series resistance) of these compensation capacitors is also critical. Keep the total ESR under 3 Ω. See *Typical Characteristics* section for how the worst case ILE is affected by ESR.

The output of the buffer is capable of driving up to 2 mA of current to a dc load, but any external load from the CAP pin may degrade the linearity of the ADS8515. Using an external buffer allows the internal reference to be used for larger dc loads and ac loads. Do not attempt to directly drive an ac load with the output voltage on CAP. This causes performance degradation of the converter. The ESR (equivalent series resistance) of these compensation capacitors is also critical. Keep the total ESR under 3 Ω. See the TYPICAL CHARACTERISTICS section concerning how ESR affects performance.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5-V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS8515 uses 90% of its power for the analog circuitry. The ADS8515 should be considered as an analog component.

The +5-V power for the A/D should be separate from the +5 V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5-V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12-V or +15-V supplies are present, a simple +5-V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5-V source.

GROUNDING

Three ground pins are present on the ADS8515. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the *system* ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS8515, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op amp sufficient for the signal in an application is sufficient to drive the ADS8515.

The resistive front end of the ADS8515 also provides an assured ±25-V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS8515 does have 3-state outputs for the parallel port, but intermediate latches should be used if the bus is to be active during conversions. If the bus is not active during conversion, the 3-state outputs can be used to isolate the A/D from other peripherals on the same bus. The 3-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS8515 has an internal LSB size of 38 μV. Transients from fast switching signals on the parallel port, even when the A/D is 3-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

Revision History

Changes from Original (June 2007) to Revision A   **Page**

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS8515IBDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8515IBDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8515IDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8515IDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8515IDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8515IDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

Reel Diameter

Reel Width (W1)

K0 — P1

B0 | W

Cavity — A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1	Q2
Q3	Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8515IBDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
ADS8515IDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8515IBDBR	SSOP	DB	28	2000	346.0	346.0	33.0
ADS8515IDBR	SSOP	DB	28	2000	346.0	346.0	33.0

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0,15.
         D.   Falls within JEDEC MO-150

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