Industrial, 14kSPS, 24-Bit Analog-to-Digital Converter with Low-Drift Reference

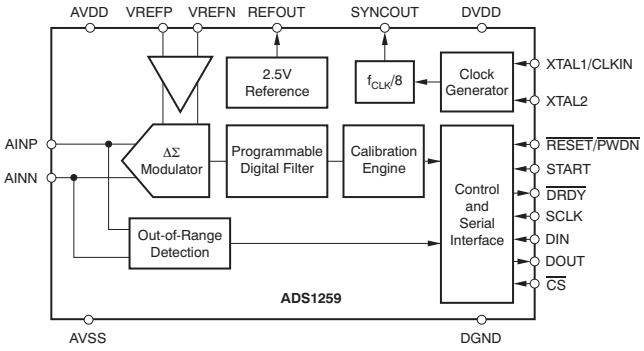
Check for Samples: ADS1259

FEATURES

- **24 Bits, No Missing Codes**
- **Output Data Rates From 10 To 14kSPS**
- **High Performance:**
  - **INL: 0.4ppm**
  - **Reference Drift: 2ppm/°C**
  - **Gain Drift: 0.5ppm/°C**
  - **Offset Drift: 0.05μV/°C**
  - **Noise: 0.7μV_{RMS} at 60SPS**
- **Simultaneous 50/60Hz Rejection at 10SPS**
- **Single-Cycle Settling**
- **Internal Oscillator**
- **Out-of-Range Detection**
- **Readback Data Integrity by Checksum and Redundant Data Read Capability**
- **SPI™-Compatible Interface**
- **Analog Supply: +5V or ±2.5V**
- **Digital Supply: +2.7V to +5V**
- **Low Power: 13mW**

APPLICATIONS

- **Industrial Process Control**
- **Scientific Instrumentation**
- **Test and Measurement**



DESCRIPTION

The ADS1259 is a high-linearity, low-drift, 24-bit, analog-to-digital converter (ADC) designed for the needs of industrial process control, precision instrumentation, and other exacting applications. Combined with a signal amplifier (such as the PGA280), a high-resolution, high-accuracy measurement system is formed that is capable of digitizing a wide range of signals.

The converter uses a fourth-order, inherently stable, delta-sigma (ΔΣ) modulator that provides outstanding noise and linearity performance. The data rates are programmable up to 14kSPS including 10SPS, 50SPS, and 60SPS that provide excellent normal mode line-cycle rejection. The digital filter can be programmed for a fast settling mode where the conversions settle in a single cycle, or programmed for a high line-cycle rejection mode. A fast responding input over-range detector flags the conversion data if an input over-range should occur.

The ADS1259 also provides an integrated low-noise, very low drift 2.5V reference. The on-chip oscillator, an external crystal, or an external clock can by used as the ADC clock source.

Data and control communication are handled over a 4MHz, SPI-compatible interface capable of operating with a minimum of three wires. Data integrity is augmented by data bytes checksum and redundant data read capability. Conversions are synchronized either by command or by pin.

Dissipating only 13mW in operation, the ADS1259 can be powered down, dissipating less than 25μW. The ADS1259 is offered in a TSSOP-20 package and is fully specified from –40°C to +105°C.

RELATED PRODUCTS

FEATURES	PRODUCT
24-bit ADC with integrated PGA	ADS1256
Wide-range PGA	PGA280
High-precision PGA; G = 1, 10, 100, 1000	PGA204

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	ADS1259		
	MIN	MAX	UNIT
AVDD to AVSS	–0.3	+5.5	V
AVSS to DGND	–2.8	+0.3	V
DVDD to DGND	–0.3	+5.5	V
Input current, momentary	–100	+100	mA
Input current, continuous	–10	+10	mA
Analog input voltage to DGND	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage to DGND	–0.3	DVDD + 0.3	V
Maximum junction temperature		+150	°C
Operating temperature range	–40	+125	°C
Storage temperature range	–60	+150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

Minimum/maximum specifications are at T_A = –40°C to +105°C. Typical specifications are at T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = +3.3V, f_{CLK} = 7.3728MHz, V_{REF} = 2.5V, and f_{DATA} = 60SPS, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1259			ADS1259B			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUTS								
Full-scale input voltage range (FSR)	V_{IN} = (AINP – AINN)		±V_{REF}			±V_{REF}		V
Absolute input voltage (AINP, AINN to DGND)		AVSS – 0.1		AVDD + 0.1	AVSS – 0.1		AVDD + 0.1	V
Differential input impedance			120			120		kΩ
Common-mode input impedance			500			500		kΩ
SYSTEM PERFORMANCE								
Resolution	No missing codes	24			24			Bits
Data rate (f_{DATA})		10		14400	10		14400	SPS(1)
Integral nonlinearity	Best fit method		±0.0003	±0.001		**±0.00004**	**±0.0003**	%FSR
Offset error			±40	±250		±40	±250	µV
Offset error after calibration(2)			±1			±1		µV
Offset drift(3)	T_A = –40°C to +105°C		0.05	0.25		0.05	0.25	µV/°C
Gain error(4)			±0.05	±0.5		±0.05	±0.5	%
Gain error after calibration(2)			±0.0002			±0.0002		%
Gain drift(3)	T_A = –40°C to +105°C		0.5	2.5		0.5	2.5	ppm/°C
Normal mode rejection	See Figure 40							
Common-mode rejection	60Hz, ac(5)	100	120		100	120		dB
Noise	See Table 1		0.7			0.7		µV
AVDD, AVSS power-supply rejection	60Hz, ac(5)	85	95		85	95		dB
DVDD power-supply rejection	60Hz, ac(5)	85	110		85	110		dB
OUT-OF-RANGE DETECTION								
Threshold(6)	Level		±105			±105		%FSR
	Accuracy		±0.5			±0.5		%FSR
VOLTAGE REFERENCE INPUTS								
Reference input range (V_{REF})	V_{REF} = (VREFP – VREFN)	0.5	2.5	AVDD – AVSS + 200mV	0.5	2.5	AVDD – AVSS + 200mV	V
Negative reference absolute input (VREFN to DGND)		AVSS – 100mV		VREFP – 0.5	AVSS – 100mV		VREFP – 0.5	V
Positive reference absolute input (VREFP to DGND)		VREFN + 0.5		AVDD + 100mV	VREFN + 0.5		AVDD + 100mV	V
Average reference input current(7)			200nA + 60nA/V			200nA + 60nA/V		
Average reference input current drift	Internal or external clock		0.2			0.2		nA/°C
INTERNAL VOLTAGE REFERENCE								
Reference output voltage	V_{REFOUT} = (REFOUT – AVSS)		2.5			2.5		V
Accuracy	T_A = +25°C			±0.1			±0.1	%
Temperature drift(3)	T_A = –40°C to +105°C		10	50		**4**	**12**	ppm/°C
	T_A = 0°C to +85°C					**2**	**5**	ppm/°C
Drive current sink and source		–10		10	–10		10	mA(8)
Load regulation			10			10		µV/mA
Turn-on settling time(9)	±0.001% settling		1			1		s

(1) SPS = samples per second.
(2) Calibration accuracy is on the level of noise (signal and ADC), reduced by the effect of 16 reading averaging.
(3) Reference drift specified by design and final production test. Drift calculated over the specified temperature range using box method.
(4) Excludes internal reference error.
(5) f_{DATA} = 14.4kSPS. Placing a notch of the digital filter at 60Hz (setting f_{DATA} = 10SPS or 60SPS) further improves the common-mode rejection and power-supply rejection of this input frequency.
(6) Absolute input voltage range for out-of-range specification: AVSS + 150mV ≤ AINP or AINN ≤ AVDD – 150mV valid.
(7) Over the range: AVSS ≤ VREFP or VREFN ≤ AVDD. For reference voltage exceeding AVDD or AVSS, input current = 150nA/10mV.
(8) Limit the reference output current to ±10mA.
(9) C_{REFOUT} = 1µF, C_{REFIN} = 1µF.

ELECTRICAL CHARACTERISTICS (continued)

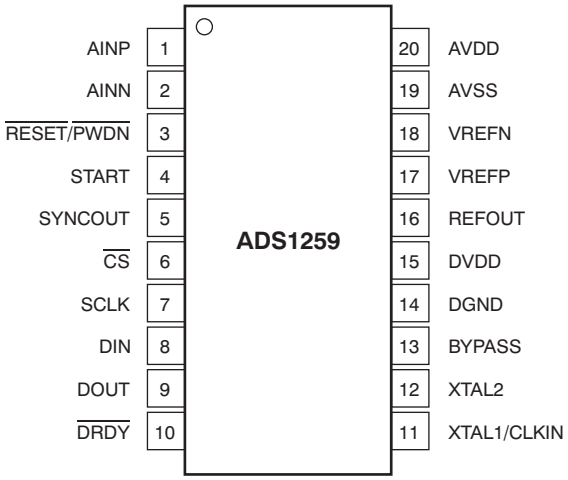
Minimum/maximum specifications are at T_A = –40°C to +105°C. Typical specifications are at T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = +3.3V, f_{CLK} = 7.3728MHz, V_{REF} = 2.5V, and f_{DATA} = 60SPS, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1259			ADS1259B			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
CLOCK SOURCE (f_{CLK})								
Internal oscillator	Nominal frequency		7.3728			7.3728		MHz
	Accuracy		±0.2	±2		±0.2	±2	%
Crystal oscillator	Frequency range	2	7.3728	8	2	7.3728	8	MHz
	Start-up time(10)		20			20		ms
External clock	Frequency range	0.1	7.3728	8	0.1	7.3728	8	MHz
	Duty cycle	40		60	40		60	%
DIGITAL INPUT/OUTPUT (DVDD = 2.7V to 5.25V)								
V_{IH}		0.8 DVDD		DVDD	0.8 DVDD		DVDD	V
V_{IL}		DGND		0.2 DVDD	DGND		0.2 DVDD	V
V_{OH}	I_{OH} = 1mA	0.8 DVDD			0.8 DVDD			V
	I_{OH} = 8mA		0.75 DVDD			0.75 DVDD		V
V_{OL}	I_{OL} = 1mA			0.2 DVDD			0.2 DVDD	V
	I_{OL} = 8mA		0.2 DVDD			0.2 DVDD		V
Input hysteresis			0.1			0.1		V
Input leakage	0 < $V_{DIGITAL\ INPUT}$ < DVDD			±10			±10	µA
POWER SUPPLY								
AVSS		–2.6		0	–2.6		0	V
AVDD		AVSS + 4.75		AVSS + 5.25	AVSS + 4.75		AVSS + 5.25	V
DVDD		2.7		5.25	2.7		5.25	V
AVDD, AVSS current	Operating (reference enabled)		2.3	3.8		2.3	3.8	|mA|
	Sleep mode (reference enabled)		200			200		|µA|
	Sleep mode (reference disabled)		1	40		1	40	|µA|
	Power-Down mode		1	40		1	40	|µA|
DVDD current(11)	Operating		500	700		500	700	µA
	Sleep mode		160	300		160	300	µA
	Power-Down mode(12)		1	10		1	10	µA
Power dissipation	Operating		13	22		13	22	mW
	Sleep mode (reference enabled)		1.5			1.5		mW
	Sleep mode (reference disabled)		0.5	1.2		0.5	1.2	mW
	Power-Down mode		10	240		10	240	µW
TEMPERATURE RANGE								
Specified temperature range		–40		+105	–40		+105	°C
Operating temperature range		–40		+125	–40		+125	°C
Storage temperature range		–60		+150	–60		+150	°C

(10) Crystal operation using 18pF load capacitors.
(11) Specified with internal oscillator operating (internal oscillator current: 40µA, typ).
(12) External CLKIN, SCLK stopped. Digital inputs maintained at V_{IH} or V_{IL} voltage levels.

PIN CONFIGURATION

PW PACKAGE
TSSOP-20
(TOP VIEW)



ADS1259 Terminal Functions

PIN NAME	PIN #	FUNCTION	DESCRIPTION
AINP	1	Analog input	Positive analog input
AINN	2	Analog input	Negative analog input
$\overline{\text{RESET}}/\overline{\text{PWDN}}$	3	Digital input	Reset/Power-Down; reset is active low; hold low for power-down
START	4	Digital input	Start conversions, active high
SYNCOUT	5	Digital output	Sync clock output ($f_{CLK}/8$)
$\overline{\text{CS}}$	6	Digital input	SPI chip-select, active low
SCLK	7	Digital input	SPI clock input
DIN	8	Digital input	SPI data input
DOUT	9	Digital output	SPI data output
$\overline{\text{DRDY}}$	10	Digital output	Data ready output, active low
XTAL1/CLKIN	11	Digital input	Internal oscillator: DGND External clock: clock input Crystal oscillator: external crystal1
XTAL2	12	Digital	External crystal2, otherwise no connection
BYPASS	13	Analog	Core voltage bypass
DGND	14	Digital	Digital ground
DVDD	15	Digital	Digital power supply
REFOUT	16	Analog output	Positive reference output
VREFP	17	Analog input	Positive reference input
VREFN	18	Analog input	Negative reference input
AVSS	19	Analog	Negative analog power supply and negative reference output
AVDD	20	Analog	Positive analog power supply

SPI TIMING CHARACTERISTICS

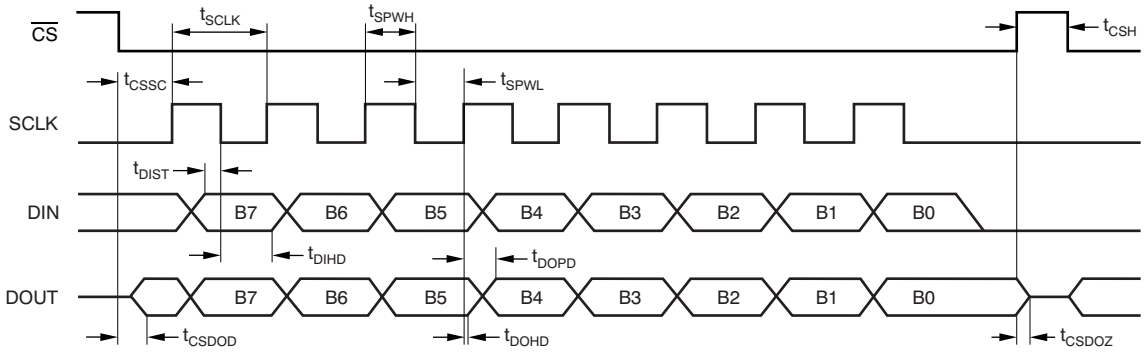


Figure 1. Serial Interface Timing

TIMING REQUIREMENTS: SERIAL INTERFACE TIMING

At T_A = –40°C to +105°C and DVDD = 2.7V to 5.25V, unless otherwise noted.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{CSSC}	$\overline{CS}$ low to first SCLK: setup time(1)	50		ns
t_{SCLK}	SCLK period	1.8		t_{CLK} (2)
t_{SPWH}	SCLK pulse width: high	90		ns
t_{SPWL}	SCLK pulse width: low(3)	90		ns
			2^{16}	t_{CLK}
t_{DIST}	Valid DIN to SCLK falling edge: setup time	35		ns
t_{DIHD}	Valid DIN to SCLK falling edge: hold time	20		ns
t_{DOPD}	SCLK rising edge to valid new DOUT: propagation delay(4)		60	ns
t_{DOHD}	SCLK rising edge to DOUT invalid: hold time	0		ns
t_{CSDOD}	$\overline{CS}$ low to DOUT driven: propagation delay(4)	0	40	ns
t_{CSDOZ}	$\overline{CS}$ high to DOUT Hi-Z: propagation delay		20	ns
t_{CSH}	$\overline{CS}$ high pulse	20		t_{CLK}

(1) $\overline{CS}$ can be tied low.
(2) $t_{CLK} = 1/f_{CLK}$.
(3) Holding SCLK low longer than $2^{16} \times t_{CLK}$ cycles resets the SPI interface (enabled by SPI register bit).
(4) DOUT load = 20pF || 100kΩ to DGND.

TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = 3.3V, V_{REF} = 2.5V, VREFN = AVSS, f_{CLK} = 7.3728MHz, and f_{DATA} = 60SPS, unless otherwise noted.

NOISE DISTRIBUTION HISTOGRAM

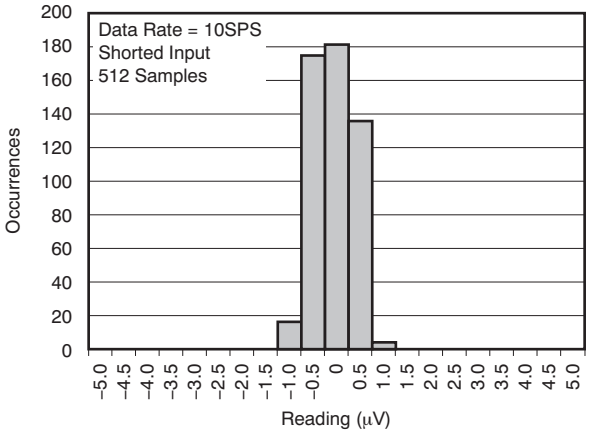


Figure 2.

NOISE DISTRIBUTION HISTOGRAM

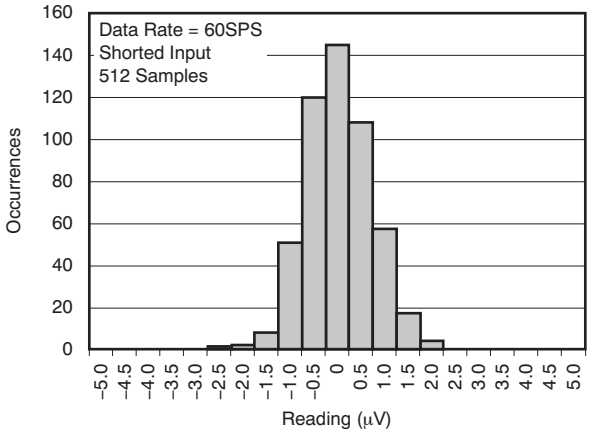


Figure 3.

NOISE DISTRIBUTION HISTOGRAM

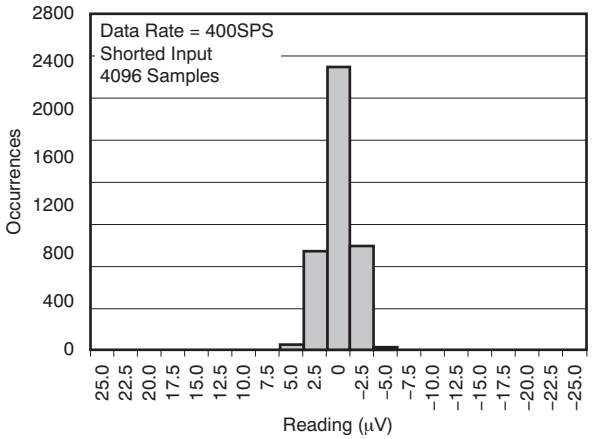


Figure 4.

NOISE DISTRIBUTION HISTOGRAM

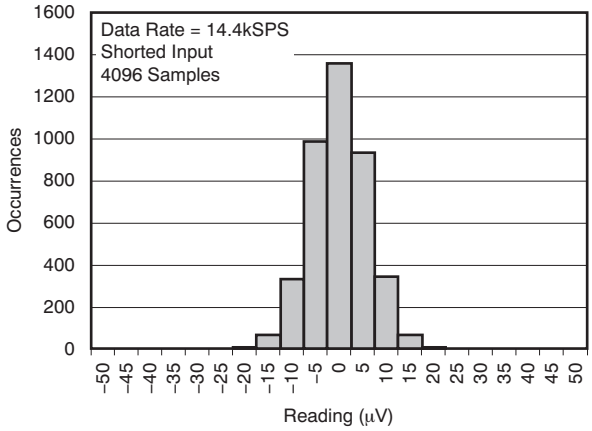


Figure 5.

EFFECTIVE NUMBER OF BITS vs TEMPERATURE

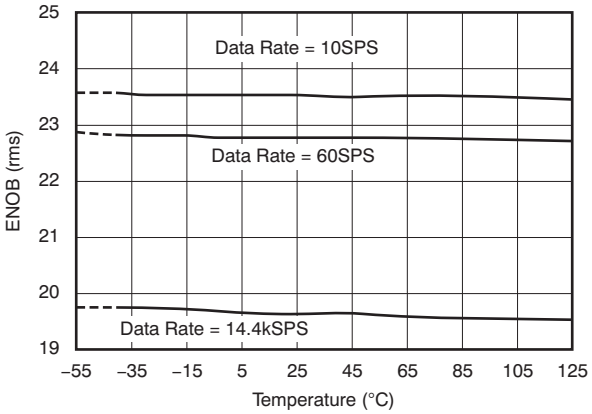


Figure 6.

EFFECTIVE NUMBER OF BITS HISTOGRAM

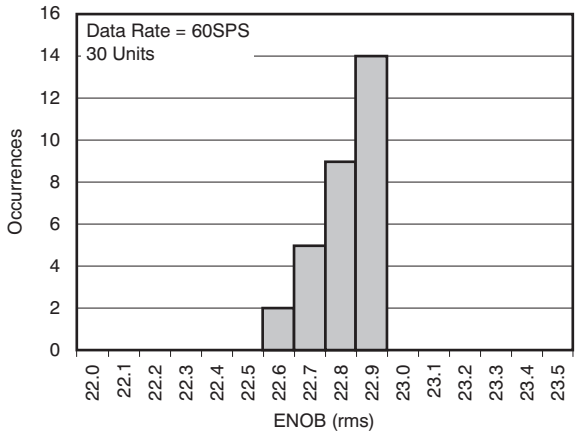


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = 3.3V, V_{REF} = 2.5V, VREFN = AVSS, f_{CLK} = 7.3728MHz, and f_{DATA} = 60SPS, unless otherwise noted.

NOISE vs INPUT VOLTAGE

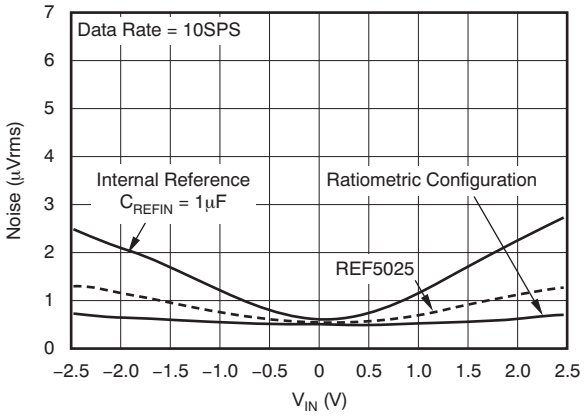


Figure 8.

NOISE vs INPUT VOLTAGE

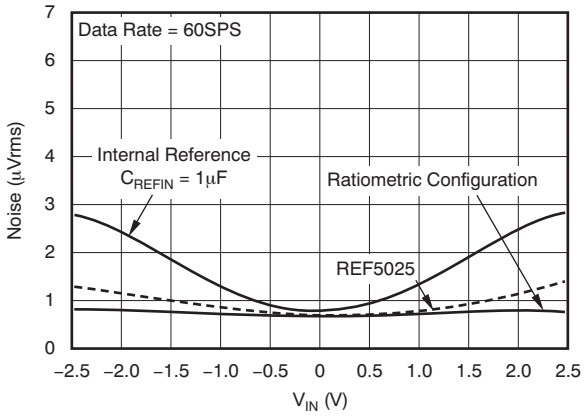


Figure 9.

NOISE vs INPUT VOLTAGE

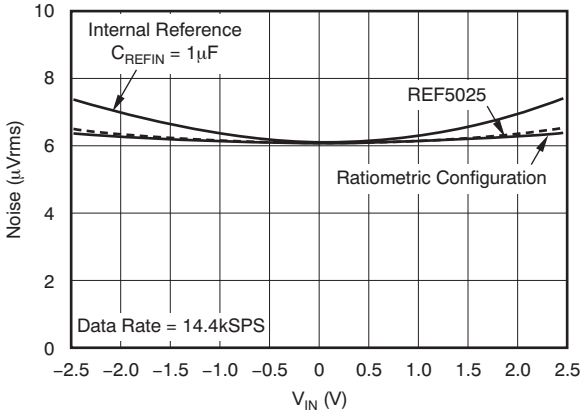


Figure 10.

NOISE vs REFERENCE VOLTAGE

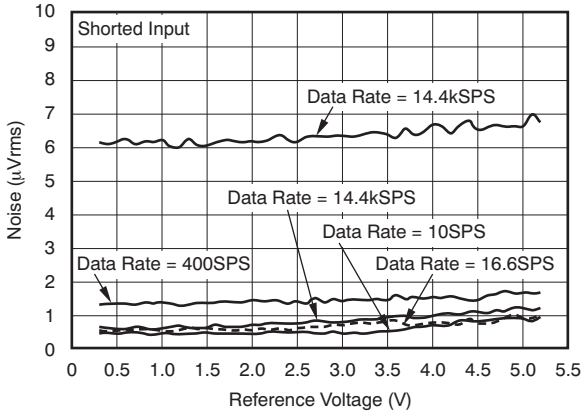


Figure 11.

LINEARITY vs INPUT LEVEL

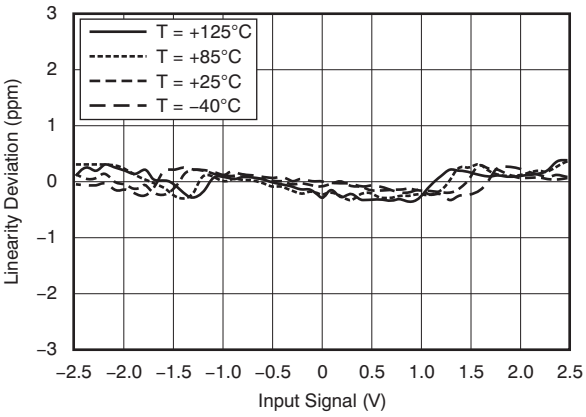


Figure 12.

INTEGRAL NONLINEARITY vs TEMPERATURE

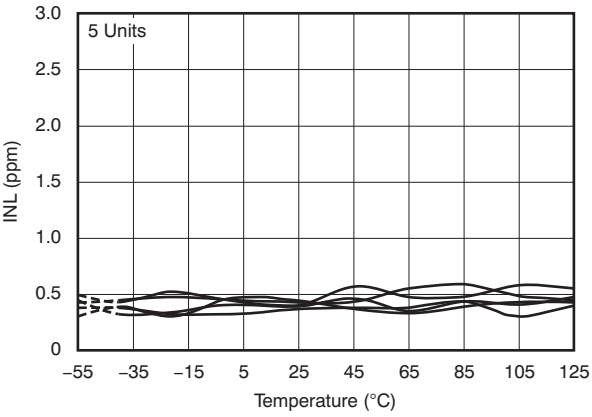


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = 3.3V, V_{REF} = 2.5V, VREFN = AVSS, f_{CLK} = 7.3728MHz, and f_{DATA} = 60SPS, unless otherwise noted.

OFFSET vs TEMPERATURE

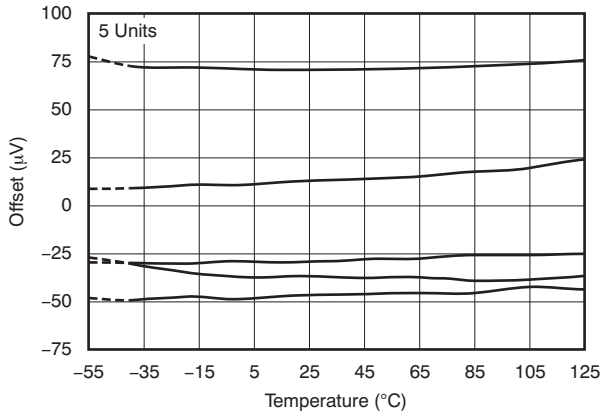


Figure 14.

GAIN vs TEMPERATURE

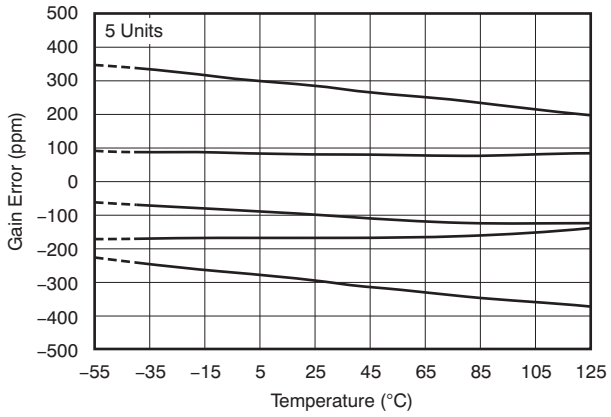


Figure 15.

OFFSET DRIFT DISTRIBUTION HISTOGRAM

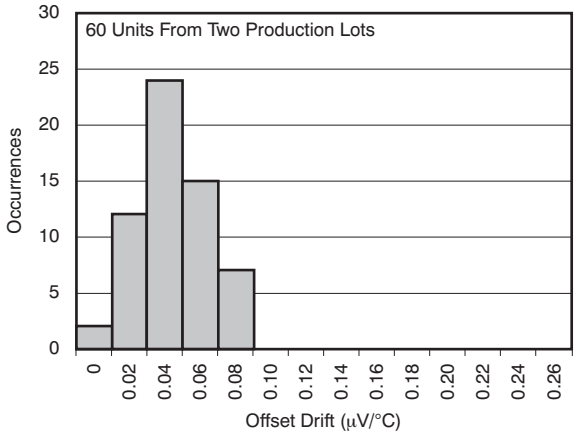


Figure 16.

GAIN DRIFT DISTRIBUTION HISTOGRAM

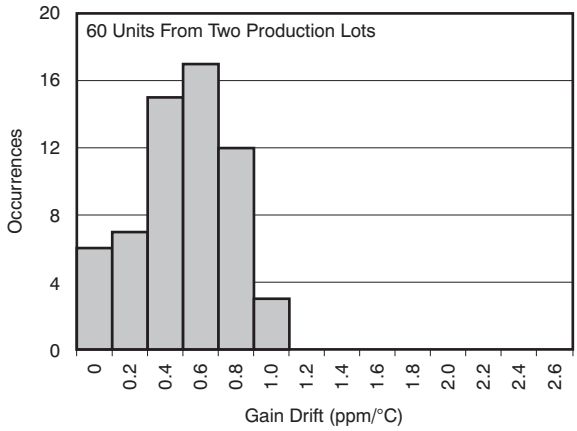


Figure 17.

INTEGRAL NONLINEARITY vs REFERENCE VOLTAGE

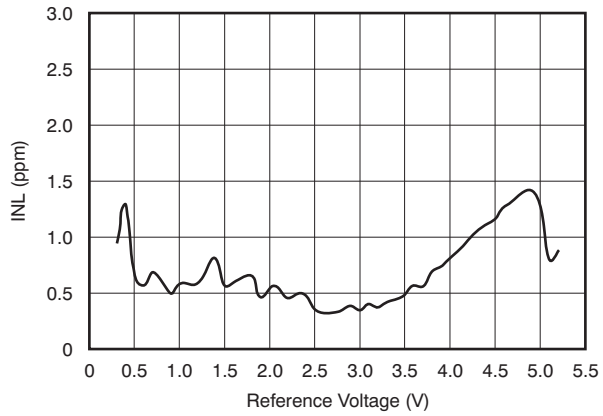


Figure 18.

GAIN ERROR AND OFFSET vs REFERENCE VOLTAGE

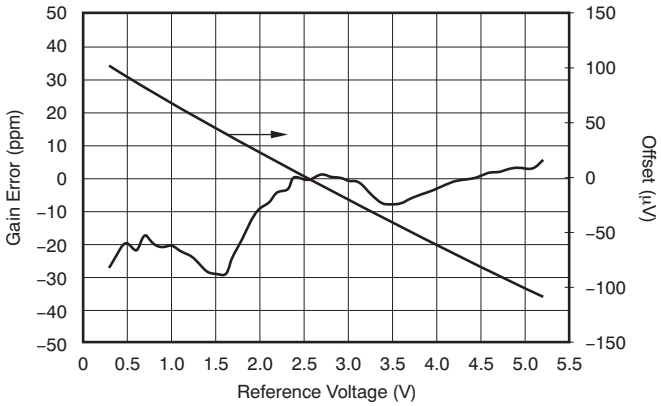


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = 3.3V, V_{REF} = 2.5V, VREFN = AVSS, f_{CLK} = 7.3728MHz, and f_{DATA} = 60SPS, unless otherwise noted.

POWER-SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY

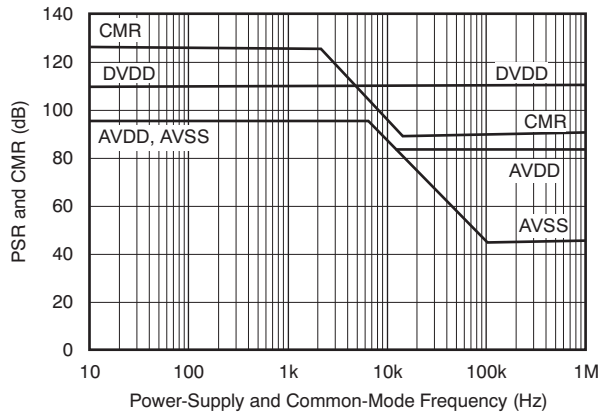


Figure 20.

POWER-SUPPLY CURRENT vs TEMPERATURE

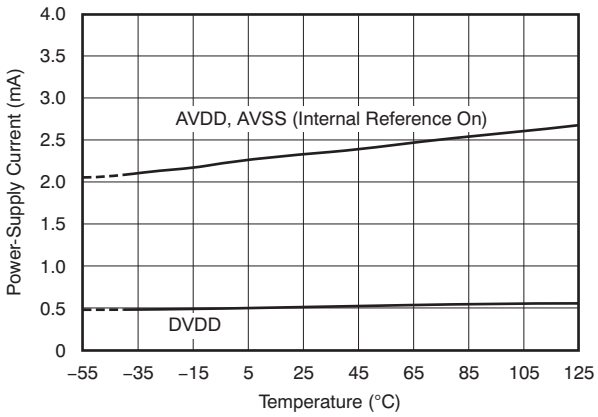


Figure 21.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE

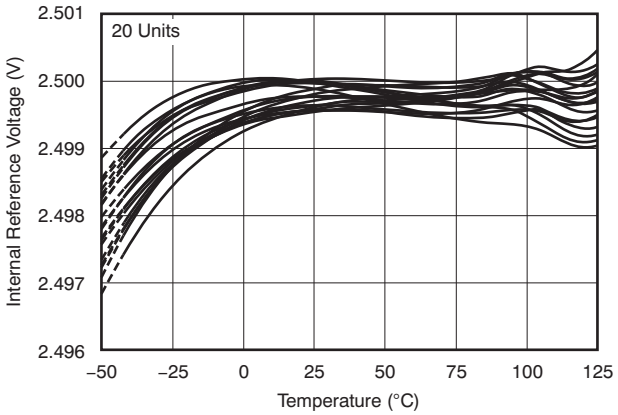


Figure 22.

INTERNAL OSCILLATOR vs TEMPERATURE

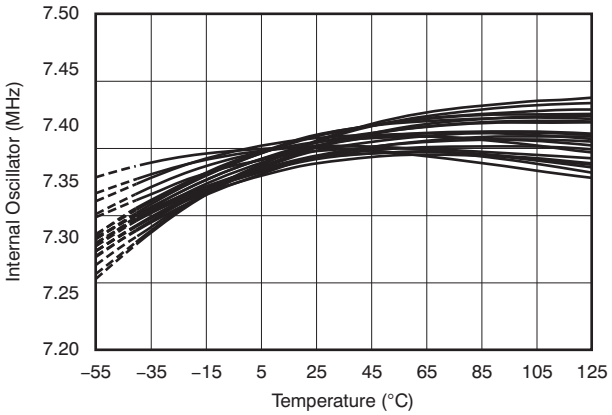


Figure 23.

OUT-OF-RANGE THRESHOLD DISTRIBUTION HISTOGRAM

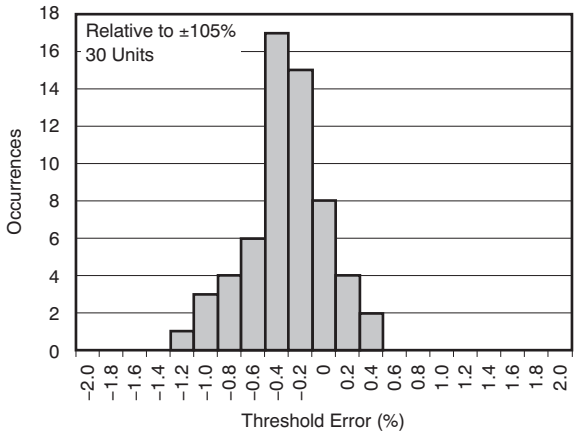


Figure 24.

OUT-OF-RANGE THRESHOLD vs TEMPERATURE

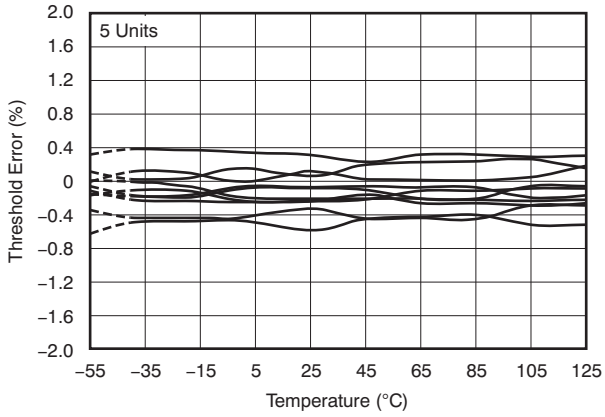


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = 3.3V, V_{REF} = 2.5V, VREFN = AVSS, f_{CLK} = 7.3728MHz, and f_{DATA} = 60SPS, unless otherwise noted.

REFERENCE INPUT CURRENT vs TEMPERATURE

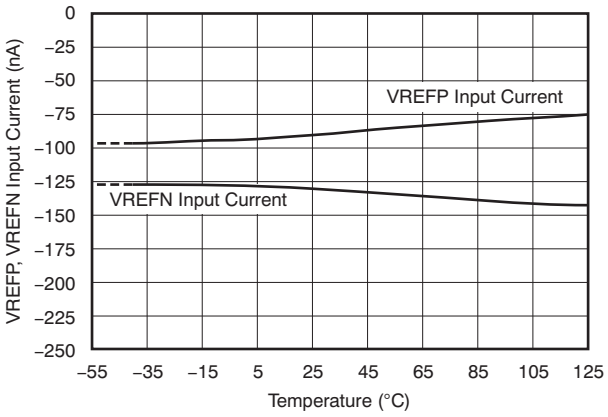


Figure 26.

REFERENCE INPUT CURRENT vs REFERENCE VOLTAGE

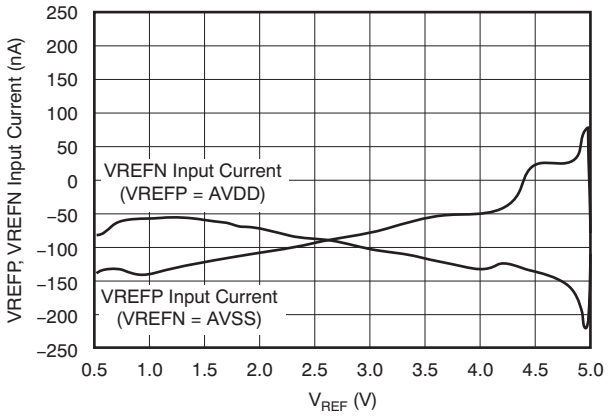


Figure 27.

DIFFERENTIAL INPUT IMPEDANCE vs TEMPERATURE

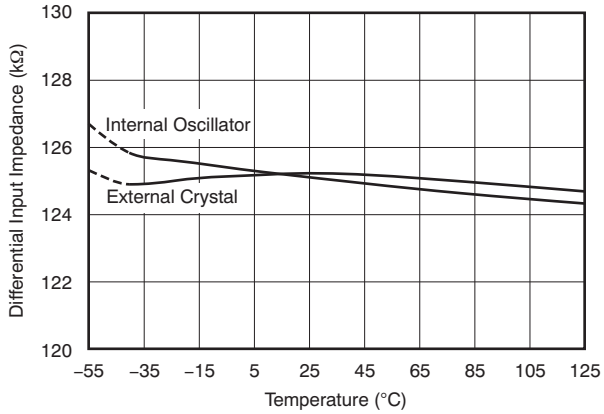


Figure 28.

INTERNAL REFERENCE SETTLING TIME

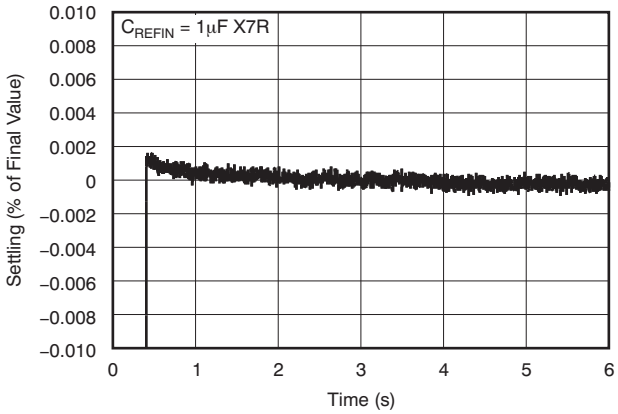


Figure 29.

OVERVIEW

The ADS1259 is a high-linearity, low drift analog-to-digital converter (ADC) designed for the needs of industrial process control, precision instrumentation, and similar applications. The converter provides high-resolution, 24-bit output data at sample rates ranging from 10SPS to 14.4kSPS.

Figure 30 shows a block diagram of the ADS1259. The device allows unipolar or bipolar analog power-supply configuration (AVDD – AVSS = 5V total). The analog supplies may be set to single +5V to accept unipolar (or offset-bipolar) signals or the supplies can be set to ±2.5V to accept true bipolar signals. The operating range of the digital power supply (DVDD) is 2.7V to 5V.

An internal low dropout regulator (LDO) powers the digital core from the DVDD supply while the device I/O operates directly from DVDD. BYPASS is the LDO output and requires a 0.1µF or larger capacitor to ground.

The inherently stable, fourth-order, ΔΣ modulator measures the differential input signal [V_{IN} = (AINP – AINN)] against the differential reference [V_{REF} = (VREFP – VREFN)]. A fast responding out-of-range detector flags the output data if the input should over-range while converting.

The digital filter receives the modulator signal and provides the digital output. The filter consists of a fifth-order sinc filter followed by a programmable averager, selectable as either a $sinc^1$ or $sinc^2$. In $sinc^1$ mode, the filter settles in a single conversion. The programmable averaging yields output data rates from 10SPS to 14.4kSPS.

The ADS1259 integrates a low-drift, low-noise +2.5V reference. The internal reference can drive loads up to ±10mA. The ADS1259 also operates from an external reference if desired. The reference input is buffered to reduce loading of external circuits.

An onboard oscillator is provided as the clock source for the device. Optionally, an external crystal can be used. As a third clock option, the device can be driven by an external clock source. SYNCOUT is an output that provides a 1/8 rate clock intended to drive the chopping clock input of the PGA280.

Gain and offset registers scale the digital filter output to produce the final code value. On-command calibration corrects for system offset and gain errors.

An SPI-compatible serial interface provides the control and configuration as well as the data interface to the ADS1259. Onboard registers combined with commands are used to control and configure the device.

The $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ pin is dual function. A momentary low resets the device and, if the pin is held low, powers down the device. The START pin, as well as commands, controls the conversions.

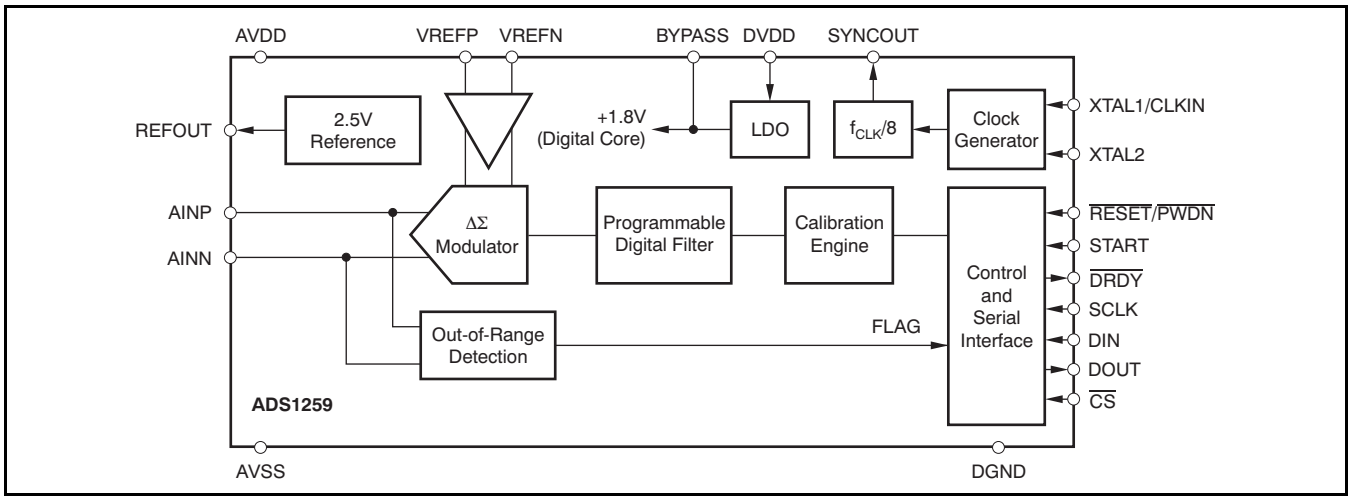


Figure 30. ADS1259 Block Diagram

NOISE PERFORMANCE

The ADS1259 offers excellent noise performance that can be optimized by adjusting the data rate and by selection of the digital filter mode. As the averaging is increased by reducing the data rate, the noise drops correspondingly. Additionally, because the $sinc^2$ digital filter provides more filtering than the $sinc^1$ digital filter, $sinc^2$ provides lower noise conversions. Table 1 shows the noise as a function of data rate and filter mode.

Table 1 expresses typical noise data in several ways: RMS noise, effective number of bits (ENOB), and noise-free bits. ENOB is calculated from Equation 1:

$$ENOB = \frac{\ln\left(\frac{FSR}{RMS\ Noise}\right)}{\ln(2)} \quad (1)$$

Where:

$FSR = 2V_{REF}$

The calculation of noise-free bits uses the same formula as Equation 1, except that the peak-to-peak noise value is used instead of RMS noise.

ADC

The analog-to-digital converter (ADC) section of the ADS1259 is composed of two blocks: a high accuracy modulator and a programmable digital filter.

MODULATOR

The high-performance modulator is an inherently-stable, fourth-order, ΔΣ, 2 + 2 pipelined structure, as shown in Figure 31. It shifts the quantization noise to a higher frequency (out of the passband) where digital filtering can easily remove it.

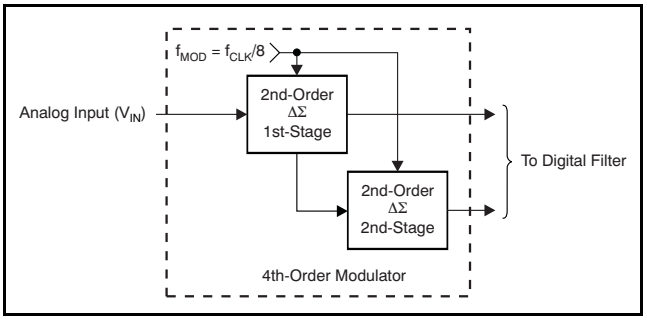


Figure 31. Fourth-Order Modulator

The modulator first stage converts the analog input voltage into a pulse-code modulated (PCM) stream. When the level of differential analog input (AINP – AINN) is near the level of the reference voltage (VREFP – VREFN), the 1s density of the PCM data stream is at its highest. When the level of the differential analog input is near zero, the PCM 0s and 1s densities are nearly equal. At the two extremes of the analog input levels (+FS and –FS), the 1s density of the PCM streams are approximately +90% and +10%, respectively.

The modulator second stage produces a 1s density data stream designed to cancel the quantization noise of the first stage. The data streams of the two stages are then combined in the digital filter stage.

Table 1. Typical Noise Data vs Data Rate and Digital Filter(1)

DATA RATE (SPS)	SAMPLE SIZE(2)	$SINC^1$ DIGITAL FILTER				$SINC^2$ DIGITAL FILTER			
		NOISE (RMS)	NOISE (p-p)	ENOB (RMS)	NOISE-FREE BITS	NOISE (RMS)	NOISE (p-p)	ENOB (RMS)	NOISE-FREE BITS
10	128	0.5	1.8	23.3	21.4	0.45	1.6	23.4	21.6
16.6	256	0.55	2.4	23.1	21.0	0.5	2	23.3	21.3
50	512	0.65	3.5	22.9	20.4	0.6	3	23.0	20.7
60	512	0.7	4	22.8	20.3	0.65	3.5	22.9	20.4
400	4096	1.4	9.5	21.8	19.0	1.2	8.3	22.0	19.2
1200	8192	2.3	17	21.1	18.2	2	14	21.3	18.4
3600	8192	3.9	32	20.3	17.3	3.4	27	20.5	17.5
14400	8192	6.2	50	19.6	16.6	(3)	(3)	(3)	(3)

(1) Noise data taken with shorted analog inputs and internal 2.5V reference using the circuit of Figure 62.
(2) Data sample sizes used for analysis.
(3) Same as $sinc^1$ mode.

MODULATOR OVERLOAD BEHAVIOR

The ADS1259 modulator is inherently stable and therefore has predictable recovery behavior resulting from an input overdrive condition. The modulator does not exhibit the self-resetting behavior of other modulator types, which often results in unstable output conversion results when overdriven.

The ADS1259 modulator outputs a 1s density data stream at 90% duty cycle with the positive full-scale input signal applied (10% duty cycle with the negative full-scale signal). If the input is overdriven past 90% modulation, but below 100% modulation (10% and 0% for negative overdrive, respectively), the modulator remains stable and continues to output the 1s density data stream. The digital filter may or may not clip the output codes to +FS or –FS, depending on the duration of the overdrive. When the input is returned to the normal range from a long duration overdrive (worst case), the modulator returns immediately to the normal range, but the group delay of the digital filter delays the return of the conversion result to within the linear range (one reading for the $sinc^1$ filter and two readings for completely settled data).

If the inputs are sufficiently overdriven to drive the modulator to full duty cycle (that is, all 1s or all 0s, or $\pm 110\% V_{REF}$), the modulator enters a stable saturated state. The digital output code may clip to +FS or –FS, again depending on the duration. A small duration overdrive may not always clip the output code. When the input returns to the normal range, the modulator requires up to 12 modulator clock cycles (f_{MOD}) to exit saturation and return to the linear region. The digital filter requires two additional conversions ($sinc^1$, more for $sinc^2$) for fully settled data.

In the extreme case of over-range, either input is overdriven exceeding that either analog supply voltage plus an internal ESD diode drop. The internal ESD diodes begin to conduct and the signal on the input is clipped. If the differential input signal range is not exceeded, the modulator remains in linear operation. If the differential input signal range is exceeded, the modulator is saturated but stable, and outputs all 1s or 0s. When the input overdrive is removed, the diodes recovery quickly and the ADS1259 recovers as normal. Note that the linear input range is ±100mV beyond the analog supply voltages; with input levels greater than this range, use care to limit the input current to 100mA peak transient (10mA continuous).

INPUT OUT-OF-RANGE DETECTION (FLAG)

The ADS1259 has a fast-responding out-of-range circuit that triggers when the differential input exceeds 105% of FSR ($\pm V_{REF}$). The out-of-range circuit latches the result of the comparator output and appends the result as either the LSB of conversion data or as bit 7 of the data checksum byte. After the conversion data are read, or after a new conversion is started, the comparator latch is reset. Figure 32 and Figure 33 show the detection block diagram and the detection operation, respectively. See the *Data Checksum Byte and FLAG Bit* section for more detail.

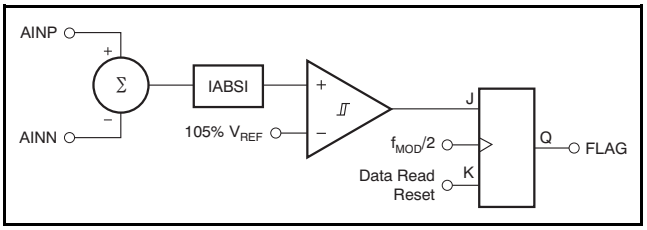


Figure 32. Input Out-Of-Range Detect Block Diagram

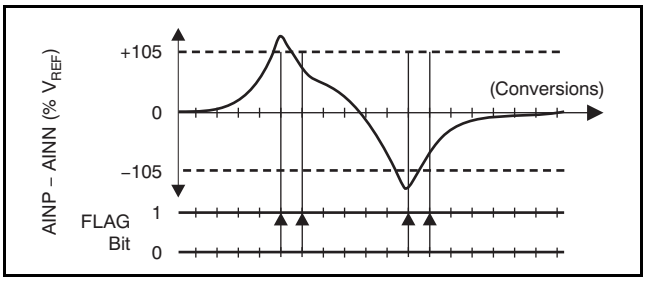


Figure 33. Input Out-Of-Range Detect Operation

Note that the flag status bit associated with the FIRST conversion after a START condition or after changes to registers CONFIG[2:0] is not valid and should be ignored.

ANALOG INPUTS (AINP, AINN)

The ADS1259 measures the differential input signal V_{IN} = (AINP – AINN) against the differential reference V_{REF} = (VREFP – VREFN) using internal capacitors that are continuously charged and discharged. Figure 35 shows the simplified schematic of the ADC input circuitry; the right side of the figure illustrates the input circuitry with the capacitors and switches replaced by an equivalent circuit. Figure 34 demonstrates the ON/OFF timings for the switches of Figure 35.

In Figure 35, S_1 switches close during the input sampling phase. With switch S_1 closed, C_{A1} charges to AINP, C_{A2} charges to AINN, and C_B charges to (AINP – AINN). For the discharge phase, S_1 opens first and then S_2 closes. C_{A1} and C_{A2} discharge to approximately to AVSS + 2.5V and C_B discharges to 0V. This two-phase sample/discharge cycle repeats with a period of $t_{SAMPLE} = 1/f_{MOD}$. f_{MOD} is the operating frequency of the modulator, where $f_{MOD} = f_{CLK}/8$.

The charging of the input sampling capacitors draws a transient current from the source driving the ADS1259 ADC inputs. The average value of this current can be used to calculate an effective impedance (R_{EFF}) where $R_{EFF} = V_{IN}/I_{AVERAGE}$. These impedances scale inversely with f_{MOD}. For example, if f_{MOD} is reduced by a factor of two, the impedances double. Note that the sampling capacitors can vary ±15% over production lots and typically vary 1% with temperature. The variations of the sampling capacitors have a corresponding effect on the analog input impedance.

ESD diodes protect the analog inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below AVSS by more than 300mV, and likewise do not exceed AVDD by more than 300mV.

AVSS – 300mV < (AINP or AINN) < AVDD + 300mV.

Note that the valid input range is:

AVSS – 100mV < (AINP or AINN) < AVDD + 100mV

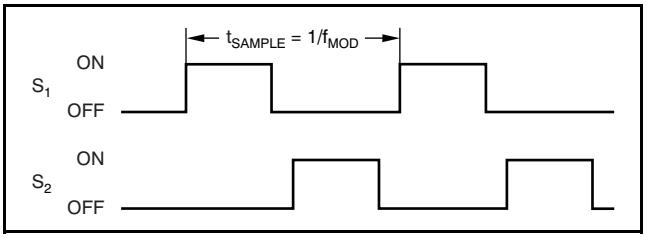


Figure 34. S_1 and S_2 Switch Timing for Figure 35

Although optimized for differential signals, the ADS1259 inputs may be driven with a single-ended signal by fixing one input to AVSS or mid-supply. Full dynamic range is achieved when the inputs are differentially driven $\pm V_{REF}$.

As a result of the switched-capacitor input structure of the ADS1259, a buffer is recommended to drive the analog inputs. An input filter comprised of 20Ω to 50Ω resistors and 10nF capacitors should also be used between the buffer and the ADS1259 inputs.

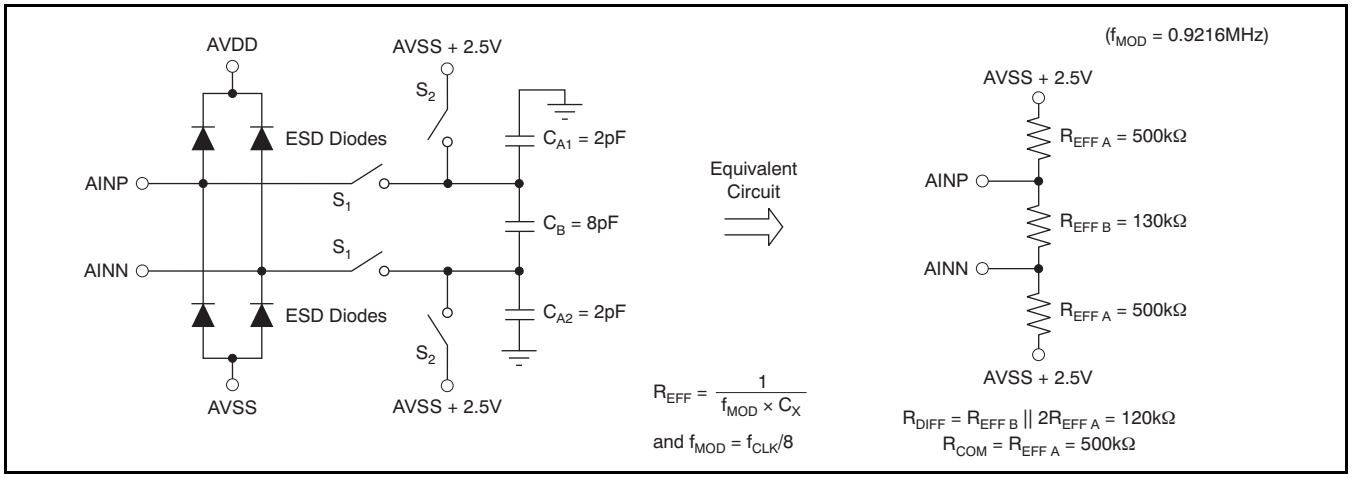


Figure 35. Simplified ADC Input Structure

REFERENCE

The ADS1259 includes an onboard voltage reference with a low temperature coefficient. The reference voltage is 2.5V with the capability of sinking and sourcing 10mA via the REFOUT pin. The ADS1259 can also operate from an external reference. The external reference is the default selection. Refer to Figure 36 for a reference block diagram.

Internal Reference

The reference output is provided between pins REFOUT and AVSS. Because the reference output return shares the same pin as AVSS, route the reference return trace and the AVSS trace independently as Kelvin-connected printed circuit board (PCB) traces. For stability reasons, connect a 1µF capacitor between REFOUT and AVSS.

An internal switch connects the internal reference to the ADC reference input pins, VREFP and VREFN. (Note that these device pins are not intended to drive external circuits.) An external 1µF capacitor, connected from VREFP to VREFN, is recommended for noise reduction. The capacitor can be increased for increased noise filtering, but the settling time of the reference may also increase. The settling time should be considered upon activating the internal reference.

See Figure 29 for typical reference settling C_{REFIN} = 1µF. The capacitor dielectric absorption results in increased settling time for RC filter circuits.

To activate the internal reference, set the register bit RBIAS = 1. This enables the reference bias. Once biased, the internal reference can then be selected as the ADC reference by the register bit EXTREF. EXTREF = 0 closes the internal switches.

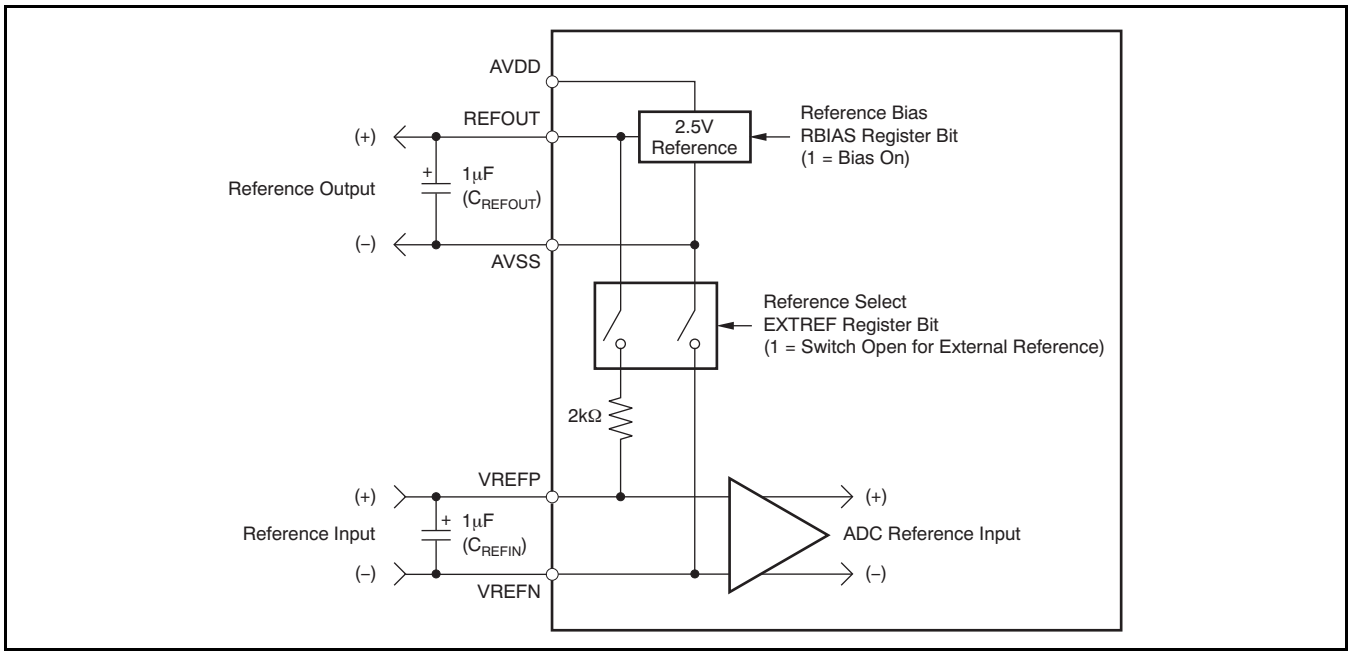


Figure 36. Reference Block Diagram

Table 2. Reference Selection for Figure 36

ADS1259 REFERENCE	RBIAS REGISTER BIT	EXTREF REGISTER BIT
Internal	1	0
External	See (1)	1

(1) If the reference output is not required, set RBIAS = 0. If the reference output is enabled (RBIAS = 1), an external 1µF capacitor must be used between REFOUT and AVSS.

Reference Drift

The ADS1259 internal reference is designed for minimal drift error, which is defined as the change in reference voltage over temperature. The drift is calculated using the box method, as described by Equation 2.

$$\text{Drift} = \left(\frac{V_{REFMAX} - V_{REFMIN}}{V_{REFNOM} \times \text{Temp Range}} \right) \times 10^6 \text{ (ppm)} \quad (2)$$

Where:

V_{REFMAX}, V_{REFMIN}, and V_{REFNOM} are the maximum, minimum, and nominal reference output voltages, respectively, over the specified temperature range.

The ADS1259 internal reference features a maximum drift coefficient of 5ppm/°C over 0°C to +85°C operating range and 12ppm/°C over –40°C to +105°C operating range.

External Reference

To select the ADS1259 for external reference operation, set the EXTREF register bit = 1 (default). If desired, the internal reference can continue to provide a +2.5V reference output via the REFOUT and AVSS pins. In this case, set the RBIAS register bit = 1 to power the internal reference. If the internal reference is activated, an external 1µF capacitor from REFOUT to AVSS is required.

For external reference applications, place a 1µF (minimum) capacitor close to the VREFP and VREFN pins.

Because the ADS1259 measures the signal inputs (AINP and AINN) against the reference inputs (VREFP and VREFN), reference noise and drift may degrade overall system performance. In ratiometric measurement applications, reference noise and drift have a cancelling effect. In absolute measurement applications, reference noise and drift directly effect the conversion results.

Voltage Reference Inputs (VREFP, VREFN)

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AVSS by more than 300mV, and likewise do not exceed AVDD by more than 300mV.

The absolute maximum reference input range is:

AVSS – 300mV < (VREFP or VREFN) < AVDD + 300mV

Note that the valid operating range of the reference inputs are shown in the Electrical Characteristics table.

DIGITAL FILTER

The programmable low-pass digital filter receives the modulator output and produces a high-resolution digital output. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rate.

The filter consists of two sections: a fixed decimation $sinc^5$ filter followed by a variable decimation filter, configurable as $sinc^1$ or $sinc^2$, as illustrated in Figure 37. The $sinc^5$ filter has fixed decimation of 64 and reduces the data rate of the modulator from $f_{CLK}/8$ to $f_{CLK}/512$. The second filter stage receives the data from the $sinc^5$ filter. The second filter stage has programmable averaging (or decimation) and can be configured in either $sinc^1$ or $sinc^2$ mode. The decimation ratio of this stage sets the final output data rate. As detailed in Table 3, the DR[2:0] register bits program the decimation ratio and the final output data rate. The output data rates are identical for both $sinc^1$ and $sinc^2$ filters.

Table 3. Decimation Ratio of Final Filter Stage

DR[2:0] REGISTER BITS	DECIMATION RATIO (R)	DATA RATE (SPS)
111	1	14400
110	4	3600
101	12	1200
100	36	400
011	240	60
010	288	50
001	864	16.6
000	1440	10

The SINC2 register bit selects either the $sinc^1$ or $sinc^2$ filter. The $sinc^1$ filter settles in one conversion cycle while the $sinc^2$ filter settles in two conversion cycles. However, the $sinc^2$ filter has the benefit of wider frequency notches which improve line cycle rejection.

FREQUENCY RESPONSE

The low-pass digital filter sets the overall frequency response of the ADS1259. The filter response is the product of the fixed and programmable filter sections, and is given by Equation 4:

$$\left|H_{(f)}\right| = \left|H_{sinc}{}^{5}(f)\right| \times \left|H_{sinc}{}^{N}(f)\right| = \left| \frac{\sin\left(\frac{512\pi \times f}{f_{CLK}}\right)}{64 \times \sin\left(\frac{8\pi \times f}{f_{CLK}}\right)} \right|^{5} \times \left| \frac{\sin\left(\frac{512\pi \times R \times f}{f_{CLK}}\right)}{R \times \sin\left(\frac{512\pi \times f}{f_{CLK}}\right)} \right|^{N} \quad (4)$$

where:

N = 1 ($sinc^1$)

N = 2 ($sinc^2$)

R = Decimation ratio (refer to Table 3)

The digital filter attenuates noise on the modulator output, including noise from within the ADS1259 and external noise present within the ADS1259 input signal. Adjusting the filtering by changing the decimation ratio used in the programmable filter changes the filter bandwidth. With a higher number of decimation, the bandwidth is reduced and more noise is attenuated.

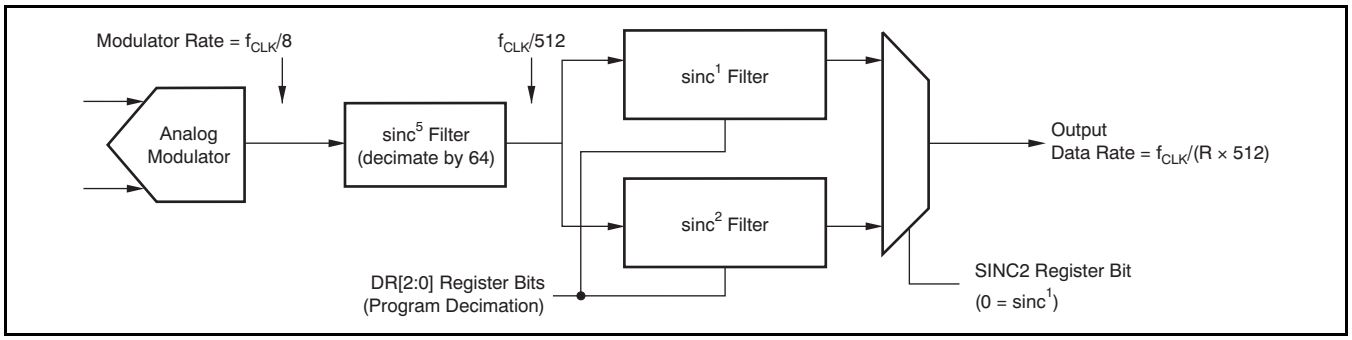


Figure 37. Block Diagram of Digital Filter

The sinc^5 filter produces wide notches at f_{CLK}/512 and multiples thereof. At these frequencies the filter has zero gain. Figure 38 shows the response data rate = 14.4kSPS.

With decimation of the second stage, the wide notches produced by the sinc^5 filter remain, but a number of narrow notches are superimposed in the response. The first of the notches occur at the data rate. The number of superimposed notches is determined by the decimation ratio, minus 1.

The second stage filter has notches (or zeroes) at the data rate and multiples thereof. Figure 39 shows the response of the second stage filter combined with the sinc^5 stage. Decimation of 4 produces three equally-spaced notches between each main notch of the sinc^5 filter. The frequency response of the other data rates (higher decimation ratios) produces a similar pattern, but with more equally-spaced notches between the main sinc^5 notches. Table 4 lists the first notch frequency and the –3dB bandwidth.

Figure 40 illustrates the detail of the magnitude response with data rate = 60SPS. Note that input frequencies within the ±1% 60Hz bandwidth are attenuated 40dB by the sinc^1 filter and 80dB by the sinc^2 filter.

Table 4. First Notch Frequency and –3dB Filter Bandwidth(1)

DATA RATE (SPS)	FIRST NOTCH (Hz)	–3dB BANDWIDTH (Hz)	
		sinc^1	sinc^2
10(2)	10	4.3	3.1
16.6(3)	16.6	7.3	5.2
50	50	22	16
60	60	27	19
400	400	177	127
1200	1200	525	380
3600	3600	1440	1100
14400	14400	2930	See (4)

(1) f_{CLK} = 7.3728MHz.
(2) Notch at 50Hz and 60Hz.
(3) Notch at 50Hz.
(4) Same as sinc^1.

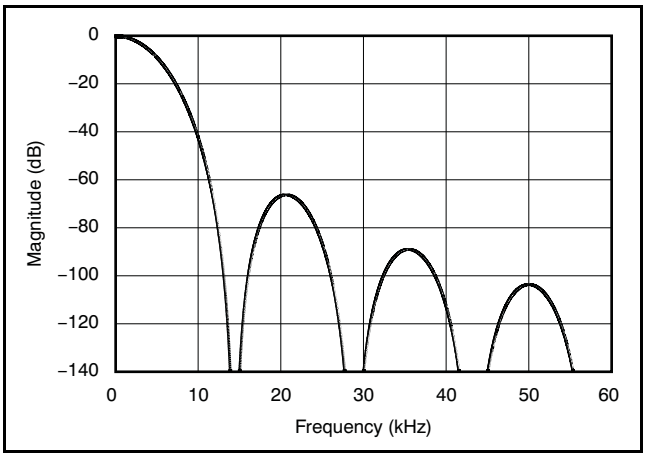


Figure 38. Frequency Response for Data Rate = 14.4kSPS

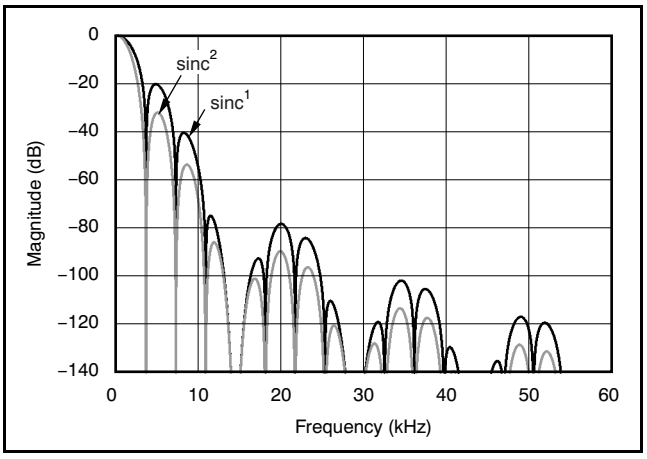


Figure 39. Frequency Response (Data Rate = 3600SPS, R = 4)

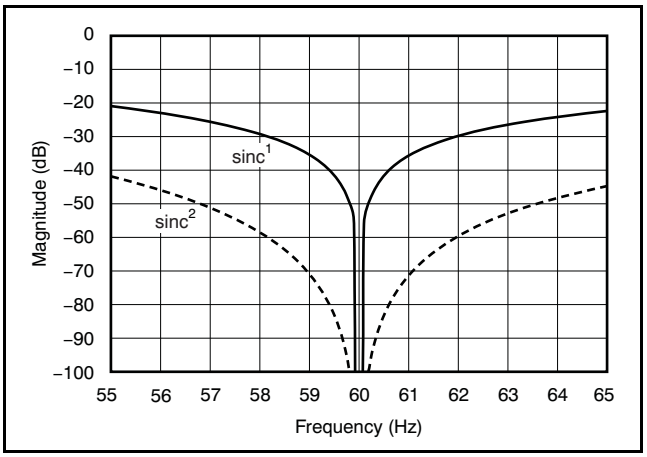


Figure 40. Magnitude Response for Data Rate = 60SPS

ALIASING

The low-pass characteristic of the digital filter repeats at multiples of the modulator rate (f_{MOD} = f_{CLK}/8). Figure 41 shows the responses plotted out to 7.3728MHz at the data rate of 14.4kSPS. Notice how the responses near dc, 0.9216MHz, 1.8432MHz, 2.7698MHz, etc, are the same as given by f = $Nf_{MOD} \pm f_{DATA}$ where *N* = 0, 1, 2, etc. The digital filter attenuates high-frequency noise on the ADS1259 inputs up to the frequency where the response repeats. However, noise or frequency components existing in the signal where the response repeats alias into the passband. Often, a simple RC antialias filter is sufficient to reject these input frequencies.

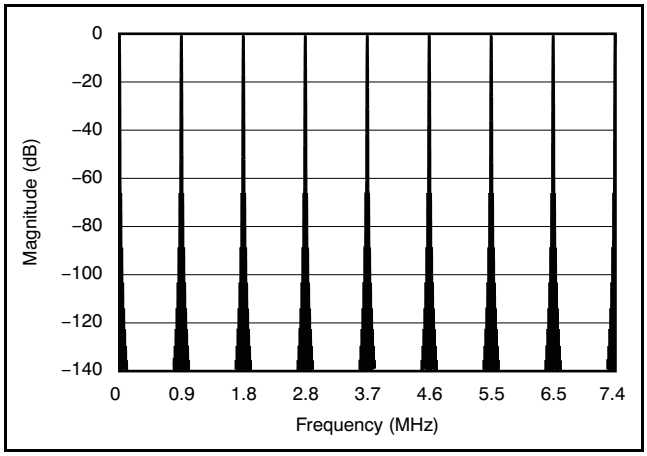


Figure 41. Frequency Response to 7.3728MHz (Data Rate = 14400SPS)

CLOCK SOURCE

There are three ways to provide the ADS1259 clock: the internal oscillator, an external clock, or an external crystal/ceramic resonator. The ADS1259 selects the clock source automatically. Figure 42 shows the clock select block. If either external clock sources are present, the internal oscillator is disabled and the external clock source is selected. If no external clock is present, the internal oscillator is selected. The ADS1259 continuously monitors the clock source. The clock source can be polled by the EXTCLK bit (bit 6 of register CONFIG2), 0 = internal oscillator, 1 = external clock.

The data rate and corresponding filter notches scale by the accuracy of clock frequency. Consideration should be given to the clock accuracy and the corresponding effect to the notch frequency locations.

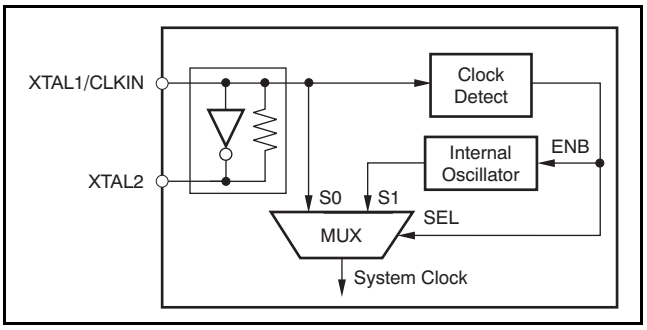


Figure 42. Equivalent Circuitry of the Clock Source

Internal Oscillator

Figure 43 shows the internal oscillator connection. XTAL1/CLKIN is grounded and XTAL2 is not connected (floating). The internal oscillator draws approximately 40µA from the DVDD supply. Note that the internal oscillator has ±2% accuracy over temperature. The oscillator accuracy has a corresponding effect on line-cycle notch frequency locations.

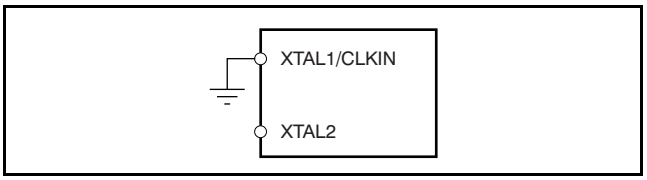


Figure 43. Internal Oscillator Connection

External Clock

Figure 44 shows the external clock connection. The clock is applied to XTAL1/CLKIN and XTAL2 floats. Make sure a clean clock input is applied to the ADS1259, free of overshoot and glitches. A series resistor often helps to reduce overshoot and should be placed close to the driving end of the clock source.

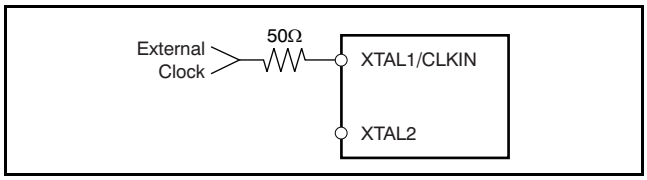


Figure 44. External Clock Connection

Crystal Oscillator

Figure 45 shows the crystal oscillator connection. The crystal connects to XTAL1/CLKIN and XTAL2 and the capacitors connect to ground. The crystal and capacitors should be placed close to the device pins with short, direct traces. Neither the XTAL1/CLKIN nor the XTAL2 pins can be used to drive any other logic. Table 5 lists the recommended crystal for the ADS1259. If using other crystals, verify the oscillator start-up behavior.

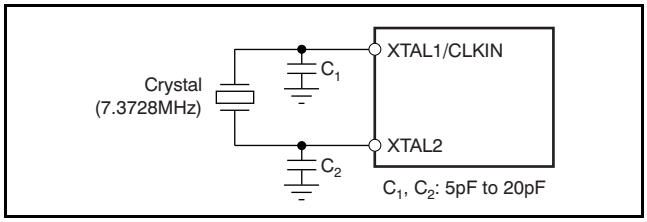


Figure 45. Crystal Connection

Table 5. Recommended Crystal

MANUFACTURER	FREQUENCY	PART NUMBER
ECS	7.3728MHz	ECS-73-18-10

SYNCOUT

SYNCOUT is a digital output pin intended to synchronize the chopping frequency of the PGA280 to the sampling frequency of the ADS1259. Synchronizing the PGA280 to the ADS1259 places the PGA280 chopped 1/f noise at an exact null in the ADS1259 frequency response, where the PGA280 1/f noise is rejected.

SYNCOUT frequency is equal to the ADS1259 clock rate divided by 8 ($f_{SYNCOUT} = f_{CLK}/8$). The output clock is enabled by the register bit SYNCOUT. Disabling the output stops the clock but the output remains actively driven low. In power-down mode, the SYNCOUT output becomes an input. As with all digital inputs, the pin must not be allowed to float. An external 1MΩ pull-down resistor is recommended to ground the input in power-down mode.

The SYNCOUT clock is reset when START is received and whenever registers CONFIG[2:0] are changed. Connect SYNCOUT to the PGA280 SYNCIN pin through a 1kΩ series resistor. Place the resistor as close as possible to the ADS1259 SYNCOUT pin.

SLEEP MODE

SLEEP mode is started by sending the SLEEP command. In SLEEP mode, the device enters a reduced power state and only a minimum of circuitry is kept active. The WAKEUP command exits the SLEEP mode and after which 512 f_{CLK} cycles are counted before the ADS1259 is ready for communication. The register settings are unaffected in SLEEP.

SLEEP does not change the RBIAS register bit. For quick conversions after WAKEUP, keep the internal reference bias on before entering SLEEP. Otherwise, after exiting SLEEP mode, allow time for the reference to settle. Alternatively, to minimize power consumption during SLEEP, set the internal reference bias off prior to engaging SLEEP. Note that in SLEEP mode the SPI timeout function is disabled.

BYPASS

The digital core of the ADS1259 is powered by an internal low dropout regulator (LDO). The DVDD supply is the LDO input and the BYPASS pin is the LDO output. A 1µF capacitor must be connected from the LDO output to DGND. No other load current should be drawn from the BYPASS pin.

RESET/PWDN

The RESET/PWDN pin has two functions: device power-down and device reset. Momentarily holding the pin low resets the device and holding the pin low for 2^{16} f_{CLK} cycles activates the Power-Down mode.

POWER-DOWN MODE

In power-down mode, internal circuit blocks are disabled (including the oscillator, reference, and SPI) and the device enters a micro-power state. To engage power-down mode, hold the RESET/PWDN pin low for 2^{16} f_{CLK} cycles. Note that the register contents are not saved because they are reset when RESET/PWDN goes high.

Keep the digital inputs at defined V_{IH} or V_{INL} logic levels (do not 3-state). To minimize power-supply leakage current, disable the external clock. Note that the ADS1259 digital outputs remain active in power-down. The analog signal inputs may float.

To exit power-down, take RESET/PWDN high. Wait 2^{16} f_{CLK} cycles before communicating to the ADS1259, as shown in Figure 46.

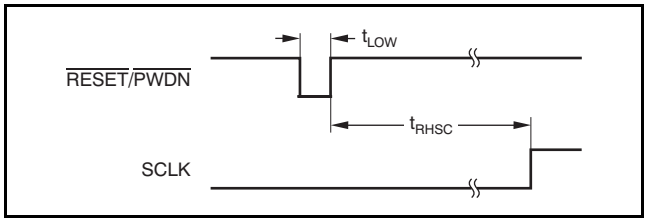


Figure 46. RESET/PWDN Timing

RESET

There are three methods to reset the ADS1259: cycle the power supplies, take RESET/PWDN low, or send the RESET opcode command.

When using the RESET/PWDN pin, take it low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the RESET pin back high.

The RESET command takes effect on the eighth falling SCLK edge of the opcode command. On reset, the configuration registers are initialized to the default states and the conversion cycle restarts. After reset, allow eight f_{CLK} cycles before communicating to the ADS1259. Note that when using the reset command, the SPI interface itself may require reset before accepting the command. See the *SPI Timing Characteristics* section for details.

POWER-ON SEQUENCE

The ADS1259 has three power supplies: AVDD, AVSS, and DVDD. The supplies can be sequenced in any order but be sure that at any time the analog inputs do not exceed AVDD or AVSS and the digital inputs do not exceed DVDD. After the last power supply has crossed the respective power-on threshold, 2^{16} f_{CLK} cycles are counted before releasing the internal reset. After the internal reset is released, the ADS1259 is ready for operation. Figure 47 shows the power-on sequence of the ADS1259.

Table 6. Timing Characteristics for Figure 46

SYMBOL	DESCRIPTION	MIN	UNIT
t_{LOW}	Pulse width low for reset	4	t_{CLK}
t_{LOW}	Pulse width low for power-down	2^{16}	t_{CLK}
t_{RHSC}	Reset high to SPI communication start	8	t_{CLK}
t_{RHSC}	Exit power-down to SPI communication start	2^{16}	t_{CLK}

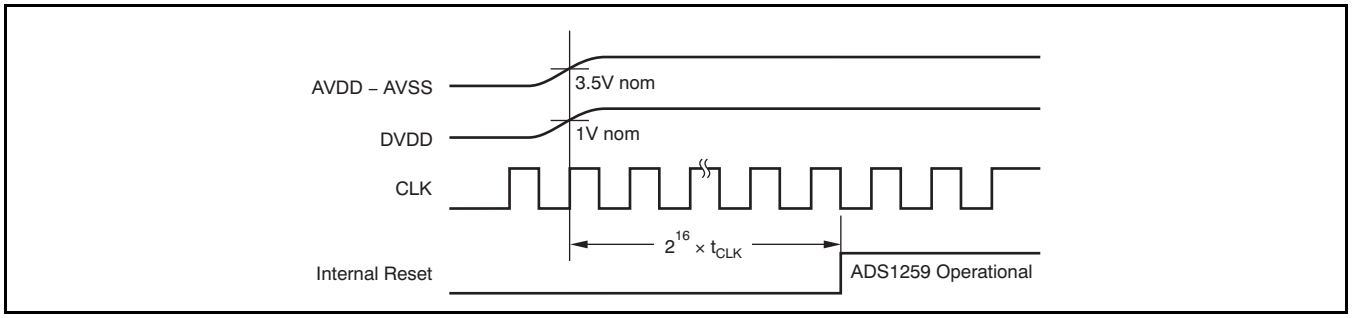
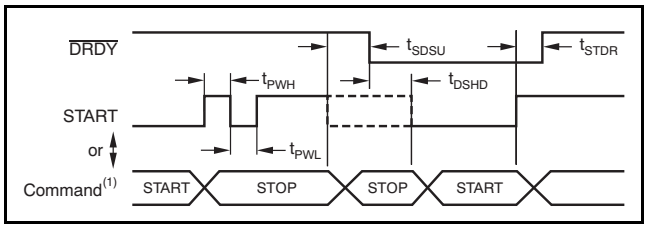


Figure 47. Power-On Sequence

START

START is a digital input that controls the ADS1259 conversions. Conversions are started when START is taken high and are stopped when START is taken low. If START is toggled during a conversion, the conversion is restarted. DRDY goes high when START is taken high. Figure 48 andTable 7 show the START timing.

Note that reasserting START within 22 t_{CLK} cycles of the DRDY falling edge causes DRDY to fall soon after. This conversion result should be discarded. The next DRDY falling edge, as given in Table 9, is the valid conversion data.



(1) START and STOP commands take effect on the seventh SCLK falling edge.

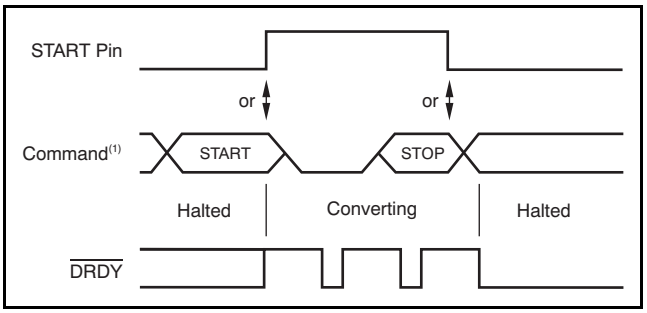
Figure 48. START to DRDY Timing

CONVERSION CONTROL

The conversions of the ADS1259 are controlled by either the START pin or by the START command. When using commands to control conversions, hold the START pin low. The ADS1259 features two modes to control conversions: Gate Control mode and Pulse Control mode. The mode is selected by the PULSE register bit.

Gate Control Mode (PULSE Bit = 0, Default)

Conversions begin when either the START pin is taken high or when the START command is sent. Conversions continue indefinitely until the START pin is taken low or the STOP command is transmitted. As seen in Figure 49, DRDY is forced high when the conversion starts and falls low when data are ready. When stopped, the conversion in process completes and further conversions are halted. Figure 48 and Table 7 show the timing of DRDY and START.



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge.

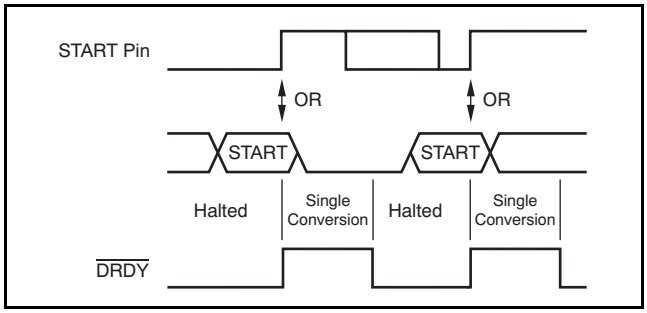
Figure 49. Gate Control Mode

Table 7. START Timing (See Figure 48)

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{SDSU}	START pin low or STOP opcode to DRDY setup time to halt further conversions	16		t_{CLK}
t_{DSHD}	START pin low or STOP opcode hold time to complete current conversion (gate mode)	16		t_{CLK}
$t_{PWH, L}$	START pin pulse width high, low	4		t_{CLK}
t_{STDR}	START pin rising edge to DRDY rising edge		4	t_{CLK}

Pulse Control Mode (PULSE Bit = 1)

In the Pulse Control mode, the ADS1259 performs a single conversion when either the START pin is taken high or when the START command is sent. As seen in Figure 50, DRDY goes high when the conversion is started. When the conversion is complete, DRDY goes low and further conversions are halted. To start a new conversion, transition the START pin back to high, or transmit the START opcode again.

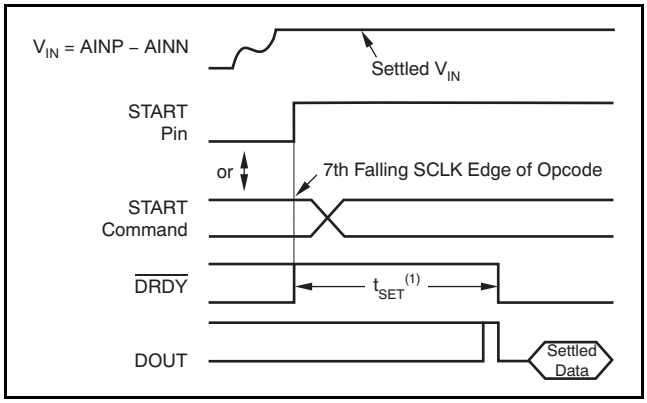


(1) START opcode command takes effect on the seventh SCLK falling edge.

Figure 50. Pulse Control Mode

CONVERSION SETTLING TIME

The ADS1259 features a digital filter architecture in which settling time can be traded for wide filter notches, resulting in improved line-cycle rejection. This trade-off is determined by the selection of the $sinc^1$ or $sinc^2$ filter. The $sinc^1$ filter settles in a single cycle while the $sinc^2$ filter provides wide-width filter notches. The settling time of the ADS1259 is different if START is used to begin conversions or if the ADS1259 is free-running the conversions. These modes are explained in the *Settling Time Using START* and *Settling Time While Continuously Converting* sections.



(1) t_{SET} = initial start delay plus the new conversion cycle time.

Figure 51. Data Retrieval Time After START

Settling Time Using START

When START goes high (via pin or command) a delay may be programmed before the conversion filter cycle begins. The programmable delay may be useful to provide time for external circuits (such as after an external signal mux change), before the reading is started. Register bits DELAY[2:0] set the initial delay time as shown in Table 8.

Table 8. Initial START Delay

DELAY[2:0]	t_{DELAY} (t_{CLK})	t_{DELAY} (µs)(1)
000	0	0
001	64	8.68
010	128	17.4
011	256	34.7
100	512	69.4
101	1024	139
110	2048	278
111	4096	556

(1) f_{CLK} = 7.3728MHz.

After the programmable delay, the digital filter is reset and a new conversion is started. DRDY goes low when data are ready. There is no need to ignore or discard data; the data are completely settled. The total time to perform the first conversion is the sum of the programmable delay time and the settling of the digital filter. That is, the value of Table 8 and Table 9 combined. Figure 51 shows the timing and Table 9 shows the settling time with programmable delay equal to '0'.

Table 9. Settling Time Using START

DATA RATE (SPS)	SETTLING TIME (t_{SET}) (ms)(1)	
	$sinc^1$	$sinc^2$
10	100	200
16.6	60.3	120
50	20.3	40.4
60	17.0	33.7
400	2.85	5.42
1200	1.18	2.10
3600	0.632	0.980
14,400	0.424	0.563

(1) f_{CLK} = 7.3728MHz, DELAY[2:0] = 000.

Settling Time While Continuously Converting

If there is a step change on the input signal while continuously converting, the next data represent a combination of the previous and current input signal and should therefore be discarded; see Figure 52 for this step change. Table 10 shows the number of conversion cycles for completely settled data while continuously converting.

Table 10. Settling Time While Continuously Converting $\overline{DRDY}$ Periods(1)

DATA RATE (SPS)	SETTLING TIME (t_{SET}) (Conversions)	
	sinc1	sinc2
10	2	3
16.6	2	3
50	2	3
60	2	3
400	2	3
1200	2	3
3600	3	4
14,400	6	7

(1) Settling time is defined as the number of $\overline{DRDY}$ periods after the input signal has settled following an input step change. For best data throughput in multiplexed applications, issue a START condition (START pin or Start command) after the input has settled following a multiplexer change; see the *Setling Time Using START* section.

OFFSET AND GAIN

The ADS1259 features low offset (40µV, typ) and low gain errors (0.05%, typ). The offset and gain errors can be corrected by sending calibration commands to the ADS1259; see the *Calibration* section.

The ADS1259 also features very low offset drift (0.05µV/°C, typ) and very low gain drift (0.5ppm/°C, typ). The offset and gain drift are calculated using the box method, as described by Equation 5 and Equation 6:

$$\text{Offset Drift} = \left(\frac{V_{OFFMAX} - V_{OFFMIN}}{\text{Temp Range}} \right) \quad (5)$$

$$\text{Gain Drift} = \left(\frac{\text{GainError}_{MAX} - \text{GainError}_{MIN}}{\text{Temp Range}} \right) \quad (6)$$

where:

V_{OFFMAX}, V_{OFFMIN}, GainError_{MAX}, and GainError_{MIN} are the maximum and minimum offset and gain error readings recorded over the Temp Range (–40°C to +105°C)

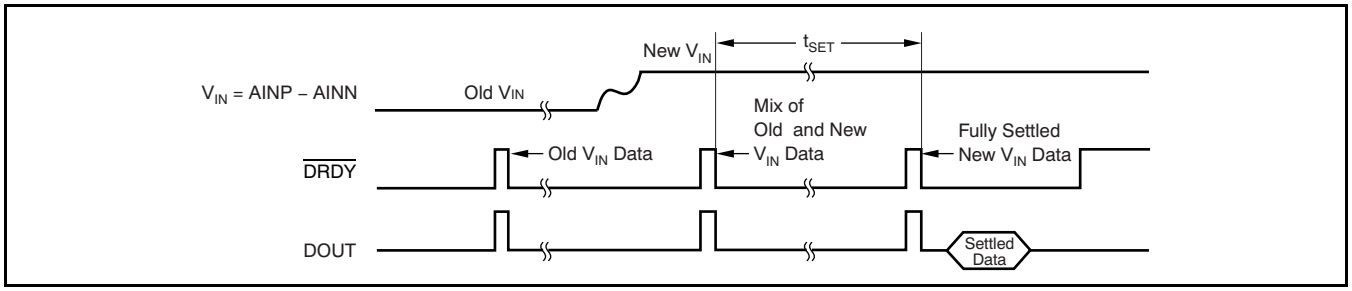


Figure 52. Step Change on V_{IN} while Continuously Converting

OFFSET AND FULL-SCALE CALIBRATION REGISTERS

The conversion data are scaled by offset and gain registers before yielding the final output code. As shown in Figure 53, the output of the digital filter is first subtracted by the offset register (OFC) and then multiplied by the full-scale register (FSC). Equation 7 shows the scaling:

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \quad (7)$$

The values of the offset and full-scale registers are set by writing to them directly, or they are set by calibration commands.

OFC[2:0] Registers

The offset calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 13. The offset is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. This value is subtracted from the conversion data. A register value of 00000h has no offset correction (default value). Note that while the offset calibration register value can correct offsets ranging from –FS to +FS (as Table 11 shows), to avoid input overload, the analog inputs cannot exceed 105% full-scale.

Table 11. Offset Calibration Values

OFC REGISTER	FINAL OUTPUT CODE(1)
7FFFFFh	800001h
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000001h
800001h	7FFFFFh

(1) Ideal output code excluding noise and inherent offset error.

FSC[2:0] Registers

The full-scale calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 14. The full-scale calibration value is 24-bit, straight binary, normalized to 1.0 at code 400000h. Table 12 summarizes the scaling of the full-scale register. A register value of 400000h (default value) has no gain correction (gain = 1). Note that while the gain calibration register value corrects gain errors above 1 (gain correction < 1), the full-scale range of the analog inputs cannot exceed 105% full-scale to avoid input overload.

Table 12. Full-Scale Calibration Register Values

FSC REGISTER	GAIN FACTOR
800000h	2.0
400000h	1.0
200000h	0.5
000000h	0

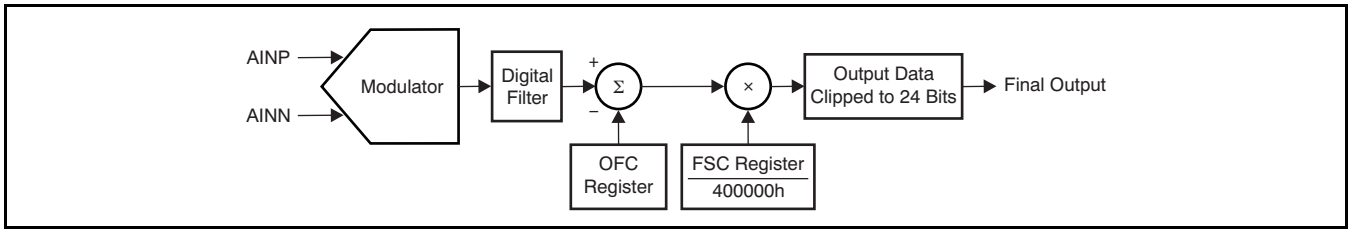


Figure 53. Calibration Block Diagram

Table 13. Offset Calibration Word

REGISTER	BYTE	BIT ORDER							
OFC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
OFC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
OFC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Table 14. Full-Scale Calibration Word

REGISTER	BYTE	BIT ORDER							
FSC0	LSB	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
FSC1	MID	B15	B14	B13	B12	B11	B10	B9	B8
FSC2	MSB	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

CALIBRATION

The ADS1259 has commands to correct for system offset and gain errors. Calibration can be performed at any time the ADS1259 and associated circuitry (such as the input amplifier, external reference, power supplies, etc) have stabilized. Options include calibrating after power-up, after temperature changes, or calibration at regular intervals. To calibrate:

- Set the gate control mode (PULSE bit = 0)
- Start the ADS1259 conversions
- Apply the appropriate input to the ADS1259 (zero or full-scale)
- Allow time for the input to completely settle
- Send the OFSCAL (offset calibration) or GANCAL (full-scale calibration) command, as appropriate
- Wait for calibration to complete as given by the time listed in Table 15. $\overline{DRDY}$ goes low when calibration is complete. The conversion result at this time uses the new offset or full-scale calibration words.

Table 15. Calibration Timing

DATA RATE (SPS)	t_{CAL} CALIBRATION TIME (ms)(1)	
	sinc^1	sinc^2
14400	1.89	2.19
3600	5.43	6.15
1200	14.9	16.7
400	43.2	48.4
60	284	318
50	341	380
16.6	1020	1140
10	1700	1900

(1) f_{CLK} = 7.3728MHz.

Figure 54 shows the calibration timing. During calibration, do not send commands.

Perform offset calibration prior to the gain calibration. The internal full-scale calibration word is bypassed during offset calibration. Do not exceed +105% of full-scale range for gain calibration. Note that the out-of-range threshold is unaffected by gain calibration.

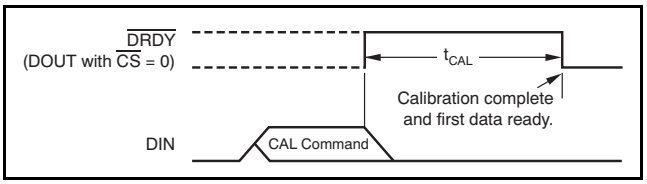


Figure 54. Calibration Timing

SERIAL INTERFACE

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT or three signals, in which case $\overline{CS}$ may be tied low. The interface is used to read conversion data, configure registers, and control the ADS1259 operation.

SERIAL COMMUNICATION

The ADS1259 communications occur by clocking commands into the device (on DIN) and reading register and conversion data (on DOUT). The SCLK input is used to clock the data into and out of the device. $\overline{CS}$ disables the ADS1259 serial port but otherwise does not affect the ADC operation. The communication protocol to the ADS1259 is half-duplex. That is, data are transmitted to and from the device one direction at a time.

Communications to and from the ADS1259 occurs on 8-bit boundaries. If an unintentional SCLK transition should occur (such as from a possible noise spike), the ADS1259 serial port may not respond properly. The port can be reset by one of the following ways:

1. Take $\overline{CS}$ high and then low to reset the interface
2. Hold SCLK low for 2^{16} f_{CLK} cycles to reset the interface
3. Take $\overline{RESET}/\overline{PWDN}$ low and back high to overall reset the device
4. Cycle the power supplies to overall reset the device

CHIP SELECT ($\overline{CS}$)

The chip select ($\overline{CS}$) selects the ADS1259 for SPI communication. To select the device, pull $\overline{CS}$ low. $\overline{CS}$ must remain low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT enters a high-impedance state. If the ADS1259 does not share the serial bus with another device, $\overline{CS}$ may be tied low. Note that $\overline{DRDY}$ remains active when $\overline{CS}$ is high.

SERIAL CLOCK (SCLK)

The serial clock (SCLK) is a Schmitt-triggered input used to clock data into and out of the ADS1259. Even though the input is relatively noise immune, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for 2^{16} f_{CLK} periods, the serial interface resets and the next communication cycle can be started. The timeout can be used to recover communication when the serial interface is interrupted. The SPI timeout is enabled by register bit SPI. When the serial interface is idle, hold SCLK low.

DATA INPUT (DIN)

DIN is the input data pin and is used with SCLK to send data to the ADS1259 (opcode commands and register data). The device latches input data on the falling edge of SCLK.

DATA OUTPUT (DOUT)

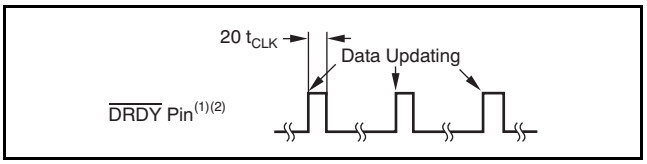
DOUT is the output data pin and is used with SCLK to read conversion and register data from the ADS1259. In addition to providing data output, in RDATAC mode DOUT indicates when data are ready. Data are ready when DOUT transitions low. In this manner, DOUT functions the same as $\overline{DRDY}$ (with $\overline{CS}$ = 0), as shown in Figure 55. When reading data, the data are shifted out on the rising edge of SCLK. DOUT is in a 3-state condition when $\overline{CS}$ is high.

DATA READY ($\overline{DRDY}$)

$\overline{DRDY}$ is an output that indicates when conversion data are available for reading (falling edge active). $\overline{DRDY}$ is asserted on an output pin and also a register bit. To poll the $\overline{DRDY}$ register bit, set the stop read data continuous mode and then read the CONFIG2 register. When the $\overline{DRDY}$ bit is low, data can be read. The data read operation must complete within 20 f_{CLK} cycles of the next $\overline{DRDY}$ falling edge. After power-on or after reset, $\overline{DRDY}$ defaults high.

When reading data in Gate Control mode, $\overline{DRDY}$ is reset high on the first SCLK rising edge. If data are not retrieved, $\overline{DRDY}$ pulses high during the new data update time, as shown in Figure 55. Do not retrieve data during this time as the data are invalid.

In Pulse Control mode, $\overline{DRDY}$ remains low until a new conversion is started. The previous conversion data may be read 20 t_{CLK} prior to the $\overline{DRDY}$ falling edge.



(1) DOUT functions in the same manner as the $\overline{DRDY}$ pin if $\overline{CS}$ is low and in the RDATAC mode.

(2) The $\overline{DRDY}$ bit functions in the same manner as the $\overline{DRDY}$ pin (SDATAC mode only).

Figure 55. $\overline{DRDY}$ and DOUT With No Data Retrieval

DATA FORMAT

The ADS1259 outputs 24 bits of conversion data in binary twos complement format, MSB first. The data LSB has a weight of $V_{REF}/(2^{23} - 1)$. A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale. Table 16 summarizes the ideal output codes for different input signals.

Table 16. Ideal Output Code versus Input Signal

DIFFERENTIAL INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
≥ V_{REF}	7FFFFFh
$\frac{+V_{REF}}{(2^{23} - 1)}$	000001h
0	000000h
$\frac{-V_{REF}}{(2^{23} - 1)}$	FFFFFFh
$\leq -V_{REF}\left(\frac{2^{23}}{2^{23} - 1}\right)$	800000h

(1) Excludes effects of noise, linearity, offset, and gain errors.

DATA INTEGRITY

Data readback integrity is augmented by a checksum byte and redundant data read capability. The checksum byte is the sum of three data conversion bytes, offset by 9Bh. Additionally, the data conversion bytes may be read multiple times by continuing to shift data past the initial read of 24 bits (32 bits if checksum is enabled).

DATA CHECKSUM BYTE AND FLAG BIT

An optional checksum byte can be appended to the conversion data bytes. The checksum makes the data word length four bytes in length instead of three. The checksum byte is enabled by the register bit CHKSUM. The checksum itself is the least significant byte sum of the three conversion data bytes, offset by 9Bh. Note that the checksum byte option only applies to the readback conversion data, not to register data. The checksum is either seven bits or eight bits, depending if the FLAG register bit is enabled. If the FLAG bit is enabled the checksum is seven bits, with bit 7 replaced by the out-of-range flag. Figure 56 and Table 17 describe the combinations of the FLAG and CHKSUM register bits.

Checksum = MSB data byte + Mid data byte + LSB data byte + 9Bh.

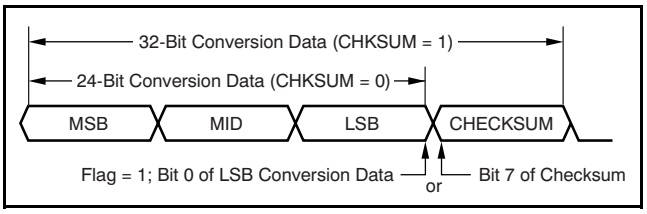


Figure 56. Checksum Byte and Out-of-Range Flag

Table 17. Checksum Byte and Over-Range Flag

FLAG REGISTER BIT	*CHKSUM* REGISTER BIT	DESCRIPTION
0	0	No checksum byte, no out-of-range flag
0	1	8-bit checksum byte, no out-of-range flag
1	0	No checksum byte, out-of-range flag replaces LSB (bit 0) of conversion data
1	1	7-bit checksum byte, out-of-range replaces MSB (bit 7) of checksum byte.

DATA RETRIEVAL

New conversion data are available when $\overline{DRDY}$ goes low. Read the data within 20 f_{CLK} cycles of the next $\overline{DRDY}$ falling edge or the data are incorrect. Do not read data during this interval. The conversion data may be read in two ways: Data Read in Continuous mode and Data Read in Stop Continuous mode.

Data Read Operation in Continuous Mode

In Read Data Continuous mode the conversion data may be shifted out directly without the need of the data read command. When $\overline{DRDY}$ (and DOUT, if $\overline{CS}$ is low) assert low, the conversion data are ready. The data are shifted out on DOUT on the rising edges of SCLK, with the most significant bit (MSB) clocked out first. In Gate Convert Mode, $\overline{DRDY}$ returns to high on the first falling edge of SCLK. In Pulse Convert mode, $\overline{DRDY}$ remains low until a new conversion starts.

As shown in Figure 58, the conversion data consist of three or four bytes (data MSB first), depending on whether the checksum byte is included. The data may be read multiple times by continuing to shift the data. The data read operation must be completed with 20 f_{CLK} cycles of next $\overline{DRDY}$ falling edge.

The Read Data Continuous mode is cancelled by sending the Stop Read Data Continuous command (SDATAC). This operation occurs simultaneously with ADC conversion data on DOUT which can be ignored. Once the SDATAC command is sent, other commands may be sent to the ADS1259. Observe the SCLK and DRDY timing requirements, when reading data in this mode, as shown in Figure 57 and Table 18.

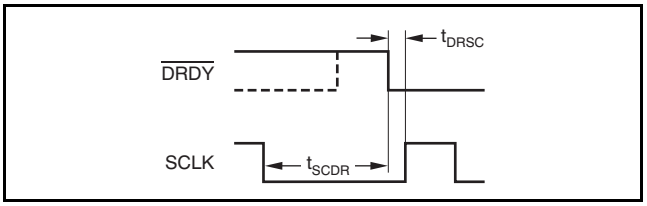
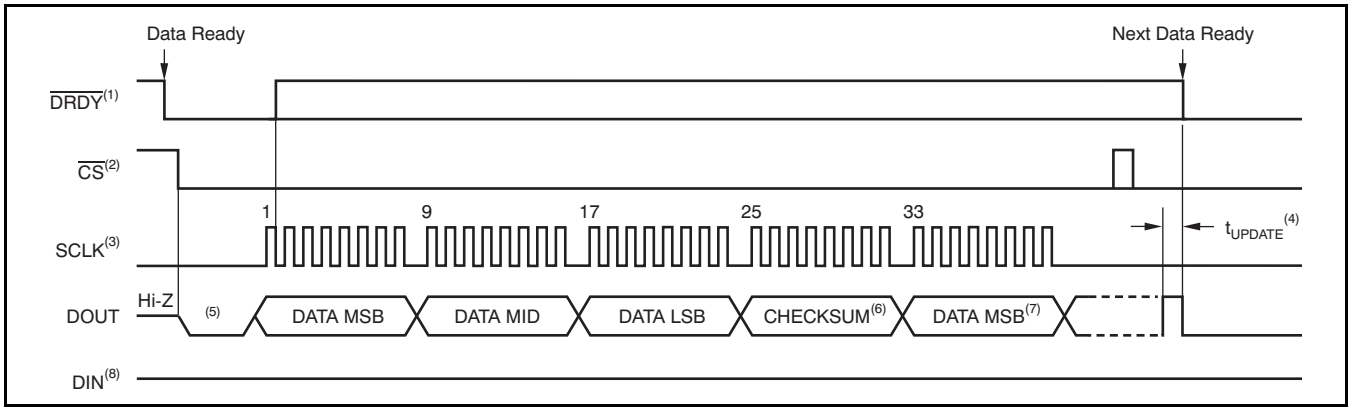


Figure 57. SCLK to $\overline{DRDY}$ Timing

Table 18. SCLK and $\overline{DRDY}$ Timing Characteristics for Figure 57

SYMBOL	DESCRIPTION	MIN	UNIT
t_{SCDR}(1)	SCLK low before $\overline{DRDY}$ low(1)	20	t_{CLK}
t_{DRSC}(1)	$\overline{DRDY}$ falling edge to SCLK rising edge(1)	40	ns

(1) These requirements apply only to reading conversion data in RDATAC mode.



(1) In Gate Convert Conversion mode, $\overline{DRDY}$ returns to high on the first falling edge of SCLK. In Pulse Convert mode, $\overline{DRDY}$ remains low until the next conversion is started.

(2) $\overline{CS}$ may be held low. If $\overline{CS}$ is low, DOUT asserts low with $\overline{DRDY}$.

(3) Data are updated on the rising edge of SCLK. DOUT is low until the first rising edge of SCLK.

(4) $t_{UPDATE} = 20/f_{CLK}$. Do not read data during this time.

(5) During this interval, DOUT follows $\overline{DRDY}$.

(6) Optional data checksum byte.

(7) Optional repeat of previous conversion data.

(8) Hold DIN low, except for transmission of the SDATAC (STOP Read Data Continuous command).

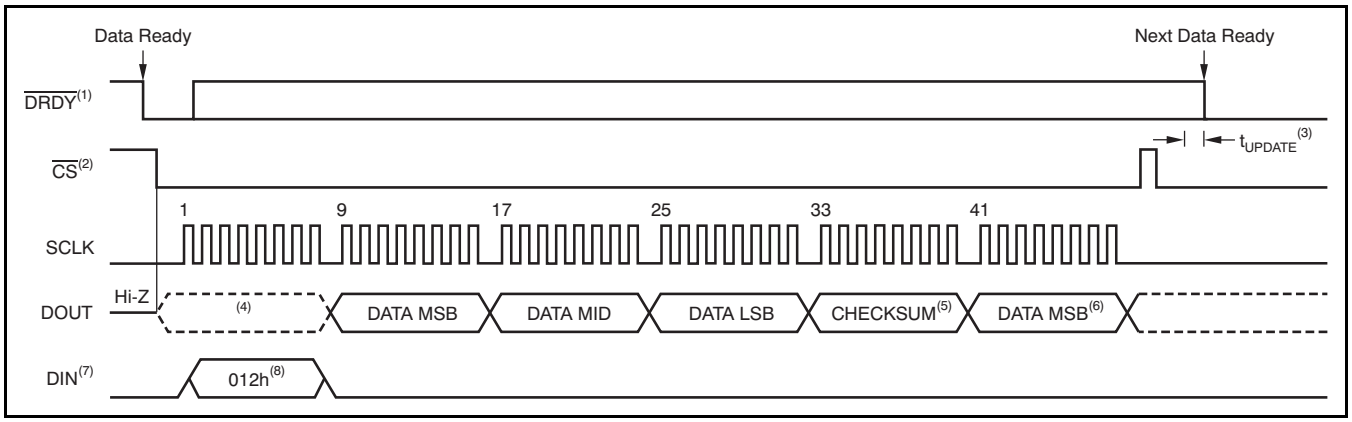
Figure 58. Data Read Operation in Continuous Mode

Data Read Operation in Stop Continuous Mode

In Stop Read Data Continuous mode, a read data command (RDATA) must be sent for each new data read operation. New conversion data are ready when $\overline{DRDY}$ falls low or the $\overline{DRDY}$ register bit transitions low. The data read operation may then occur. The read data command must be sent at least 20 f_{CLK} cycles before the $\overline{DRDY}$ falling edge or the data are incorrect. Do not the read data command during this time.

As shown in Figure 59, after sending the RDATA command the data are shifted out on DOUT on the rising edges of SCLK. The MSB is clocked out on the first rising edge of SCLK. In Gate Control mode, $\overline{DRDY}$ returns to high on the first falling edge of SCLK. In Pulse Control mode, $\overline{DRDY}$ remains low until a new conversion is started.

The conversion data consist of three or four bytes (MSB first), depending on whether the checksum byte is included. The data may be read multiple times by continuing to shift the data.



(1) In Gate Control mode, $\overline{DRDY}$ returns to high on the first falling edge of SCLK. In Pulse Control mode, $\overline{DRDY}$ remains low until the next conversion is started. The $\overline{DRDY}$ pin or $\overline{DRDY}$ register bit can also be polled to determine when data are ready.

(2) $\overline{CS}$ may be held low.

(3) $t_{UPDATE} = 20/f_{CLK}$. Do not issue the Read Data opcode during this time.

(4) During this interval, DOUT does not follow $\overline{DRDY}$ (stop continuous mode).

(5) Optional conversion data checksum.

(6) Optional repeat of previous conversion data.

(7) DIN data are latched on the falling edge of SCLK. Data are output on the rising edges of SCLK.

(8) Read Data command = 012h.

Figure 59. Data Read Operation in STOP Continuous Mode

REGISTER MAP

The operation of the ADS1259 is controlled through a set of registers. Collectively, the registers contain all the information needed to configure the part, such as data rate, calibration, etc. Table 19 shows the register map.

Table 19. Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0h	CONFIG0	10XX0101b	1	0	ID1	ID0	0	RBIAS	0	SPI
1h	CONFIG1	00001000b	FLAG	CHKSUM	0	SINC2	EXTREF	DELAY2	DELAY1	DELAY0
2h	CONFIG2	XX000000b	$\overline{\text{DRDY}}$	EXTCLK	SYNCOUT	PULSE	0	DR2	DR1	DR0
3h	OFC0	00000000b	OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
4h	OFC1	00000000b	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
5h	OFC2	00000000b	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
6h	FSC0	00000000b	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
7h	FSC1	00000000b	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
8h	FSC2	01000000b	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

CONFIG0: CONFIGURATION REGISTER 0 (Address = 0h)

7	6	5	4	3	2	1	0
1	0	ID1	ID0	0	RBIAS	0	SPI

Reset value = 10XX0101b.

Bit 7 **Reserved (read-only)**

Always returns '1'.

Bit 6 **Reserved (read-only)**

Always returns '0'.

Bits 5-4 **ID[1:0]: Factory-programmed identification bits (read-only)**

(Note that these bits may change without notification.)

Bit 3 **Reserved**

Always write '0'.

Bit 2 **RBIAS: Internal reference bias**

0 = Internal reference bias disabled
1 = Internal reference bias enabled (default)

Bit 1 **Reserved**

Always write '0'.

Bit 0 **SPI: SCLK timeout of SPI interface**

0 = SPI timeout disabled
1 = SPI timeout enabled (default), when SCLK is held low for 2^{16} clock cycles

CONFIG1: CONFIGURATION REGISTER 1 (Address = 1h)

7	6	5	4	3	2	1	0
FLAG	CHKSUM	0	SINC2	EXTREF	DELAY2	DELAY1	DELAY0

Reset value = 00001000b.

Bit 7 **FLAG: Out-of-range flag**

0 = Disabled (default)
1 = Enabled: replaces bit 24 (LSB) of the conversion data with the out-of-range bit; if the CHKSUM byte is enabled, bit 7 of the checksum byte

Bit 6 **CHKSUM: Checksum**

0 = Disabled (default)
1 = Conversion data checksum byte included in readback

Bit 5 **Reserved**

Always write '0'.

Bit 4 **SINC2: Digital filter mode**

0 = $sinc^1$ filter (default)
1 = $sinc^2$ filter

Bit 3 **EXTREF: Reference select**

0 = Internal
1 = External (default)

Bits 2-0 **DELAY[2:0]: START conversion delay**

000 = No delay (default)
001 = 64 t_{CLK}
010 = 128 t_{CLK}
011 = 256 t_{CLK}
100 = 512 t_{CLK}
101 = 1024 t_{CLK}
110 = 2048 t_{CLK}
111 = 4096 t_{CLK}

CONFIG2: CONFIGURATION REGISTER 2 (Address = 2h)

7	6	5	4	3	2	1	0
$\overline{\text{DRDY}}$	EXTCLK	SYNCOUT	PULSE	0	DR2	DR1	DR0

Reset value = XX000000b.

Bit 7 **$\overline{\text{DRDY}}$: Data ready (read-only)**

This bit duplicates the state of the $\overline{\text{DRDY}}$ pin. Poll this bit to indicate that data are ready. When $\overline{\text{DRDY}}$ is low, data are ready.

Bit 6 **EXTCLK: Clock source (read-only)**

0 = Device clock source is internal oscillator
1 = Device clock source is external clock
Note that the ADS1259 selects the clock source automatically.

Bit 5 **SYNCOUT: SYNCOUT clock enable**

0 = SYNCOUT disabled (default)
1 = SYNCOUT enabled
Note that if disabled, the output is driven low.

Bit 4 **PULSE: Conversion Control mode select**

0 = Gate Control mode (default)
1 = Pulse Control mode

Bit 3 **Reserved**

Always write '0'

Bits 2-0 **DR[2:0] Data rate setting**

000 = 10SPS (default)
001 = 16.6SPS
010 = 50SPS
011 = 60SPS
100 = 400SPS
101 = 1200SPS
110 = 3600SPS
111 = 14400SPS
NOTE: f_{CLK} = 7.3728MHz

OFC0: OFFSET CALIBRATION BYTE 0, LEAST SIGNIFICANT BYTE (Address = 3h)

7	6	5	4	3	2	1	0
OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00

Reset value = 00000000b.

OFC1: OFFSET CALIBRATION BYTE 1 (Address = 4h)

7	6	5	4	3	2	1	0
OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08

Reset value = 00000000b.

OFC2: OFFSET CALIBRATION BYTE 2, MOST SIGNIFICANT BYTE (Address = 5h)

7	6	5	4	3	2	1	0
OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16

Reset value = 00000000b.

FSC0: FULL-SCALE CALIBRATION BYTE 0, LEAST SIGNIFICANT BYTE (Address = 6h)

7	6	5	4	3	2	1	0
FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00

Reset value = 00000000b.

FSC1: FULL-SCALE CALIBRATION BYTE 1 (Address = 7h)

7	6	5	4	3	2	1	0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08

Reset value = 00000000b.

FSC2: FULL-SCALE CALIBRATION BYTE 2, MOST SIGNIFICANT BYTE (Address = 8h)

7	6	5	4	3	2	1	0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

Reset value = 01000000b.

COMMAND DEFINITIONS

The commands summarized in Table 20 control and configure the operation of the ADS1259. The commands are stand-alone, except for the register read and register write operations which require a second command byte plus data. $\overline{CS}$ can be taken high or held low between opcode commands but must stay low for the entire command operation. Note that the Read Data Continuous mode must be cancelled by the Stop Read Data Continuous mode opcode (SDATAC) before sending further commands.

Table 20. Command Definitions(1)

COMMAND	TYPE	DESCRIPTION	FIRST OPCODE BYTE	SECOND OPCODE BYTE
WAKEUP	Control	Wake up from SLEEP mode	0000 001x (02h or 03h)(2)	
SLEEP	Control	Begin SLEEP mode	0000 010x (04h or 05h)(2)	
RESET	Control	Reset to power-up values	0000 011x (06h or 07h)(2)	
START	Control	START conversion	0000 100x (08h or 09h)(2)	
STOP	Control	STOP conversion	0000 101x (0Ah or 0Bh)(2)	
RDATAC	Control	Set Read Data Continuous mode	0001 0000 (10h)	
SDATAC	Control	Stop Read Data Continuous mode	0001 0001 (11h)	
RDATA	Data	Read data by opcode	0001 001x (12h or 13h)(2)	
RREG	Register	Read *nnnn* register at address *rrrr*	0010 *rrrr* (20h + 0000 *rrrr*)	0000 *nnnn* (00h + *nnnn*)
WREG	Register	Write *nnnn* register at address *rrrr*	0100 *rrrr* (40h + 0000 *rrrr*)	0000 *nnnn* (00h + *nnnn*)
OFSCAL	Calibration	Offset calibration	0001 1000 (18h)	
GANCAL	Calibration	Gain calibration	0001 1001 (19h)	

(1) *nnnn* = number of registers to be read/written – 1. For example, to read/write 3 registers, set *nnnn* = 2 (0010).
rrrr = starting register address for read/write opcodes.
(2) These commands are decoded on the seventh bit of the opcode. The eighth bit is a *don't care* bit. All other commands are decoded on the eighth bit.

WAKEUP: Exit SLEEP Mode

Description: This command exits the low-power SLEEP mode; see the *SLEEP Mode* section.

SLEEP: Enter SLEEP Mode

Description: This command enters the low-power SLEEP mode. See the *SLEEP Mode* section.

RESET: Reset Registers to Default Values

Description: This command resets the digital filter cycle and returns all register settings to the default values.

START: Start Conversions

Description: This command starts data conversions. If PULSE bit = 1, then a single conversion is performed. If PULSE bit = 0, then conversions continue until the STOP command is sent. Tie the START pin low to control conversions by command.

STOP: Stop Conversions

Description: This command stops conversions. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. See the *Conversion Control* section. Tie the START pin low to control conversions by command.

RDATAC: Read Data Continuous

Description: This command enables the Read Data Continuous mode (default). See the *Read Data Continuous Mode* section for details. Disable this mode with the SDATAC command before sending other commands.

SDATAC: Stop Read Data Continuous

Description: This command cancels the Read Data Continuous mode.

RDATA: Read Data

Description: Issue this command opcode after $\overline{\text{DRDY}}$ goes low to read the conversion result (in Stop Read Data Continuous mode). See the *Read Data Mode* section for more details.

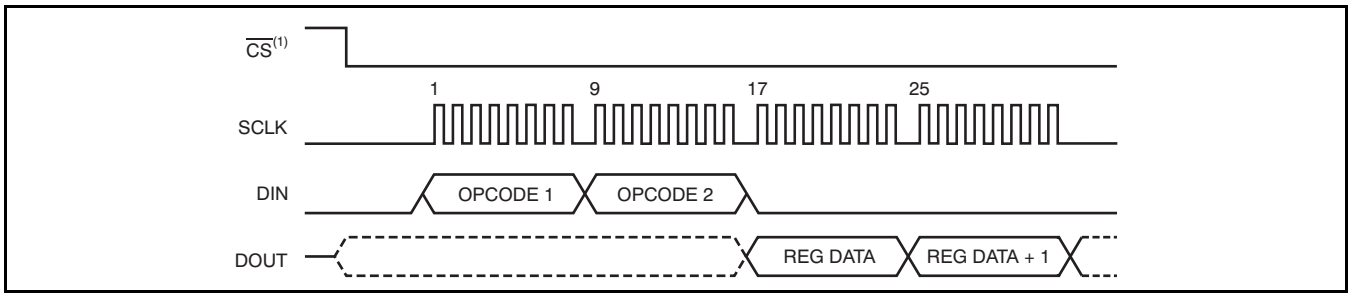
RREG: Read from Registers

Description: These opcode bytes read register data. The Register Read command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to read – 1.

First opcode byte: 0010 *rrrr*, where *rrrr* is the starting register address.

Second opcode byte: 0000 *nnnn*, where *nnnn* is the number of registers to read.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register.



(1) $\overline{\text{CS}}$ may be tied low.

Figure 60. RREG Command Example: Read Two Registers Starting from Register 00h (CONFIG0) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

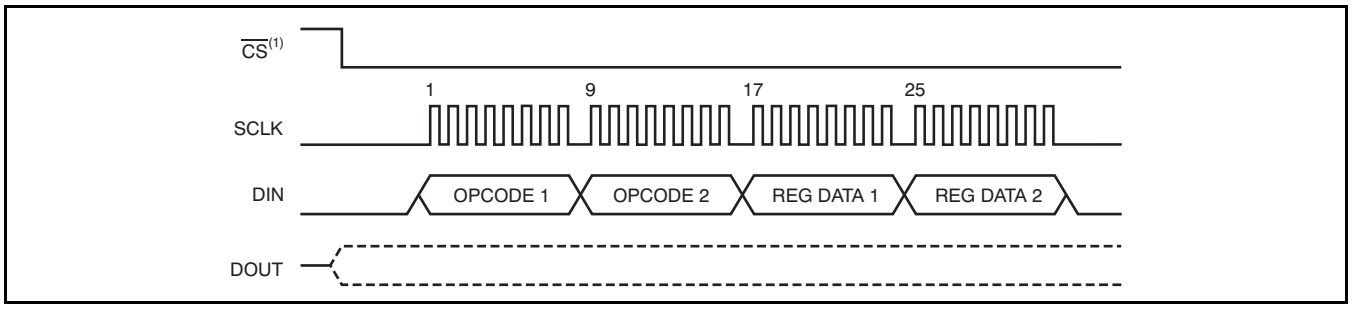
WREG: Write to Register

Description: These two opcode bytes write register data. The Register Write command is a two-byte opcode followed by the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to write – 1.

First opcode byte: 0100 *rrrr*, where *rrrr* is the starting register address.

Second opcode byte: 0000 *nnnn*, where *nnnn* is the number of registers to write

After the opcode bytes, the register data follows (in MSB-first format).



(1) $\overline{CS}$ may be tied low.

Figure 61. WREG Command Example: Write Two Registers Starting from 00h (CONFIG0) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

OFSCAL: Offset Calibration

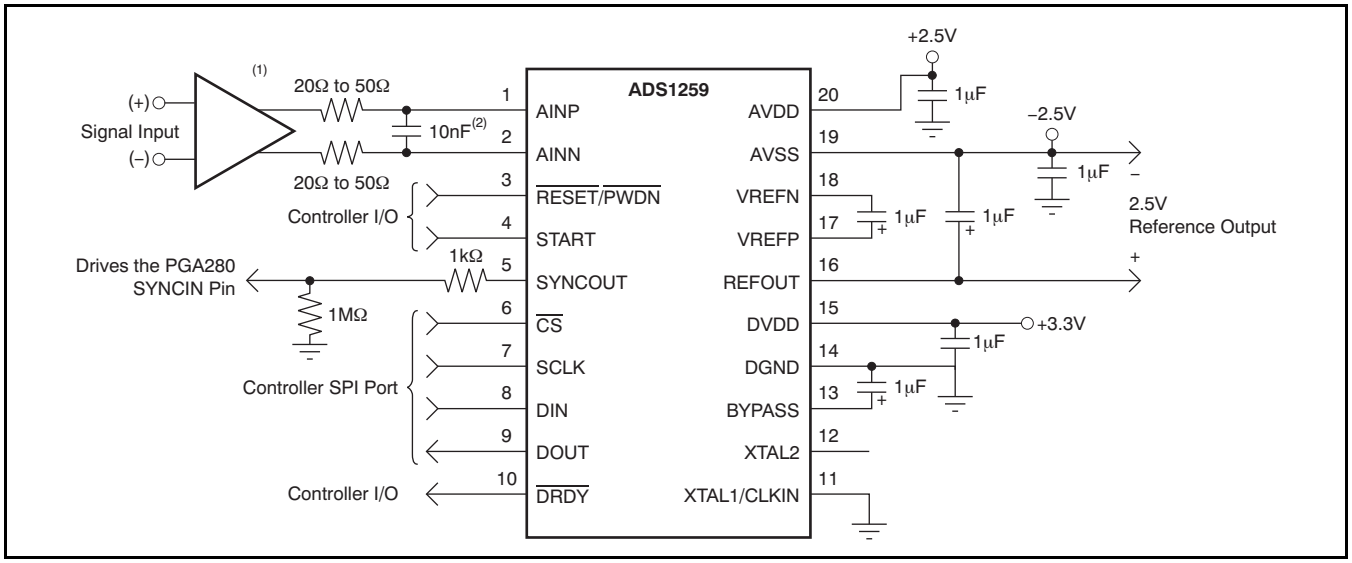
Description: This command performs an offset calibration. Apply a zero signal and allow the input to stabilize before sending the command; see the *Calibration* section for more details.

GANCAL: Gain Calibration

Description: This command performs a gain calibration. Apply a full-scale signal and allow the input to stabilize before sending the command; see the *Calibration* section for more details.

BASIC CONNECTION

The ADS1259 basic connections are shown in Figure 62. The diagram shows the ADS1259 operating with internal oscillator and with internal reference. Dual ±2.5V analog power supplies are also shown. Pins 6-9 are the SPI port connection. The remaining digital I/O pins connect to the controller I/O. Note that the minimum configuration of the digital I/O may include only SCLK, DIN, and DOUT.



(1) It is recommended to buffer the ADS1259 inputs. The output isolation resistors may be incorporated within the amplifier feedback loop.

(2) Low distortion C0G or film capacitor recommended.

Figure 62. ADS1259 Basic Connection Diagram

LAYOUT

Place the input buffer and input decoupling capacitors close to the ADS1259 inputs. The bypass capacitors for power-supply and reference decoupling should also be placed close to the device. In some cases, it may be necessary to use a split ground plane in which digital return currents of external components are routed away from the ADS1259. In this case, connect the grounds at the power supply.

CONFIGURATION GUIDE

Configuration of the ADS1259 involves configuring the device hardware (power supply, I/O pins, etc) and device register settings. The registers are configured by commands sent via the device SPI port.

Power Supplies

The ADS1259 analog section operates either with a single +5V or dual ±2.5V supplies. The digital section operates from +2.7V to +5V. The digital and analog power supplies may be tied together (+5V only).

Reference

Select either the internal reference or an external reference for the ADS1259 (see the *Reference* section). The default is external reference. Figure 62 depicts the internal reference connection.

Clock

Choose the desired clock source (see the *Clock Source* section). Figure 62 depicts the internal clock operation.

SYNCOUT Pin

Connect the SYNCOUT pin to the SYNCIN pin of the PGA280, using a 1kΩ series resistor (placed close to the ADS1259). The 1MΩ pull-down resistor is required when the ADS1259 is in power-down mode.

$\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ Pin

This pin must be high in normal operation. If it is desired to completely power down the device, or to have a hardware reset control, then connect this pin to the controller. If these functions are not needed, tie the pin high. (Note that the device can both be reset and SLEEP mode engaged by commands.)

START Pin

If it is desired to control conversions by pin, connect this line to the controller. Otherwise, this line can be tied high to free-run conversions. The conversions can also be controlled by software commands. In this case, tie the START pin low.

$\overline{\text{DRDY}}$ Pin

$\overline{\text{DRDY}}$ is an output that indicates when data are ready for readback. Note that the DOUT pin (and also the $\overline{\text{DRDY}}$ register bit) indicates when data are ready as well, so $\overline{\text{DRDY}}$ connection to a controller is optional.

$\overline{\text{CS}}$ Pin

If the ADS1259 is a single device connected to the SPI bus, then $\overline{\text{CS}}$ can be tied low. Otherwise, for applications where the ADS1259 shares the bus with another device, $\overline{\text{CS}}$ must be connected.

Miscellaneous Digital I/O

Avoid ringing on the digital inputs and outputs. Resistors in series with the trace driving end helps to reduce ringing by controlling impedances.

SOFTWARE GUIDE

After the power supplies have fully established, allow a minimum of 2^{16} system clocks before beginning communication to the device. The registers can then be configured by commands via the SPI port. The following steps detail a suggested procedure to initialize the ADS1259.

1. Send the SDATAC command <11h>. This command cancels the RDATAC mode. RDATAC mode must be cancelled before the register write commands.
2. Send the register write command. The following example shows the register write as a block of nine bytes, starting at register 0 (CONFIG0).

BYTES	DATA	OPERATION
1, 2	01000000, 00001000	Write register opcode bytes, starting at address 0, 9-byte block
3	00000101	CONFIG0; register data, bias the reference, SPI timeout
4	01010000	CONFIG1; checksum enabled, $sinc^2$ filter selection, internal reference
5	00000011	CONFIG2; Gate Convert mode, 60SPS
6, 7, 8	00000000, 00000000, 00000000	OFC[2:0]; 3 bytes for offset, no offset correction
9, 10, 11	00000000, 00000000, 01000000	FSC[2:0]; 3 bytes for gain, no full-scale correction

3. Optional readback verification of the register data

   READ register command: <20h>, <08>

   The nine bytes of readback data that follow represent the nine register bytes.
4. Take the START pin high or send the START command to start conversions.
5. Optionally, send the RDATAC command <10h>. This permits reading of conversion data without the need of the read data command. Otherwise, the read data opcode must be sent to read each conversion result.
6. When the $\overline{\text{DRDY}}$ pin or the DRDY bit goes low, or when DOUT transitions low, read the data.

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