ACPL-M50L and ACPL-054L

Low Power, 1MBd Digital Optocoupler

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

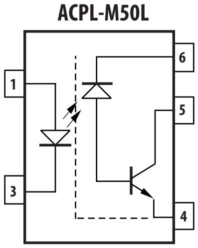
Description

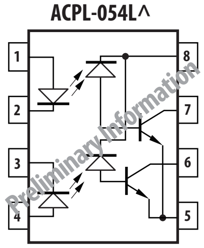
The ACPL-M50L (single-channel) and ACPL-054L (dual-channel) are low power, low-input current, high speed digital optocouplers in a SO-5 and SO-8 footprint respectively.

This digital optocouplers use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The ACPL-M50L/054L have an increased common mode transient immunity of 15kV/μs minimum at V_{CM} = 1500V over a temperature range of -40 to 105°C. The current transfer ratio (CTR) is 140% typical at I_F = 3mA. This digital optocoupler can be use in any TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications.

Functional Diagram





TRUTH TABLE

LED	Vo
ON	LOW
OFF	HIGH

^ Advanced information, may subject to changes.

The connection of a 0.1 μF bypass capacitor between pins 4 and 6 for ACPL-M50L and between pins 5 and 8 for ACPL-054L is recommended.

Features

- Wide supply voltage: 2.7V to 24V V_{CC} Operation
- Low Drive Current: 3mA
- Open-Collector Output
- TTL compatible
- Compact SO-5 (ACPL-M50L) and SO-8 (ACPL-054L) package
- 15 kV/μs High Common-Mode Rejection at V_{CM} = 1500 V
- Guaranteed performance across Temperature Range: -40°C to +105°C
- Low Propagation Delay: 1μA max at 5V
- Worldwide Safety Approval (Pending):
  - UL1577 recognized, 3750Vrms/1min
  - CSA Approval
  - IEC/EN/DIN EN 60747-5-5 Approval

Applications

- Communications Interface
- Digital Signal Isolation
- Micro-controller Interface
- Feedback Elements in Switching Power Supplies
- Digital isolation for A/D, D/A conversion Digital field

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-M50L	-000E	SO-5	X			100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel
ACPL-054L^	-000E	SO-8	X			100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

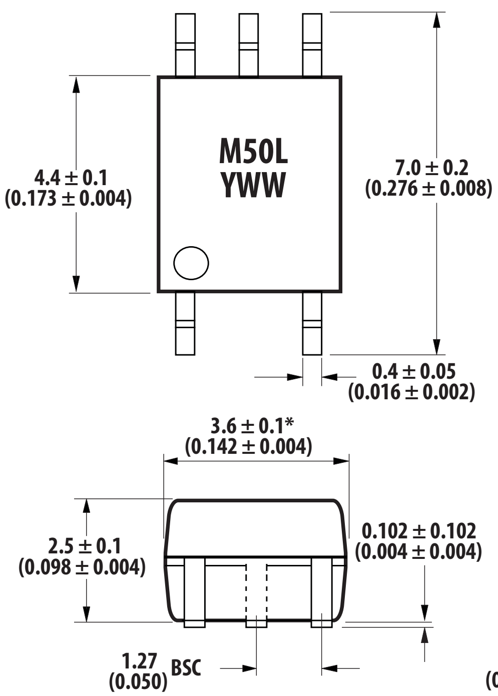
ACPL-M50L-500E to order product of Mini-flat Surface Mount 5-pin package in Tape and Reel packaging with RoHS compliant.

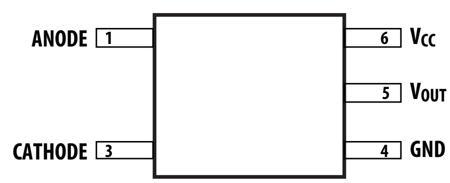
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

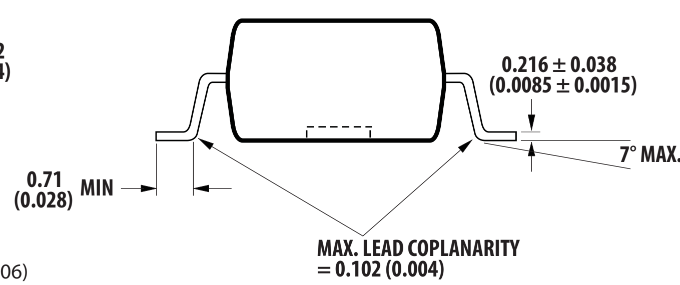
^ Advanced information, may subject to changes.

Package Outline Drawings

ACPL-M50L Small Outline SO-5 Package (JEDEC MO-155)

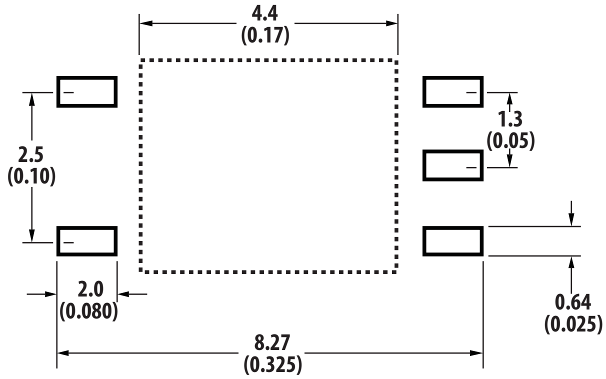






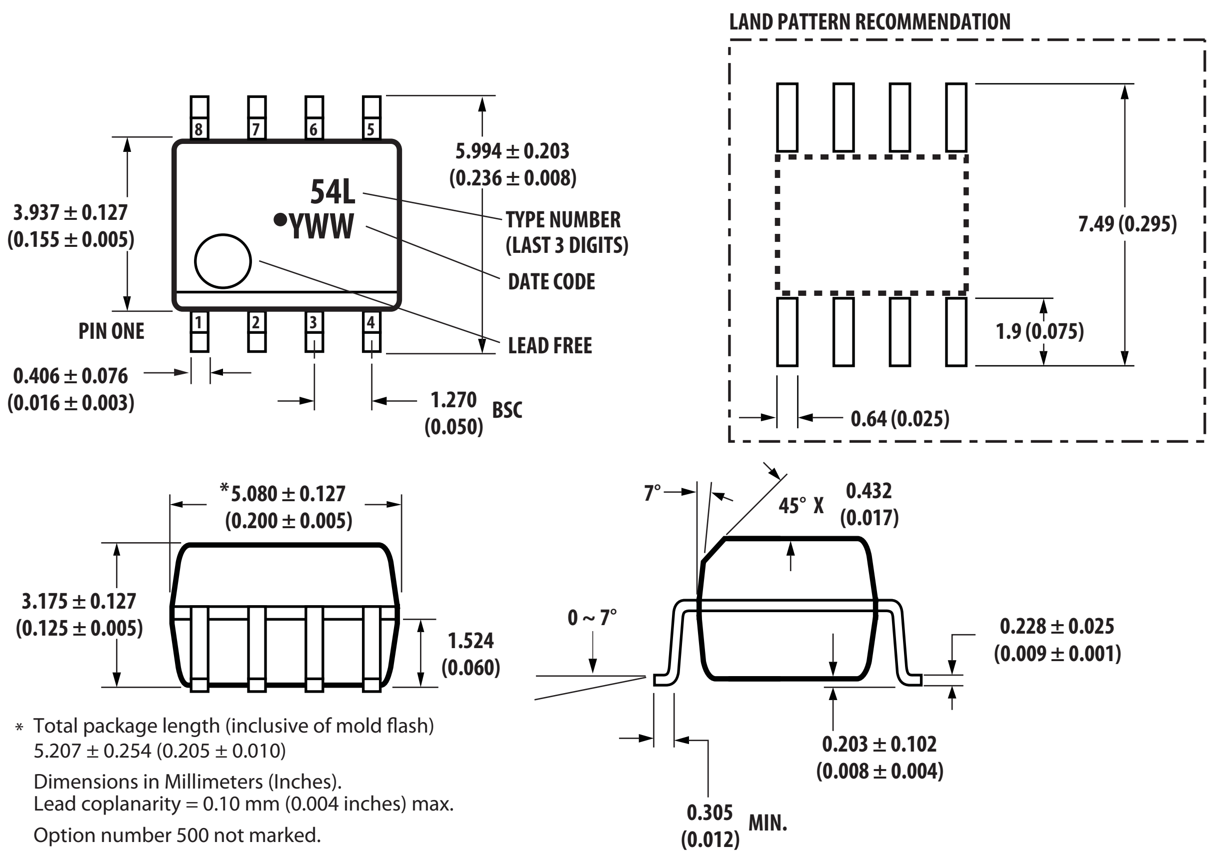
Dimensions in Millimeters (Inches)
* Maximum mold flash on each side is 0.15 mm (0.006)
Note: Floating lead protrusion is 0.15 mm (6 mils) max.

Land Pattern Recommendation



Dimension in Millimeters (Inches)

ACPL-054L (Small Outline S0-8 Package)



* Total package length (inclusive of mold flash)
5.207 ± 0.254 (0.205 ± 0.010)

Dimensions in Millimeters (Inches).
Lead coplanarity = 0.10 mm (0.004 inches) max.

Option number 500 not marked.

Note: Floating lead protrusion is 0.15 mm (6 mils) max.

Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-M50L/054L will be approved by the following organizations:

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS}.

CSA

Approval under CSA Component Acceptance Notice #5.

IEC/EN/DIN EN 60747-5-5 (Option 060E only)

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-M50L	ACPL-054L	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	5	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	5	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics*

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150 Vrms for rated mains voltage ≤ 300 Vrms for rated mains voltage ≤ 600 Vrms		 I – IV I – III I – II	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	560	Vpeak
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	1063	Vpeak
Input to Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	896	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	Vpeak
Safety-limiting values – maximum values allowed in the event of a failure. Case Temperature Input Current Output Power	 T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units
Storage Temperature		T_S	-55	150	°C
Operating Temperature		T_A	-40	105	°C
Lead Soldering Cycle	Temperature			260	°C
	Time			10	s
Average Forward Input Current[1]		$I_{F(avg)}$		20	mA
Peak Forward Input Current[2] (50% duty cycle, 1ms pulse width)		$I_{F(peak)}$		40	mA
Peak Transient Input Current (≤1μs pulse width, 300ps)		$I_{F(trans)}$		1	A
Reversed Input Voltage		V_R		5	V
Input Power Dissipation[3]		P_{IN}		36	mW
Output Power Dissipation [4]		P_O		45	mW
Average Output Current		$I_{O(AVG)}$		8	mA
Peak Output Current		$I_{O(PEAK)}$		16	mA
Supply Voltage		V_{CC}	-0.5	30	V
Output Voltage		V_O	-0.5	24	V
Solder Reflow Temperature Profile			See Package Outline Drawings section		

Notes:
1. Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C.
2. Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C.
3. Derate linearly above 85°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 85°C free-air temperature at a rate of 1.2 mW/°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	2.7	24	V
Input Current, High Level	I_{FH}	3	10	mA
Operating Temperature	T_A	-40	105	°C

Electrical Specifications (DC)

Over recommended operating T_A = -40°C to 105°C, supply voltage (2.7V ≤ V_{CC} ≤ 24V) and unless otherwise specified. All typicals are at T_A=25°C

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions			Fig.
Current Transfer Ratio	CTR [1]	80	140	200	%	T_A=25°C	V_O=0.4V	V_{CC}= 3.3V or 5V I_F= 3mA	2,3
		50			%		V_O=0.5V		
Logic Low Output Voltage	V_{OL}		0.2	0.4	V	T_A=25°C	I_O=3mA	V_{CC}= 3.3V or 5V I_F= 3mA	
			0.2	0.5	V		I_O=2.4mA		
Logic High Output Current	I_{OH}		0.003	0.5	µA	T_A=25°C	V_O=V_{CC}=5.5V	I_F=0mA	4,5
			0.01	1			V_O=V_{CC}=24V		
				80			V_O=V_{CC}=24V		
Logic Low Supply Current	I_{CCL}		36	100	µA		I_F=3mA, V_O=open, V_{CC}=24V		
Logic High Supply Current	I_{CCH}		0.02	2	µA		I_F=0mA, V_O=open, V_{CC}=24V		
Input Forward Voltage	V_F		1.5	1.8	V	T_A=25°C	I_F=3mA		1
			1.5	1.95	V		I_F=3mA		
Input Reversed Breakdown Voltage	BV_R	5			V		I_R=10µA		
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$		-1.6		mV/°C		I_F=3mA		
Input Capacitance	C_{IN}		77		pF		F = 1MHz, V_F = 0		

Notes:

1. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, IF, times 100%.

Switching Specifications

Over recommended operating (T_A = -40°C to 105°C), I_F = 3mA, (2.7V ≤ V_{CC} ≤ 24V), unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions		Fig.
Propagation Delay Time to Logic Low at Output	T_{PHL}		0.2	0.5	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 3.3V, R_L = 1.2kΩ, C_L = 15pF, V_{THHL} = 1.5V	14
			0.2	1	µs			6, 14
			0.22	0.5	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 5.0V, R_L= 1.9kΩ, C_L = 15pF, V_{THHL} = 1.5V	14
			0.22	1	µs			7, 14
			0.33	0.7	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 24V, R_L = 10kΩ, C_L = 15pF, V_{THHL} = 1.5V	14
			0.33	1.3	µs			8, 14
Propagation Delay Time to Logic High at Output	T_{PLH}		0.38	0.8	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 3.3V, R_L = 1.2kΩ, C_L = 15pF, V_{THHL} = 2.0V	14
			0.38	1.2	µs			6, 14
			0.31	0.7	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 5.0V, R_L = 1.9kΩ, C_L = 15pF, V_{THHL} = 2.0V	14
			0.31	1	µs			7, 14
			0.3	0.7	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 24V, R_L = 10kΩ, C_L = 15pF, V_{THHL} = 2.0V	14
			0.3	1	µs			8, 14
Pulse Width Distortion [1]	PWD		0.18	0.8	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 3.3V, R_L = 1.2kΩ, C_L = 15pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	14
			0.18	1.2	µs			14
			0.1	0.7	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 5.0V, R_L = 1.9kΩ, C_L = 15pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	14
			0.1	1	µs			14
			0.1	0.7	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 24V, R_L = 10kΩ, C_L = 15pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	14
			0.1	1	µs			14
Propagation Delay Difference Between Any two Parts [2]	t_{psk}		0.18	0.8	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 3.3V, R_L = 1.2kΩ, C_L = 15pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	
			0.1	0.7	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 5.0V, R_L = 1.9kΩ, C_L = 15pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	
			0.1	0.7	µs	T_A=25°C	Pulse: f = 10kHz, Duty cycle = 50%, I_F = 3mA, V_{CC} = 5.0V, R_L = 1.9kΩ, C_L = 15pF, V_{THHL} = 1.5V, V_{THLH} = 2.0V	
Common Mode Transient Immunity at Logic High Output [3]	$\|CM_H\|$	10	15		kV/µs		V_{CM} = 1500V, I_F = 0mA, T_A = 25°C, (R_L = 1.2kΩ, V_{CC} = 3.3V) or (R_L = 1.9kΩ, V_{CC} = 5V)	15
Common Mode Transient Immunity at Logic Low Output [4]	$\|CM_L\|$	10	15		kV/µs		V_{CM} = 1500V, I_F = 3mA, T_A = 25°C, (R_L = 1.2kΩ, V_{CC} = 3.3V) or (R_L = 1.9kΩ, V_{CC} = 5V)	15

Notes:
1. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
2. The difference between t_{PLH} and t_{PHL} between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
3. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V).
4. Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM} to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).

Package Characteristics

All Typical at $T_A = 25°C$.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage [1,2]	V_{ISO}	3750			V_{rms}	RH ≤ 50%, t = 1 min., $T_A = 25°C$
Input-Output Resistance [1]	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc
Input-Output Capacitance [1]	C_{I-O}		0.6		pF	f = 1 MHz, $T_A = 25°C$
Input-Output Insulation [1]	I_{I-O}			1.0	μA	RH ≤ 45%, t = 5 s V_{I-O} = 3 kVdc, $T_A = 25°C$
Input-Input Insulation Leakage Current [3]	I_{I-I}			0.005	μA	RH ≤ 45%, t = 5 s V_{I-I} = 500Vdc
Input-Input Resistance [3]	R_{I-I}		10^{11}		Ω	
Input-Input Capacitance [3]	C_{I-I}		0.25		pF	f = 1 MHz

Notes:
1. Device considered a two terminal device: pins 1 and 3 shorted together and pins 4, 5 and 6 shorted together for ACPL-M50L, pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together for ACPL-054L.
2. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, I_{I-O} ≤ 5 μA).
3. Measured between pins 1 ad 2 shorted together, and pins 3 and 4 shorted together.

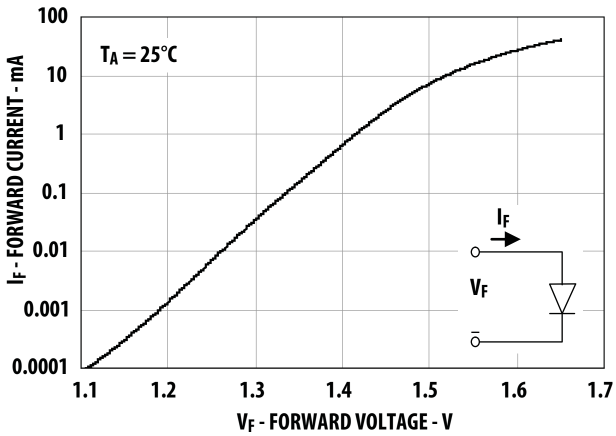


Figure 1. Input Current vs. Forward Voltage

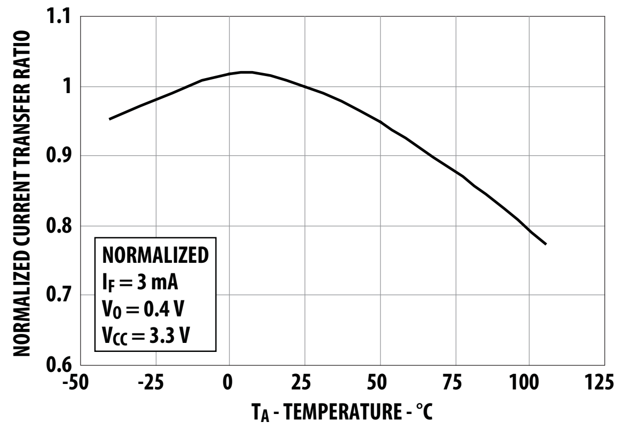


Figure 2. Typical Current Transfer Ratio vs. Temperature

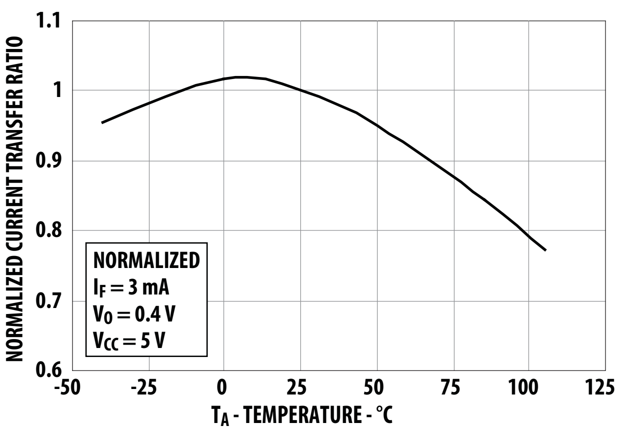


Figure 3. Typical Current Transfer Ratio vs. Temperature

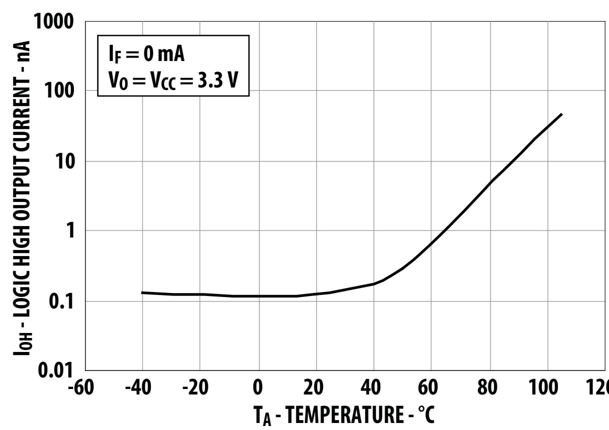


Figure 4. Typical Logic High Output Current vs. Temperature

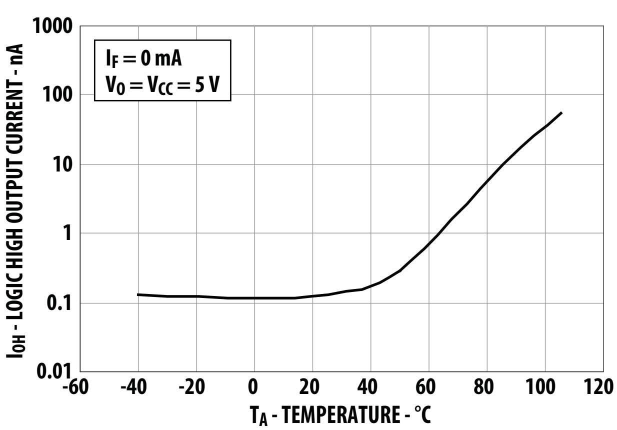


Figure 5. Typical Logic High Output Current vs. Temperature

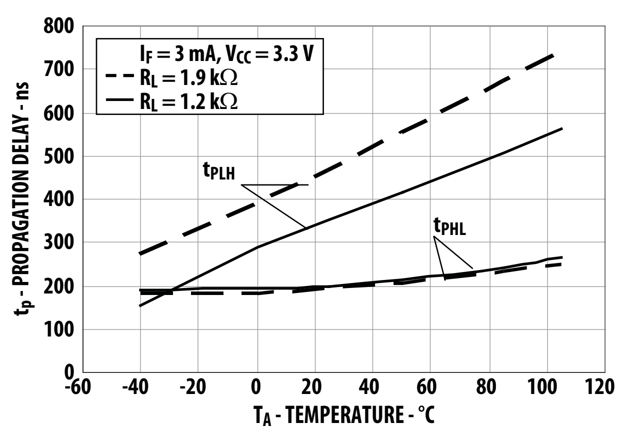


Figure 6. Typical Propagation Delay vs. Temperature

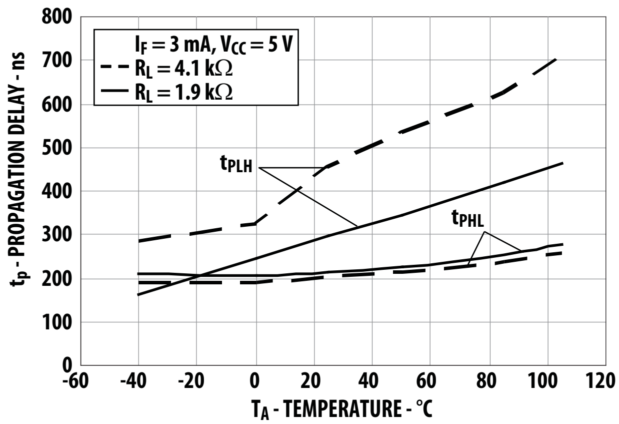


Figure 7. Typical Propagation Delay vs. Temperature

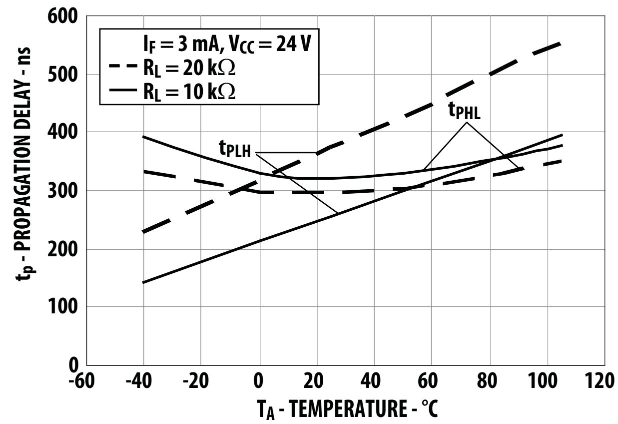


Figure 8. Typical Propagation Delay vs. Temperature

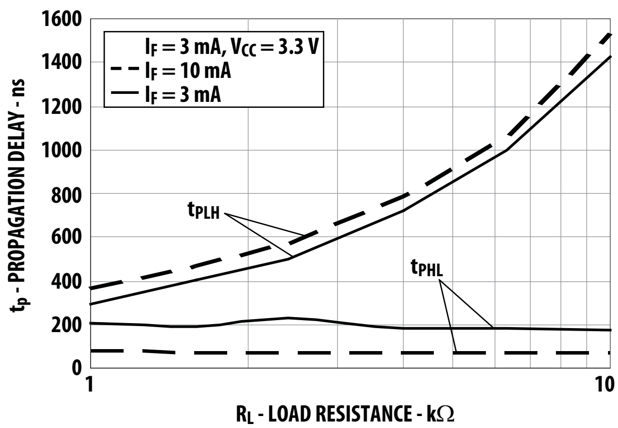


Figure 9. Typical Propagation Delay vs. Load Resistance

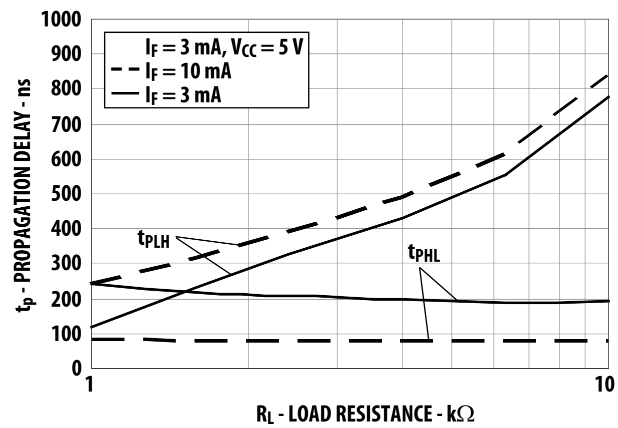


Figure 10. Typical Propagation Delay vs. Load Resistance

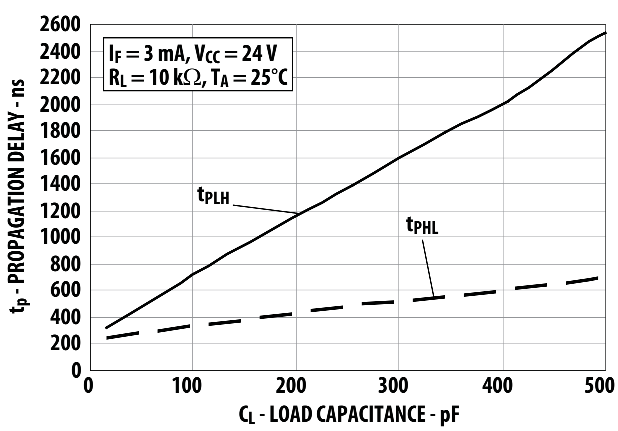


Figure 11. Typical Propagation delay vs. Load Capacitance

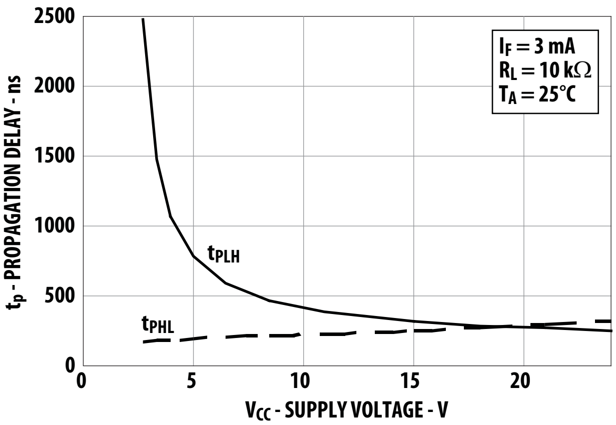


Figure 12. Typical Propagation Delay vs. Supply Voltage

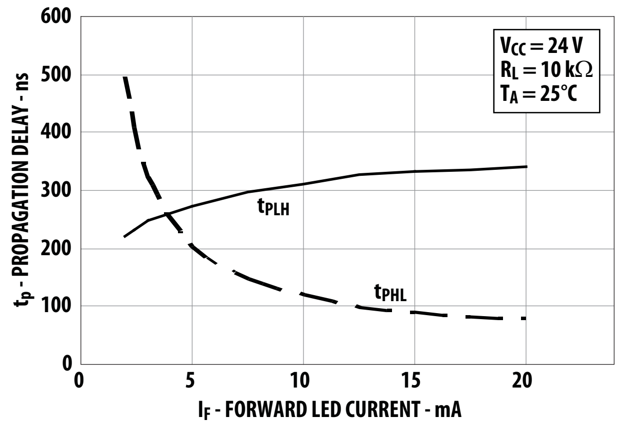


Figure 13. Typical Propagation Delay vs. Supply Voltage

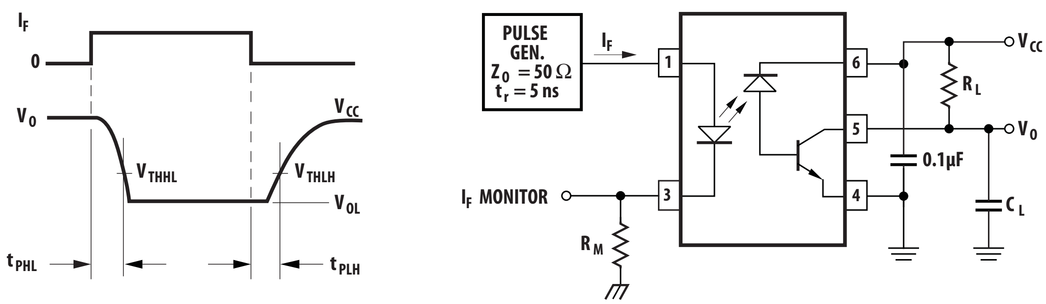


Figure 14. Switching Test Circuits

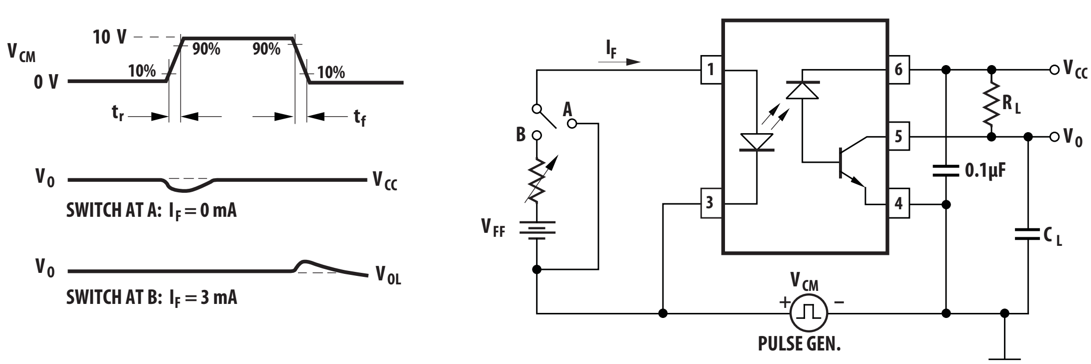


Figure 15. Test Circuit for Transient Immunity and typical waveforms

AV02-2223EN - November 18, 2009