STD95N3LLH6
STU95N3LLH6

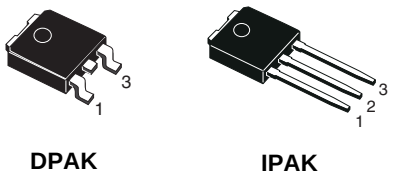
N-channel 30 V, 0.0035 Ω , 80 A, DPAK, IPAK STripFET™ VI DeepGATE™ Power MOSFET

Preliminary Data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STD95N3LLH6	30 V	0.004 Ω	80 A
STU95N3LLH6	30 V	0.0045 Ω	80 A

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses



DPAK IPAK

Application

- Switching applications

Description

This product utilizes the 6th generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure.The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in a standard package, that makes it suitable for the most demanding DC-DC converter applications, where high power density has to be achieved.

Figure 1. Internal schematic diagram

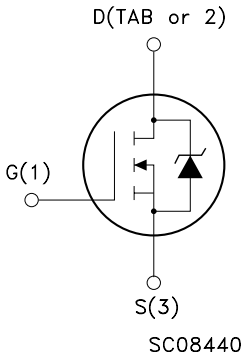


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD95N3LLH6	95N3LLH6	DPAK	Tape and reel
STU95N3LLH6	95N3LLH6	IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D	Drain current (continuous) at T_C = 100 °C	61	A
I_{DM} (2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
	Derating factor	0.47	W/°C
E_{AS} (3)	Single pulse avalanche energy	TBD	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature	175	°C

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting Tj = 25°C, I_D = 40 A, V_{DD} = 25 V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.14	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-case max	100	°C/W
T_j	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 20 V V_{DS} = 20 V,Tc = 125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 40 A SMD version		0.0035	0.004	Ω
		V_{GS} = 10 V, I_D = 40 A		0.004	0.0045	Ω
		V_{GS} = 4.5 V, I_D = 40 A SMD version		0.005	TBD	Ω
		V_{GS} = 4.5 V, I_D = 40 A		0.0055	TBD	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS} = 0		2100 400 170		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 15 V, I_D = 80 A V_{GS} = 4.5 V *(see Figure 3)*		16 TBD TBD		nC nC nC
Q_{gs1} Q_{gs2}	Pre V_{th} gate-to-source charge Post V_{th} gate-to-source charge	V_{DD} = 15 V, I_D = 80 A V_{GS} = 5 V *(see Figure 8)*		TBD TBD		nC nC
R_G	Gate input resistance	f = 1 MHz gate bias Bias = 0 test signal level = 20 mV open drain		TBD		Ω

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 15 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 5 V *(see Figure 2)*		TBD TBD		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 15 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 5 V *(see Figure 2)*		TBD TBD		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)				80 320	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 40 A, V_{GS} = 0			1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80 A, di/dt = 100 A/µs, V_{DD} = 20 V *(see Figure 4)*		TBD TBD TBD		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuit

Figure 2. Switching times test circuit for resistive load

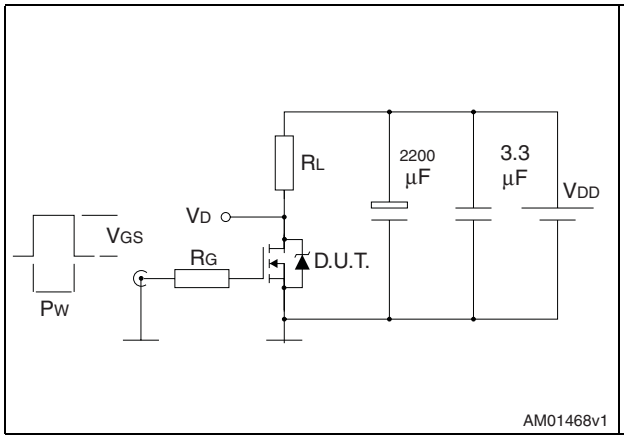


Figure 3. Gate charge test circuit

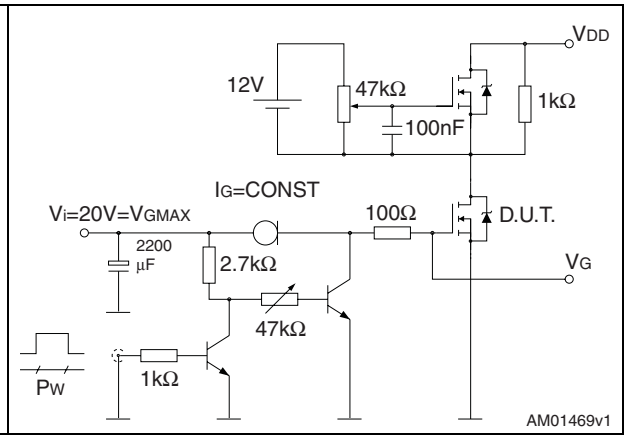


Figure 4. Test circuit for inductive load switching and diode recovery times

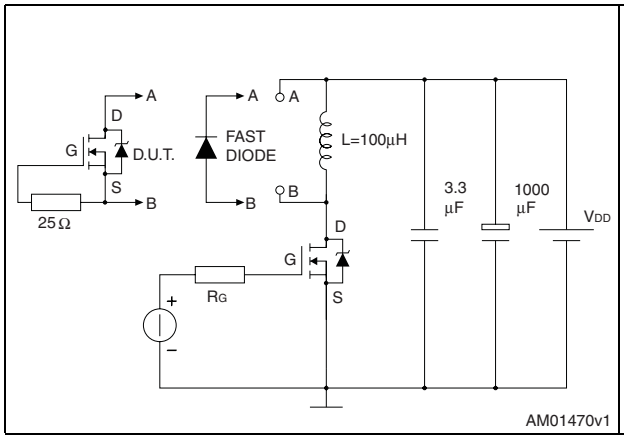


Figure 5. Unclamped Inductive load test circuit

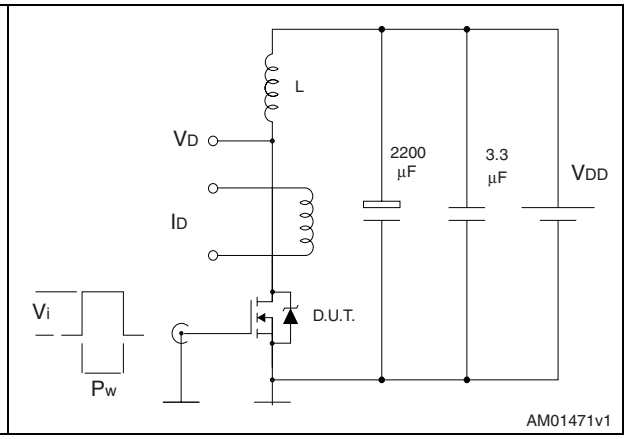


Figure 6. Unclamped inductive waveform

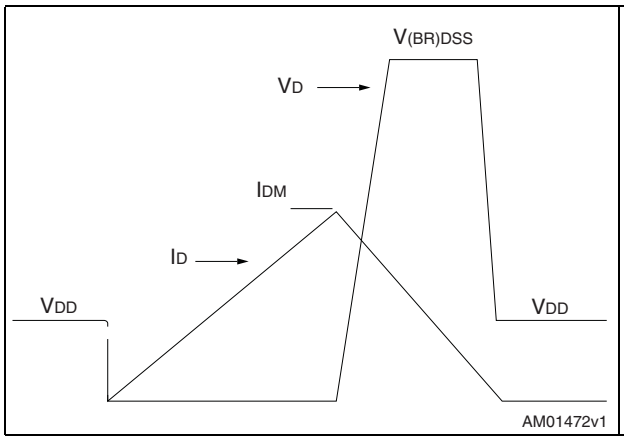


Figure 7. Switching time waveform

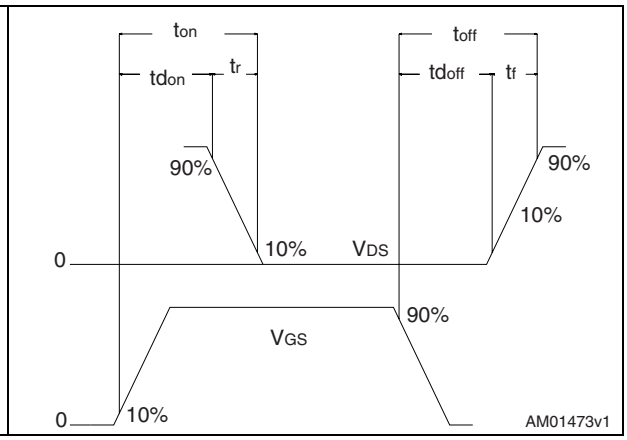
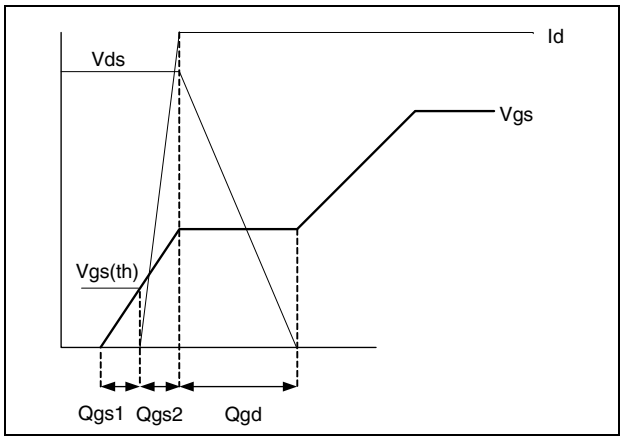


Figure 8. Gate charge waveform

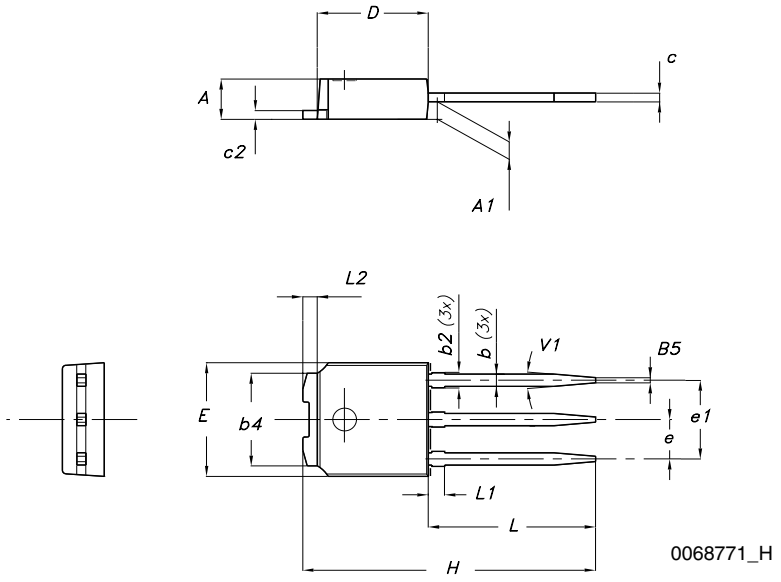


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

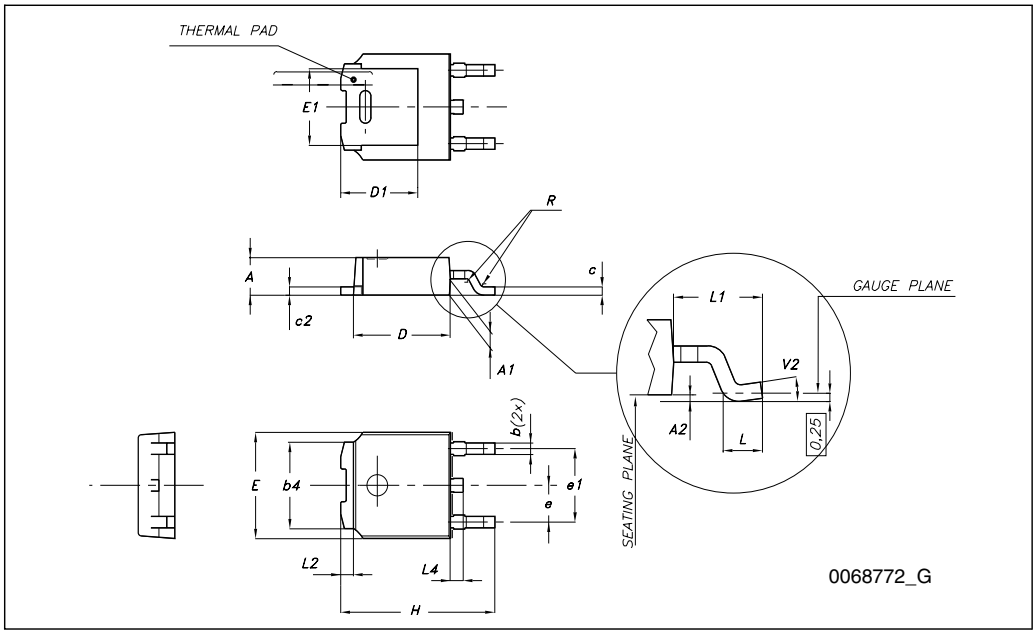
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10 °	



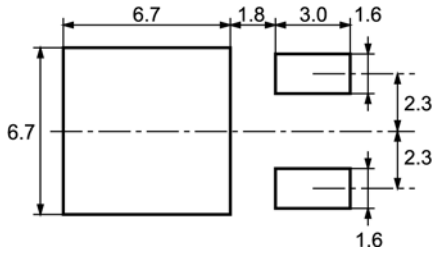
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



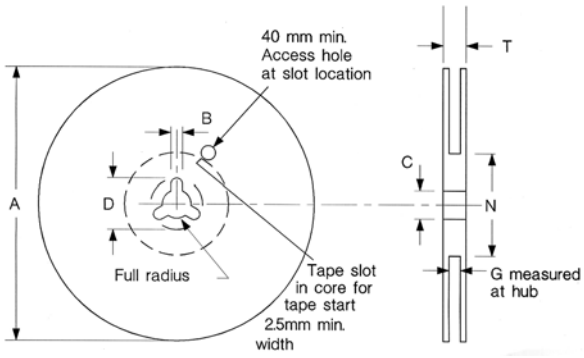
5 Packaging mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



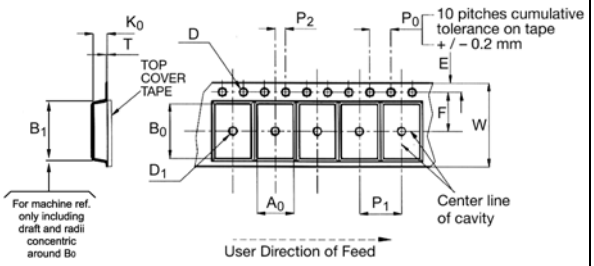
REEL MECHANICAL DATA

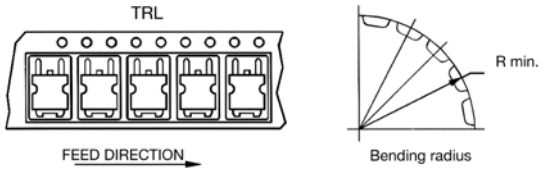
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641





6 Revision history

Table 8. Document revision history

Date	Revision	Changes
01-Dec-2008	1	First release