P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.048 at V_{GS} = - 4.5 V	- 6.5	14
	0.063 at V_{GS} = - 2.5 V	- 5.7	

FEATURES

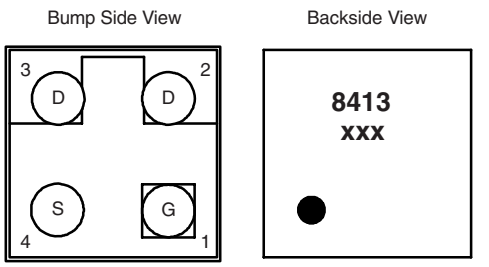
- TrenchFET® Power MOSFET
- New MICRO FOOT® Chipscale Packaging Reduces Footprint Area Profile (0.62 mm) and On-Resistance Per Footprint Area

Pb-free
RoHS COMPLIANT

APPLICATIONS

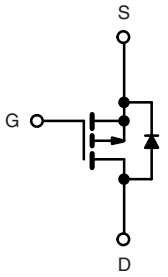
- Load Switch
- Battery Switch
- Charger Switch
- PA Switch

MICRO FOOT



Device Marking: 8413
xxx = Date/Lot Traceability Code

Ordering Information: Si8413DB-T1-E1 (Lead (Pb)-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**5 s**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	- 20		V
Gate-Source Voltage		V_{GS}	± 12		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	- 6.5	- 4.8	A
	T_A = 70 °C		- 5.2	- 3.8	
Pulsed Drain Current		I_{DM}	- 25		
Continuous Source Current (Diode Conduction)[a]		I_S	- 2.5	- 1.3	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	2.77	1.47	W
	T_A = 70 °C		1.77	0.94	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Package Reflow Conditions[b]	VPR		215		
	IR/Convection		220		

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 5 s	R_{thJA}	35	45	°C/W
	Steady State		72	85	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	16	20	

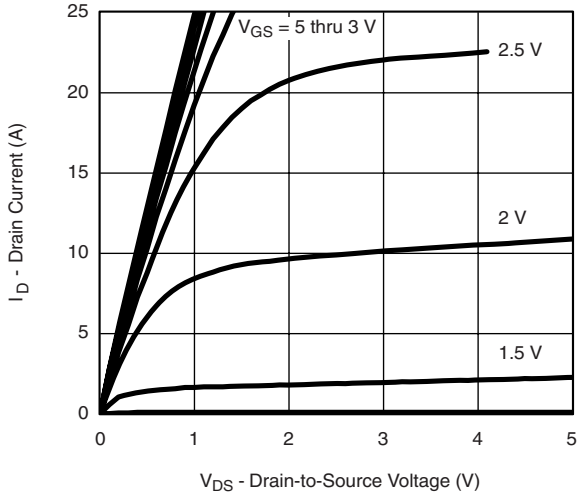
Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. Refer to IPC/JEDEC (J-STD-020A), no manual or hand soldering.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.6		- 1.4	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 70 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 5			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 1 A		0.0393	0.048	Ω
		V_{GS} = - 2.5 V, I_D = - 1 A		0.052	0.063	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 1 A		7.4		S
Diode Forward Voltage[a]	V_{SD}	I_S = - 1 A, V_{GS} = 0 V		- 0.8	- 1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 1 A		14	21	nC
Gate-Source Charge	Q_{gs}			1.7		
Gate-Drain Charge	Q_{gd}			5.1		
Gate Resistance	R_g			18		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		31	50	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			105	160	
Fall Time	t_f			90	135	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = - 1 A, di/dt = 100 A/µs		85	130	

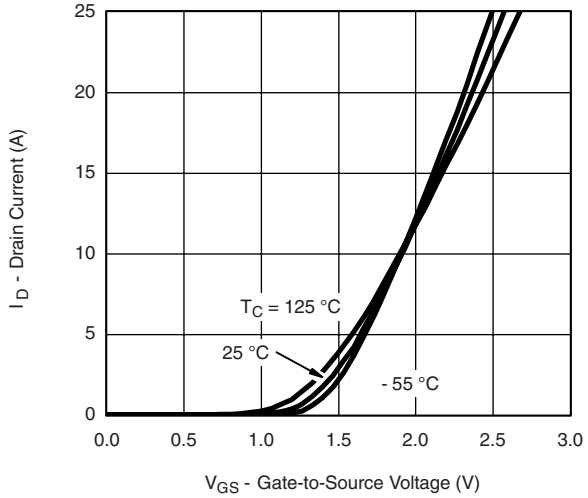
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

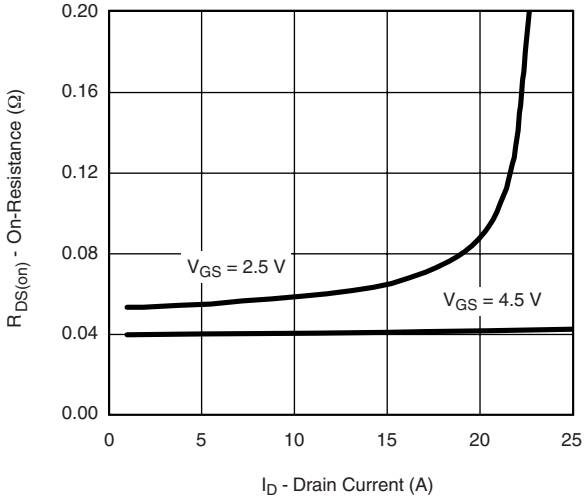


Output Characteristics

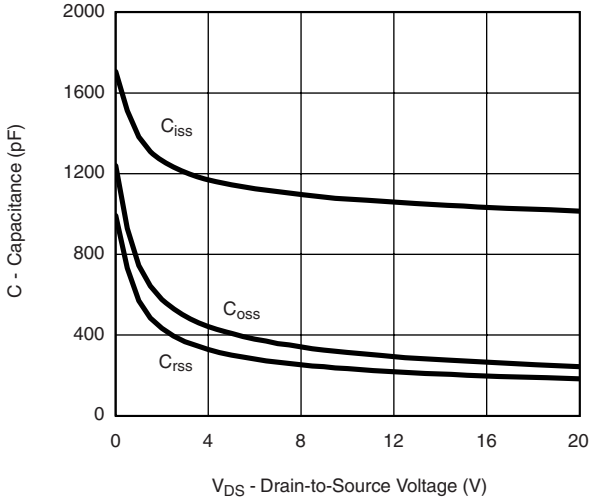


Transfer Characteristics

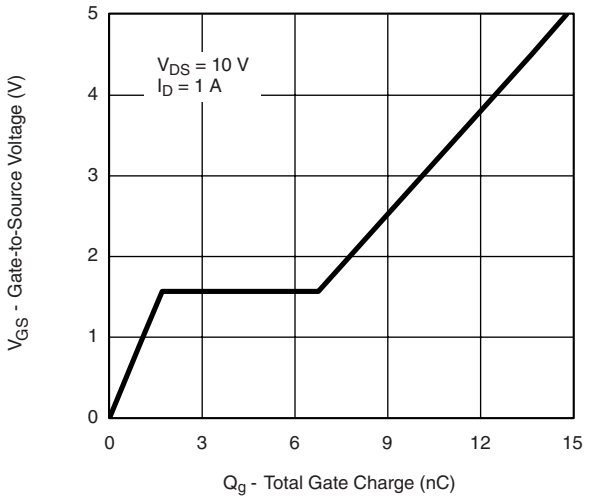
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



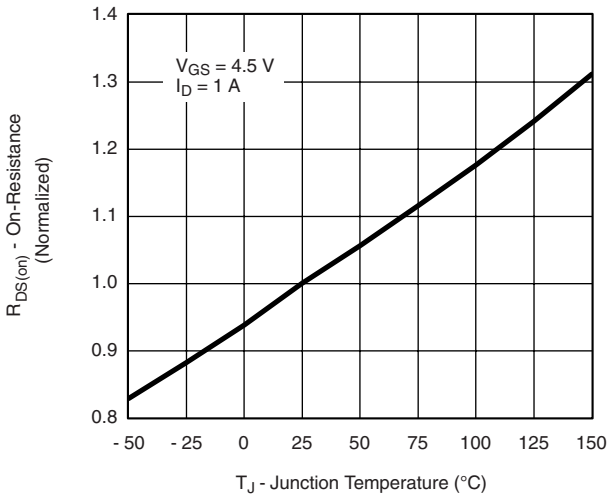
On-Resistance vs. Drain Current



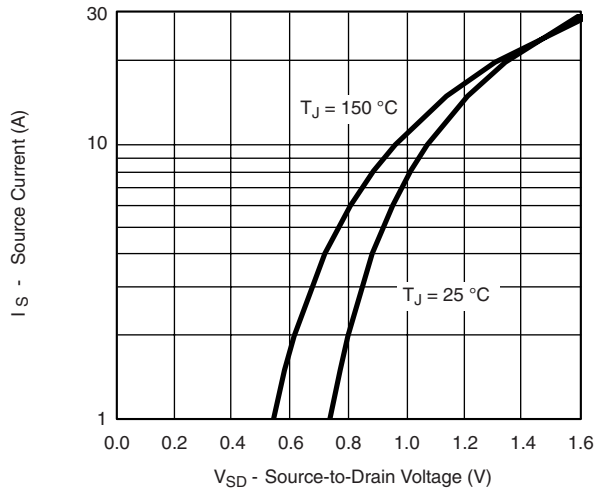
Capacitance



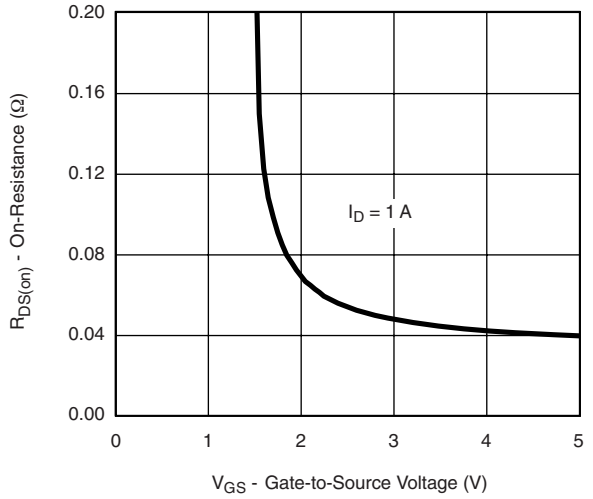
Gate Charge



On-Resistance vs. Junction Temperature

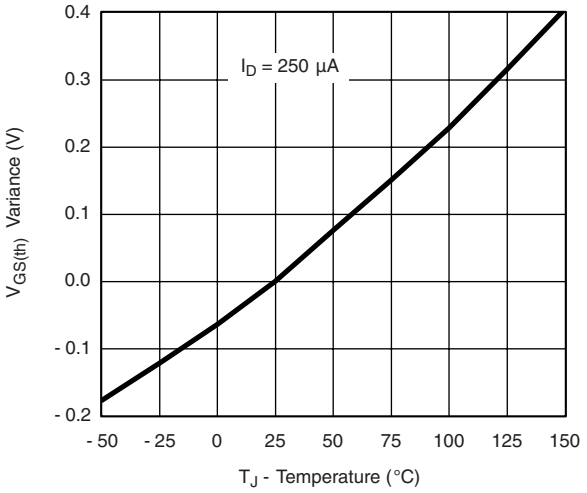


Source-Drain Diode Forward Voltage

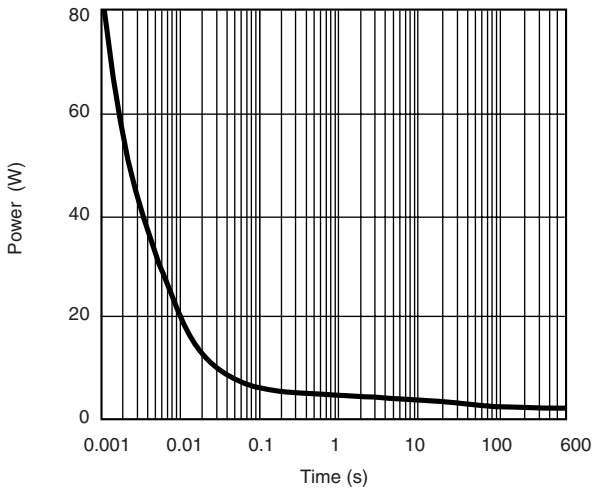


On-Resistance vs. Gate-to-Source Voltage

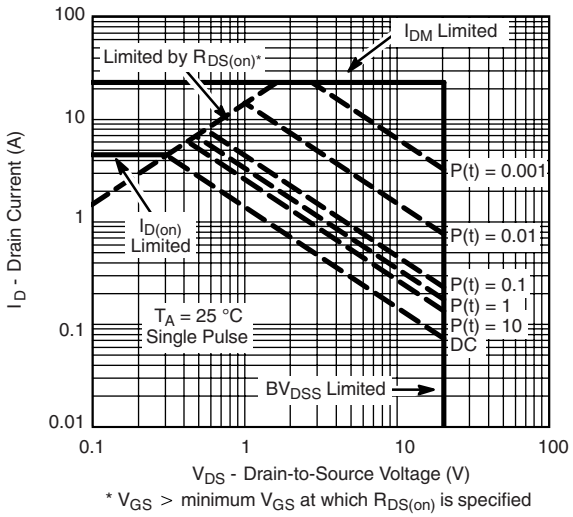
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



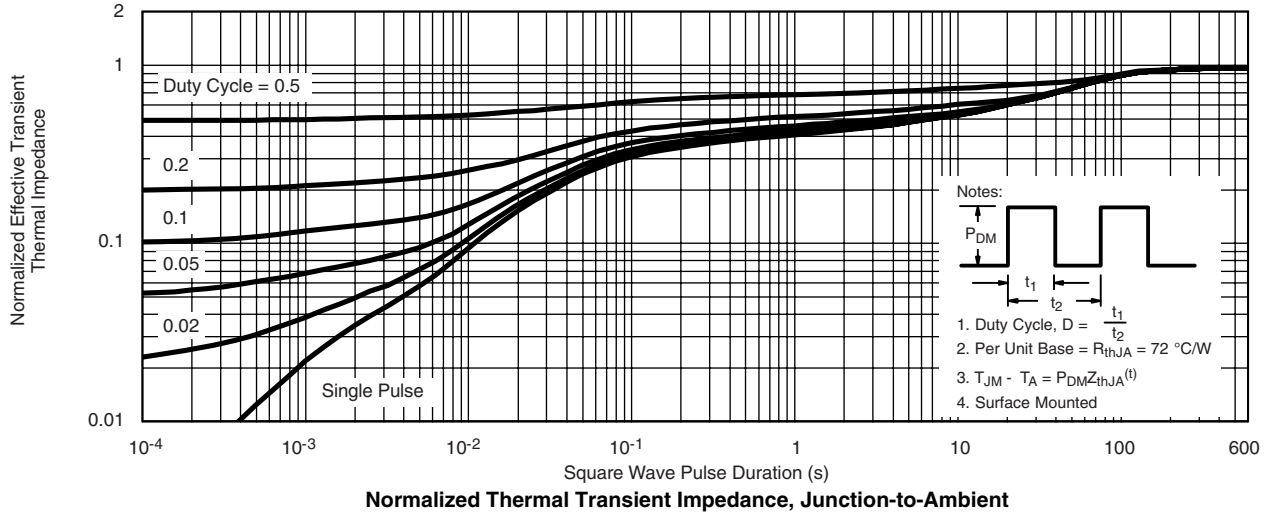
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

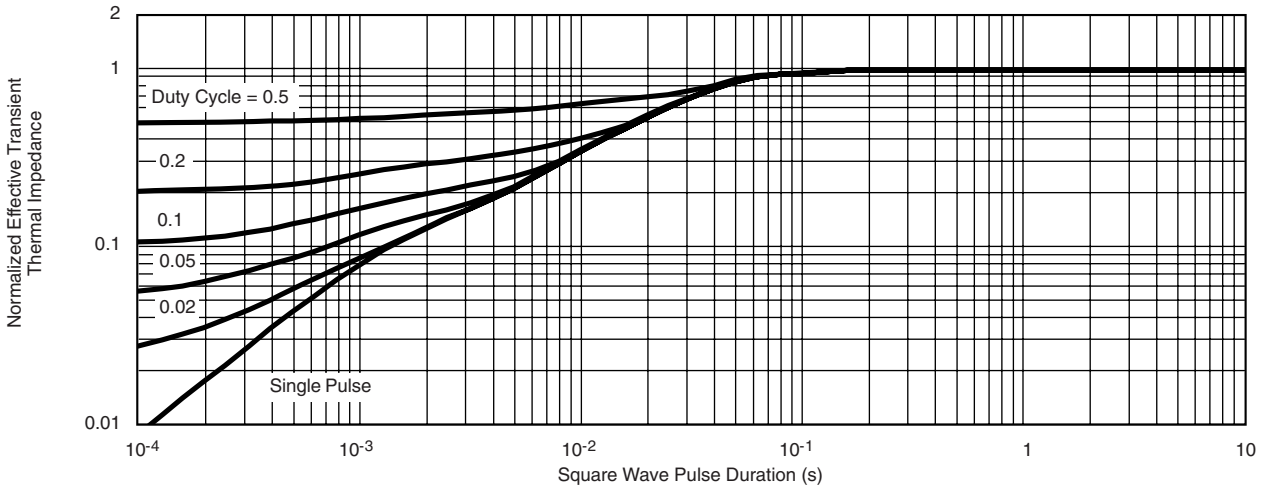


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

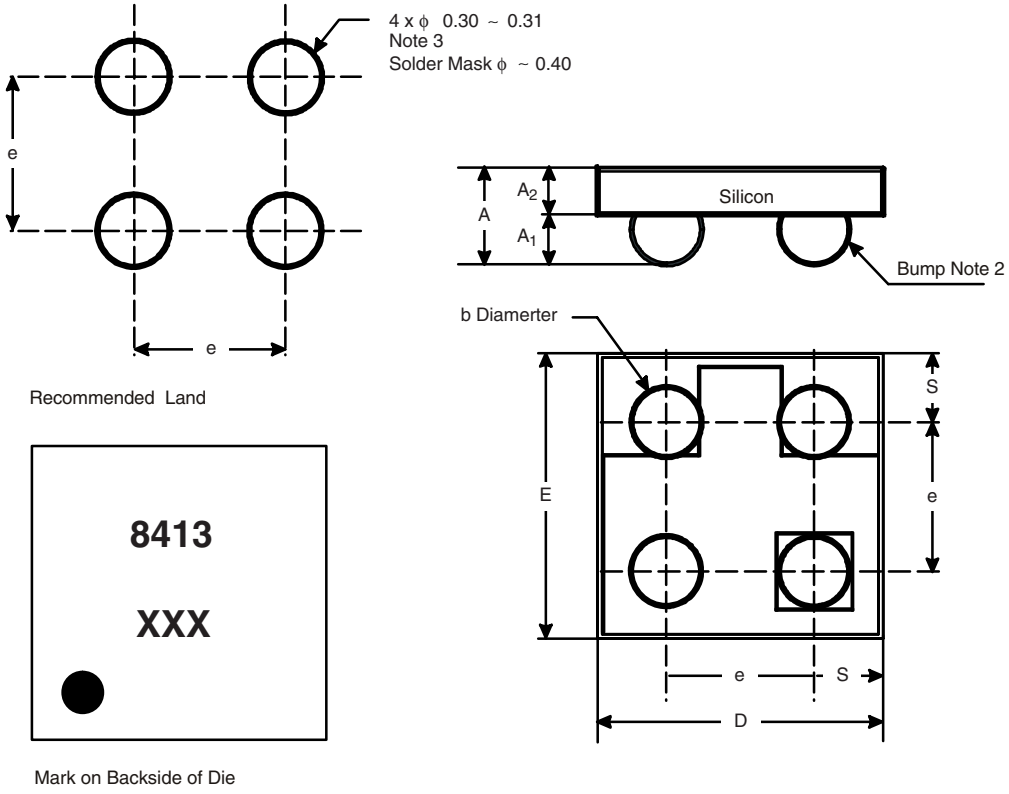
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (2 x 2, 0.8 mm PITCH)



Notes (Unless Otherwise Specified):
1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

DIMENSIONS	MILLIMETERS*		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.600	0.650	0.0236	0.0256
A_1	0.260	0.290	0.0102	0.0114
A_2	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.750	0.850	0.0295	0.0335
S	0.370	0.380	0.0146	0.0150

* Use millimeters as the primary measurement.

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