Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
−20	0.017 @ V_{GS} = −4.5 V	−12
	0.020 @ V_{GS} = −2.5 V	−11
	0.024 @ V_{GS} = −1.8 V	−10.1

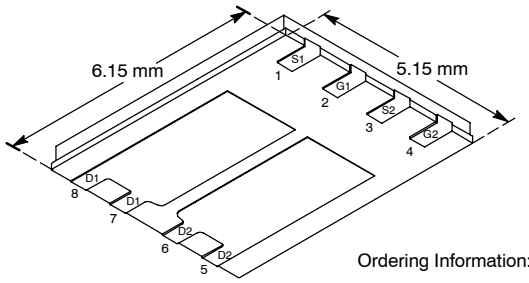
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

APPLICATIONS

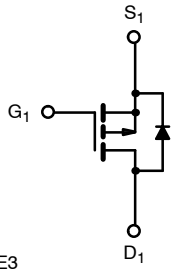
- Load Switch

PowerPAK SO-8

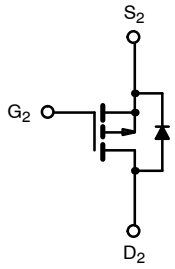


Bottom View

Ordering Information: Si7983DP-T1—E3



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	−20		V
Gate-Source Voltage		V_{GS}	±8		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	−12	−7.7	A
	T_A = 70°C		−9.6	−6.2	
Pulsed Drain Current		I_{DM}	−30		
continuous Source Current (Diode Conduction)[a]		I_S	−2.9	−1.2	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	3.5	1.4	W
	T_A = 70°C		2.2	0.9	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	26	35	°C/W
	Steady State		60	85	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.2	2.7	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

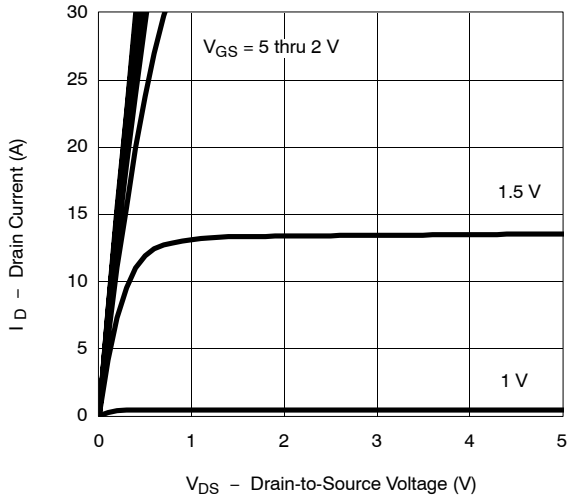
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −600 μA	−0.40		−1	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −20 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −20 V, V_{GS} = 0 V, T_J = 55°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −12 A		0.014	0.017	Ω
		V_{GS} = −2.5 V, I_D = −11 A		0.016	0.020	
		V_{GS} = −1.8 V, I_D = −4.1 A		0.020	0.024	
Forward Transconductance[a]	g_{fs}	V_{DS} = −15 V, I_D = −12 A		41		S
Diode Forward Voltage[a]	V_{SD}	I_S = −2.9 A, V_{GS} = 0 V		−0.8	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −4.5 V, I_D = −12 A		49	74	nC
Gate-Source Charge	Q_{gs}			7.2		
Gate-Drain Charge	Q_{gd}			12.1		
Gate Resistance	R_g	f = 1 MHz		8		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_g = 6 Ω		35	55	ns
Rise Time	t_r			60	90	
Turn-Off Delay Time	$t_{d(off)}$			390	585	
Fall Time	t_f			190	285	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −2.9 A, di/dt = 100 A/μs		106	160	

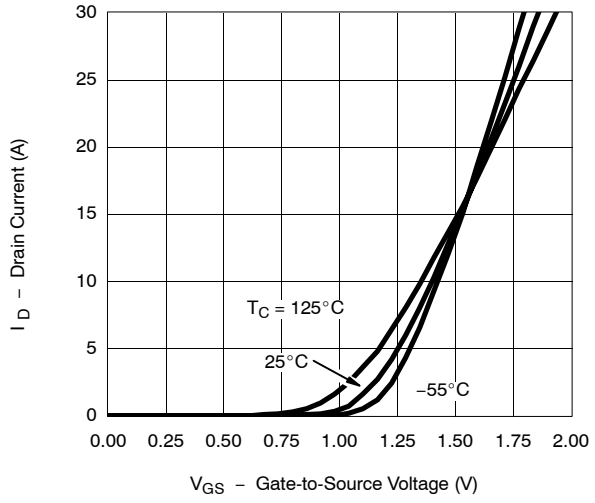
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

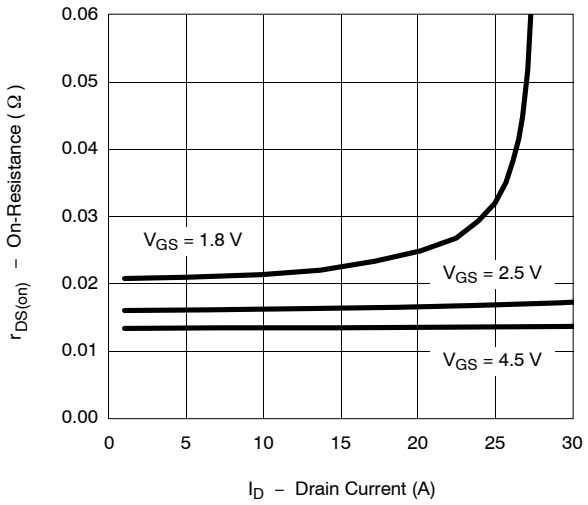


Transfer Characteristics

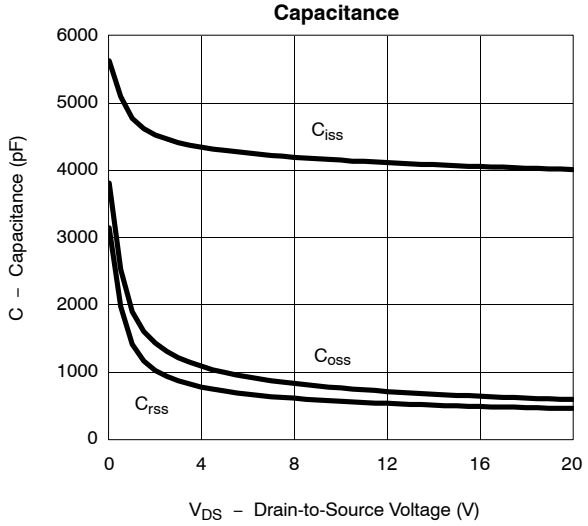


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

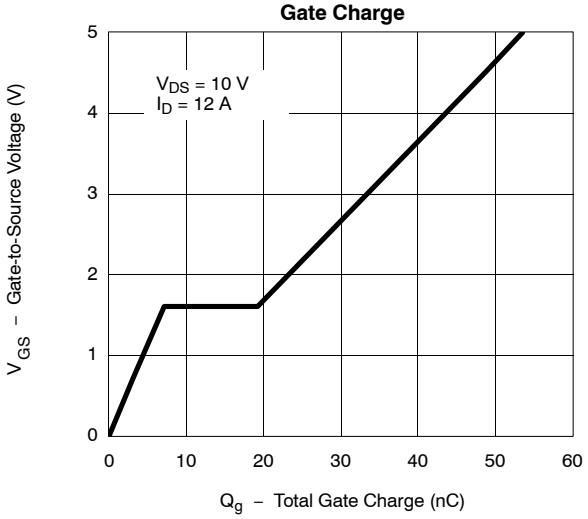
On-Resistance vs. Drain Current



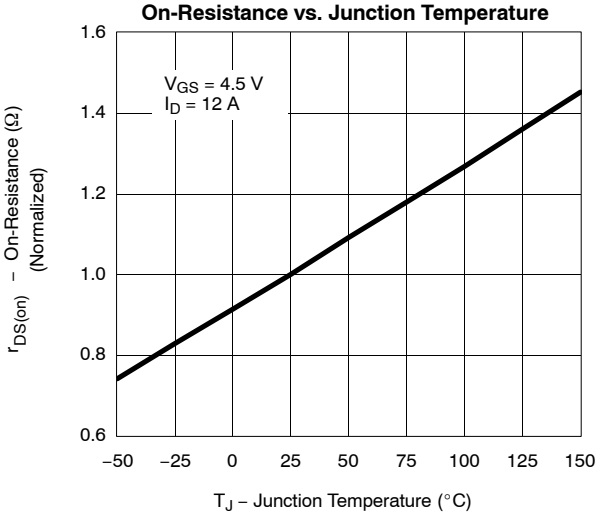
Capacitance



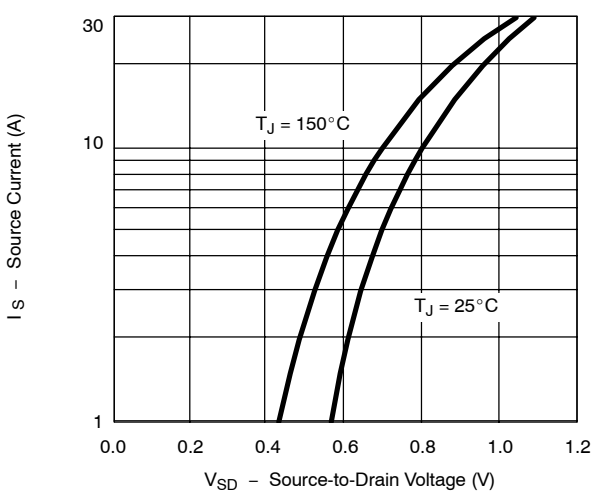
Gate Charge



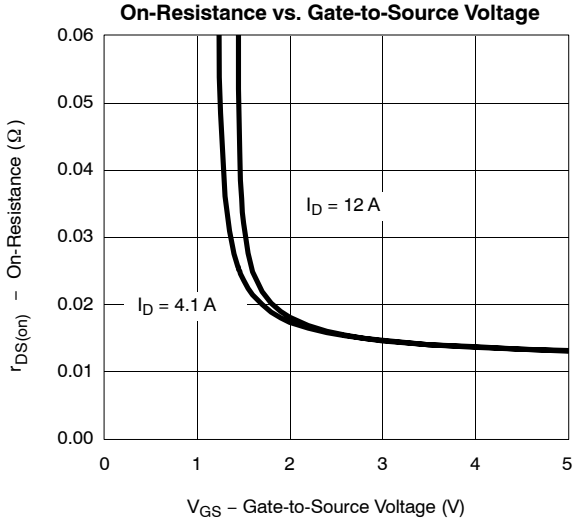
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

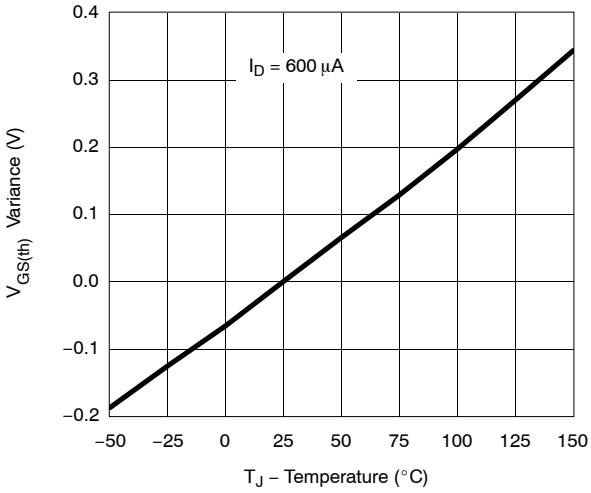


On-Resistance vs. Gate-to-Source Voltage

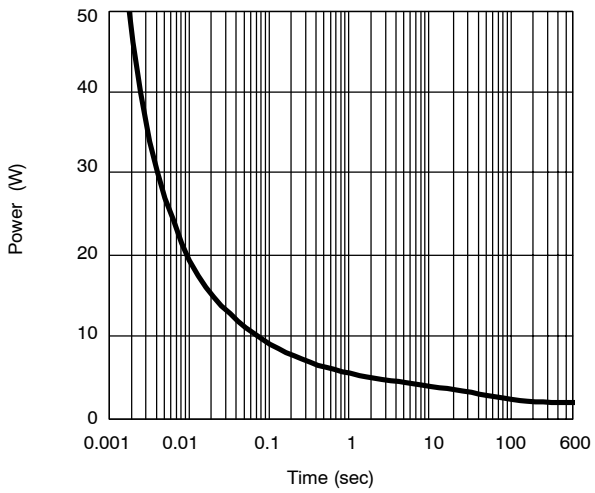


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

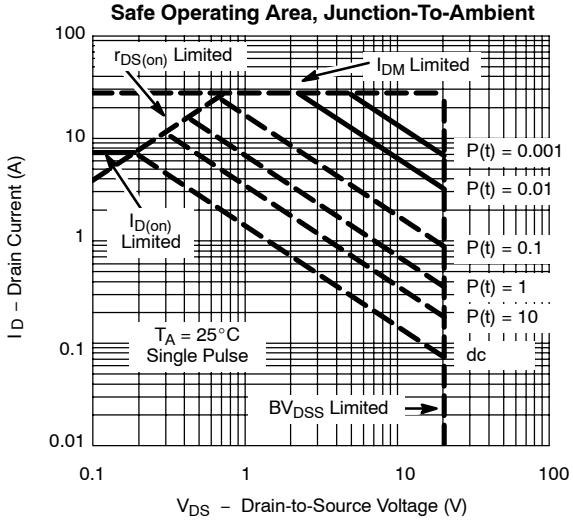
Threshold Voltage



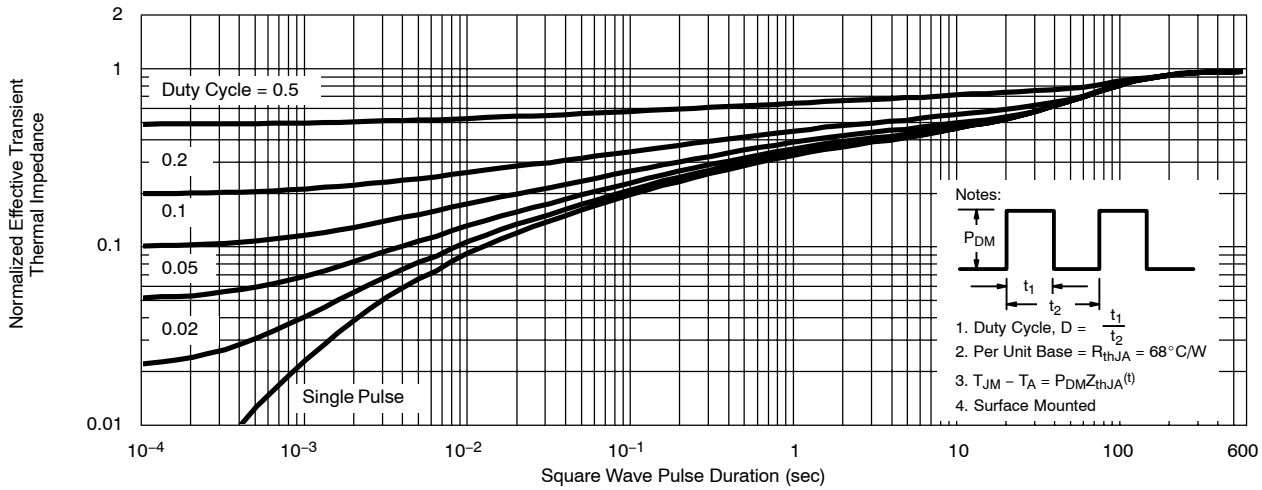
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-To-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



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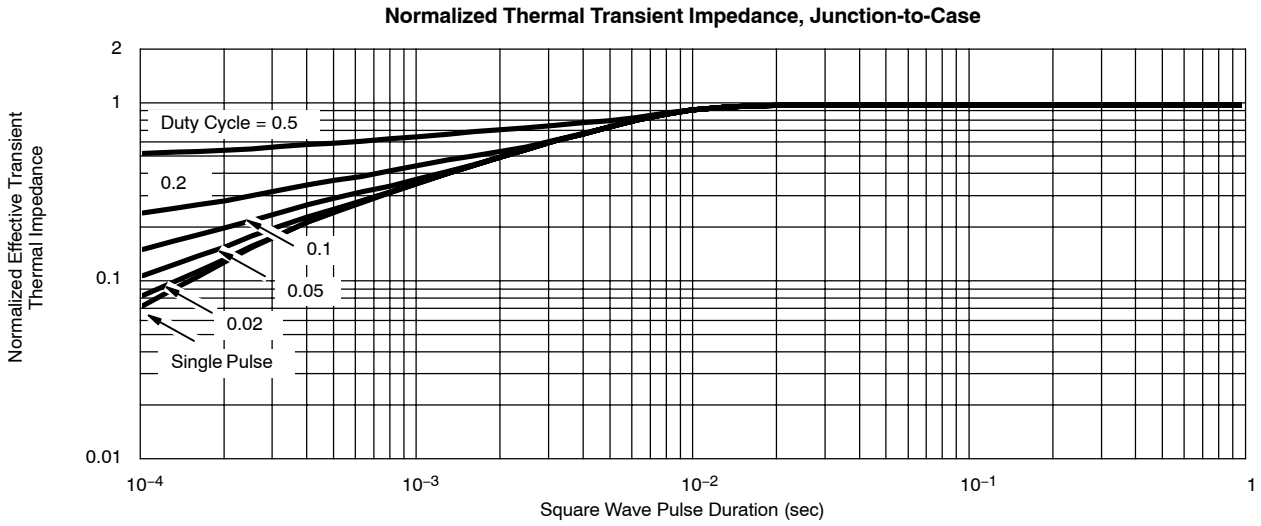

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