Dual P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 40	0.060 at V_{GS} = - 10 V	- 6[e]	11 nC
	0.089 at V_{GS} = - 4.5V	- 5[f]	

FEATURES

- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 1.07 mm Profile
- 100 % R_g and UIS Tested

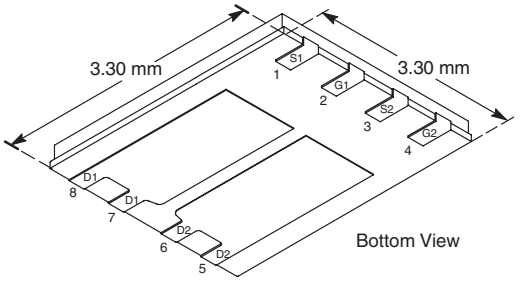
Pb-free

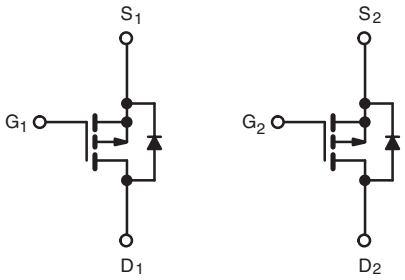
RoHS COMPLIANT

APPLICATIONS

- Load Switch

PowerPAK 1212-8





P-Channel MOSFET P-Channel MOSFET

Ordering Information: Si7905DN-T1-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 6[e]	A
	T_C = 70 °C		- 5	
	T_A = 25 °C		- 5[a, b]	
	T_A = 70 °C		- 4[a, b]	
Pulsed Drain Current		I_{DM}	- 20	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 6[e]	
	T_A = 25 °C		- 2[a, b]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 15	
Single-Pulse Avalanche Energy		E_{AS}	11.25	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	20.8	W
	T_C = 70 °C		13.3	
	T_A = 25 °C		2.5[a, b]	
	T_A = 70 °C		1.6[a, b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature)[c, d]			260	

Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. t = 10 s.
c. See Solder Profile (*http://www.vishay.com/ppg?73257*). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
e. Package limited.
f. T_C = 25 °C.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, b]	t ≤ 10 s	R_{thJA}	38	50	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4.5	6	

Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. Maximum under Steady State conditions is 94 °C/W.

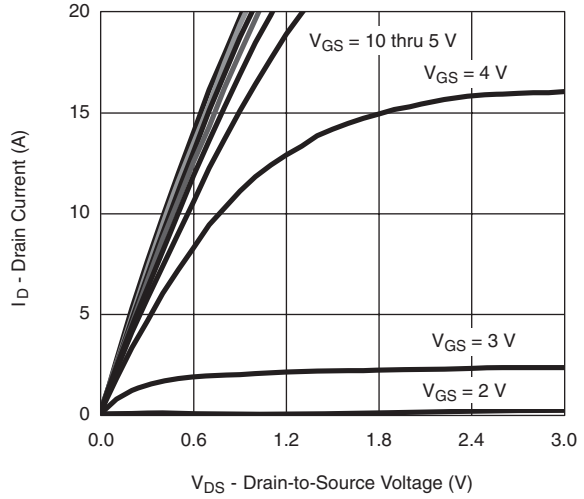
SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 44		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			4.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1		- 3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 40 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 40 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ - 5 V, V_{GS} = - 10 V	- 10			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = - 10 V, I_D = - 5 A		0.048	0.060	Ω
		V_{GS} = - 4.5 V, I_D = - 4 A		0.065	0.089	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 5 A		25		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 20 V, V_{GS} = 0 V, f = 1 MHz		880		pF
Output Capacitance	C_{oss}			100		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge	Q_g	V_{DS} = - 20 V, V_{GS} = - 10 V, I_D = - 5 A		20	30	nC
		V_{DS} = - 20 V, V_{GS} = - 4.5 V, I_D = - 5 A		11	16.5	
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			5		
Gate Resistance	R_g	f = 1 MHz		5.7	8.6	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 20 V, R_L = 5 Ω I_D ≅ - 4 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		42	65	ns
Rise Time	t_r			100	150	
Turn-Off DelayTime	$t_{d(off)}$			24	40	
Fall Time	t_f			11	17	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 20 V, R_L = 5 Ω I_D ≅ - 4 A, V_{GEN} = - 10 V, R_g = 1 Ω		6	10	
Rise Time	t_r			13	20	
Turn-Off DelayTime	$t_{d(off)}$			26	40	
Fall Time	t_f			10	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 6	A
Pulse Diode Forward Current[a]	I_{SM}				- 20	
Body Diode Voltage	V_{SD}	I_F = - 4 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 4 A, di/dt = 100 A/µs, T_J = 25 °C		20	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			15	23	nC
Reverse Recovery Fall Time	t_a			14		ns
Reverse Recovery Rise Time	t_b			16		

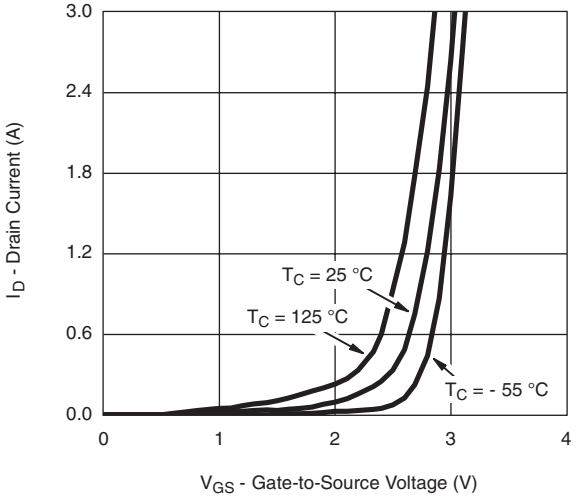
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

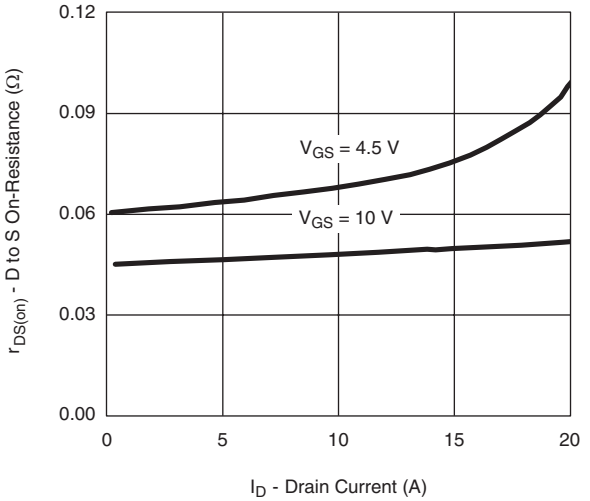
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



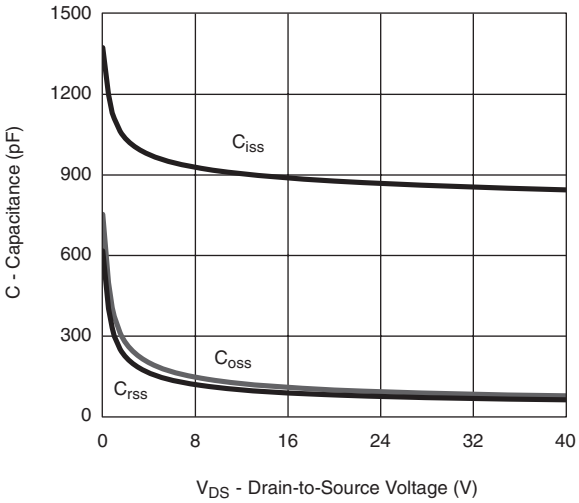
Output Characteristics



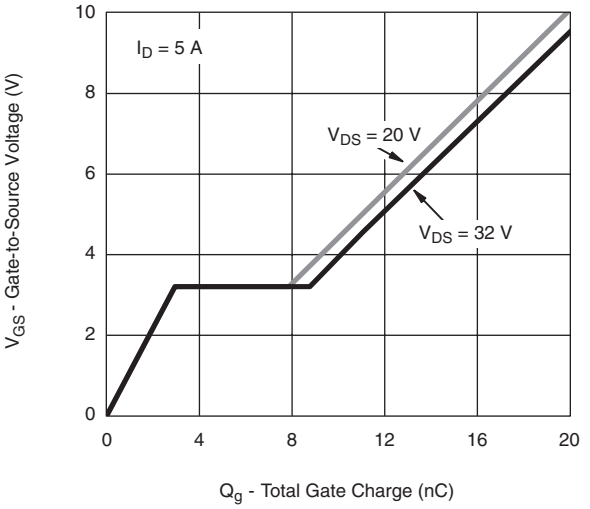
Transfer Characteristics



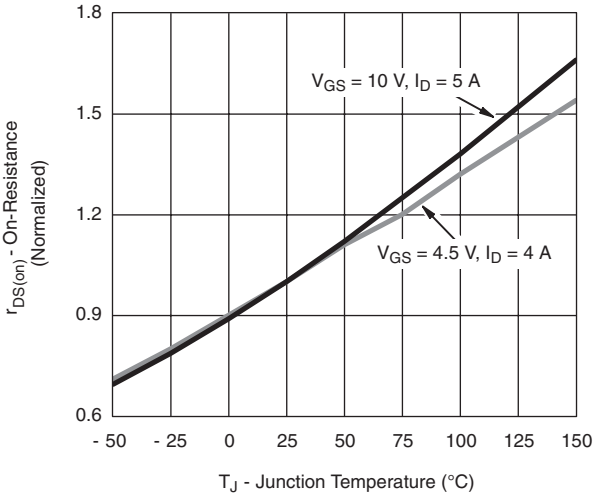
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

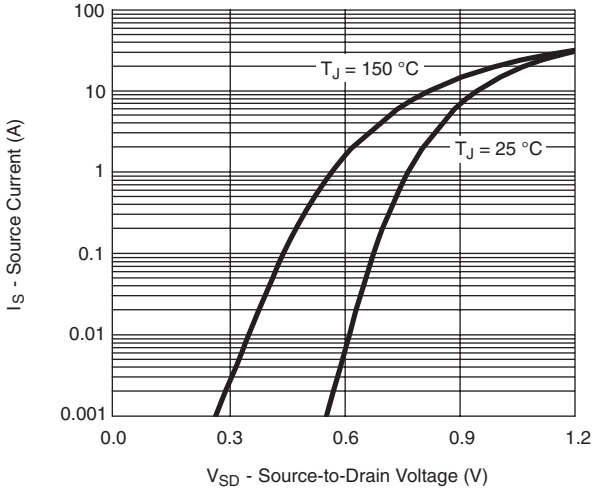


Gate Charge

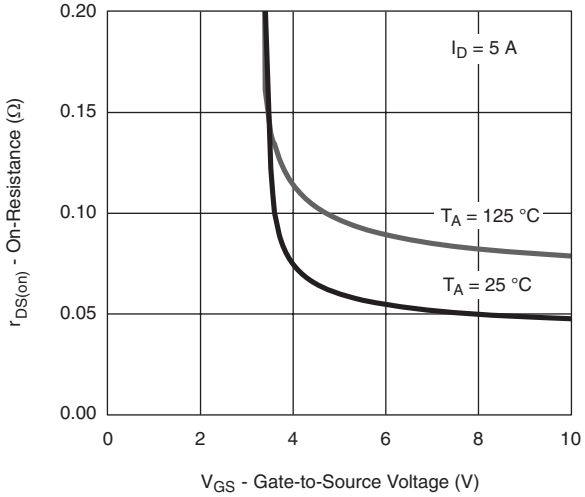


On-Resistance vs. Junction Temperature

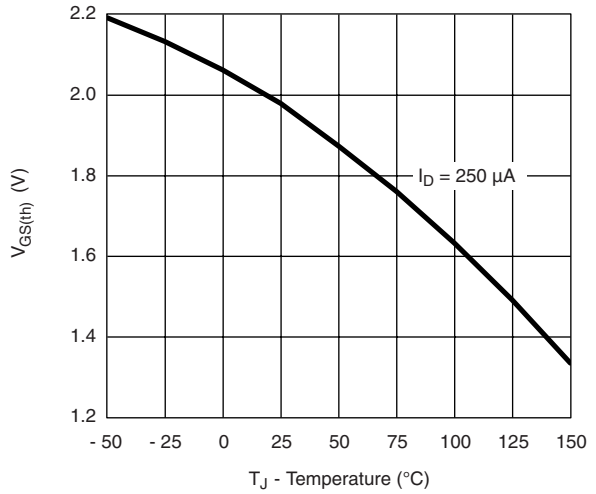
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



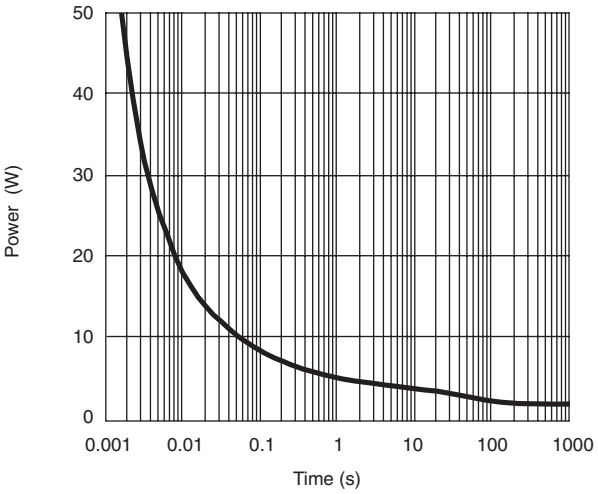
Source-Drain Diode Forward Voltage



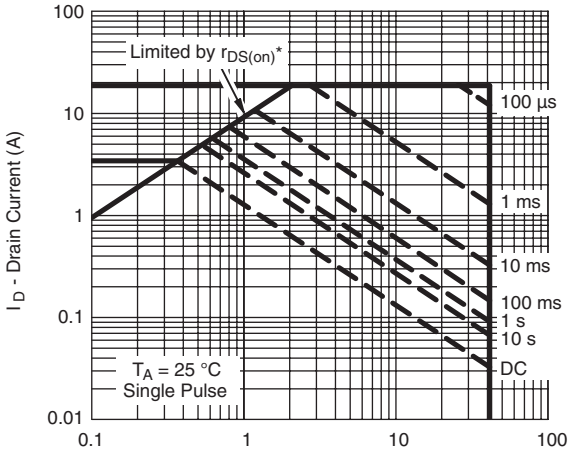
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



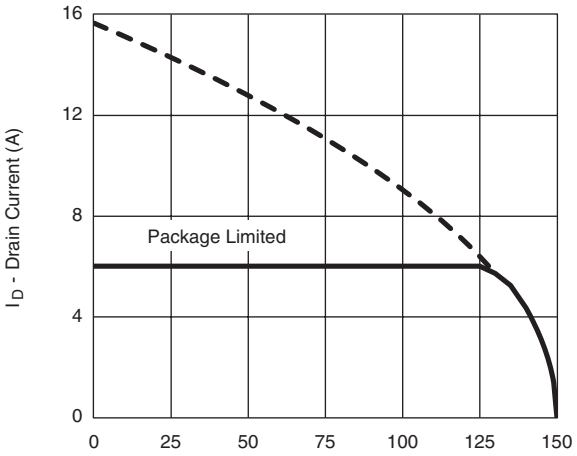
Single Pulse Power, Junction-to-Ambient



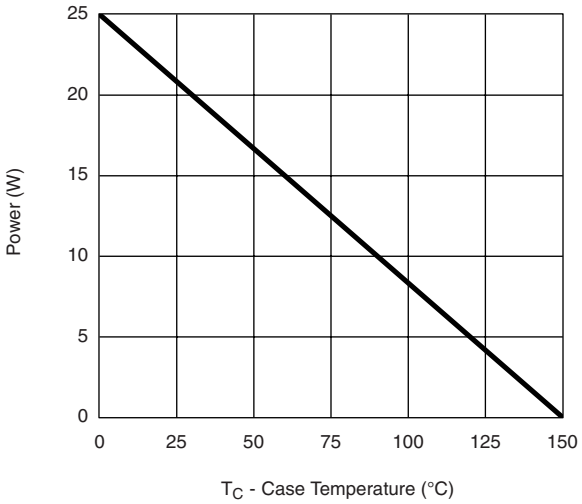
* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

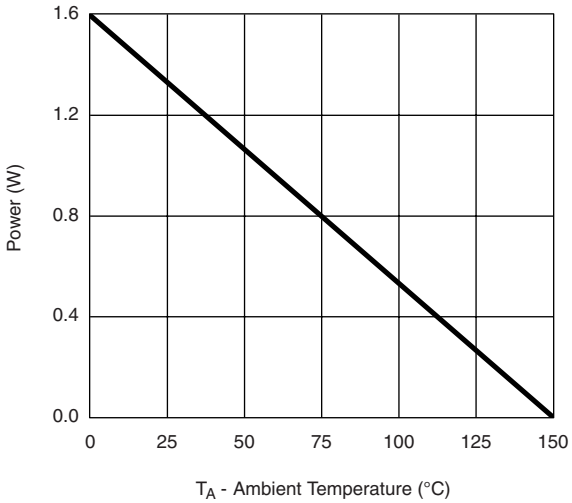
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



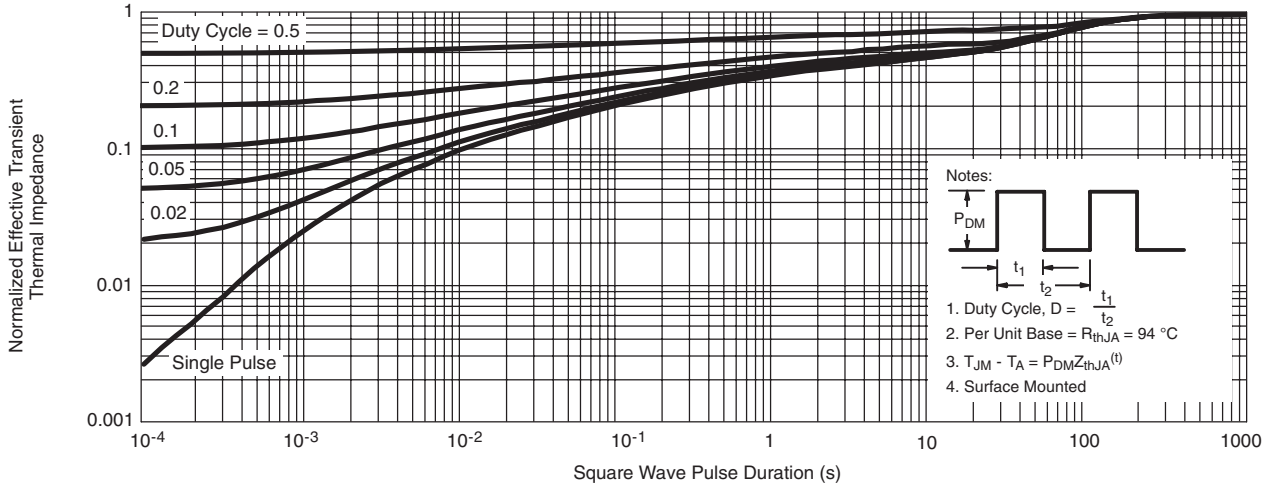
Power, Junction-to-Case



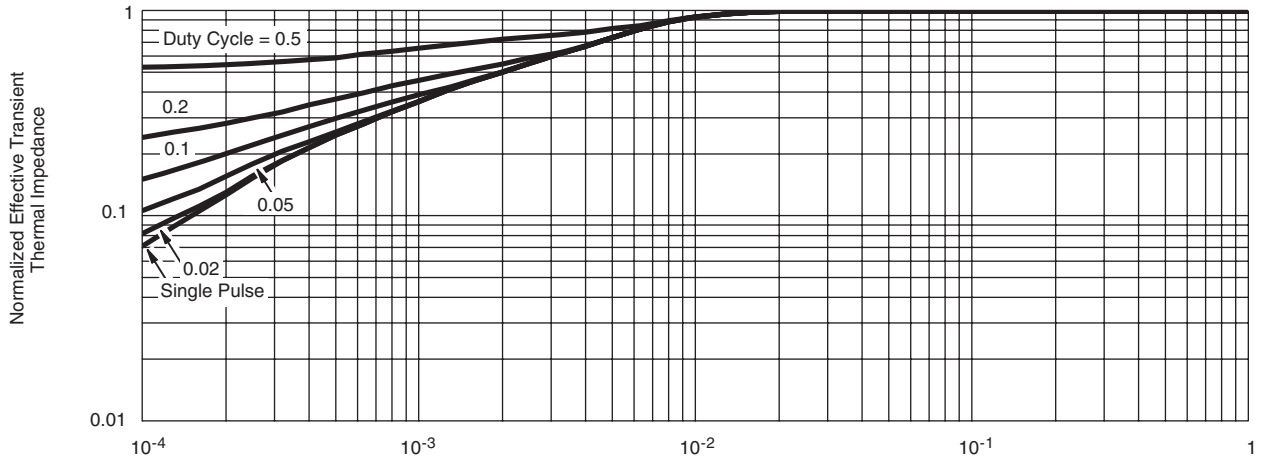
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?69920.

Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.