P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
– 30	0.0085 at V_{GS} = – 10 V	– 18
	0.013 at V_{GS} = – 4.5 V	– 14

FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

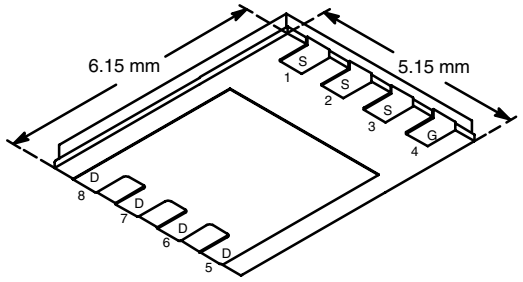
Pb-free Available

RoHS* COMPLIANT

APPLICATIONS

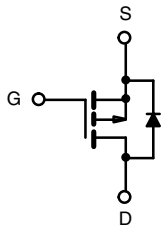
- Battery and Load Switching
  - Notebook and Tablet Computers
  - Notebook and Tablet Battery Packs

PowerPAK SO-8



Bottom View

Ordering Information: Si7491DP-T1
Si7491DP-T1—E3 (Lead (Pb)-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	– 30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	– 18	– 11	A
	T_A = 70 °C		– 14	– 8	
Pulsed Drain Current		I_{DM}	– 50		
Continuous Source Current (Diode Conduction)[a]		I_S	– 4.5	– 1.6	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	5	1.8	W
	T_A = 70 °C		3.2	1.1	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	– 55 to 150		°C
Soldering Recommendations (Peak Temperature)[b,c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	20	25	°C/W
	Steady State		54	68	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.7	2.2	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (*http://www.vishay.com/ppg?73257*). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

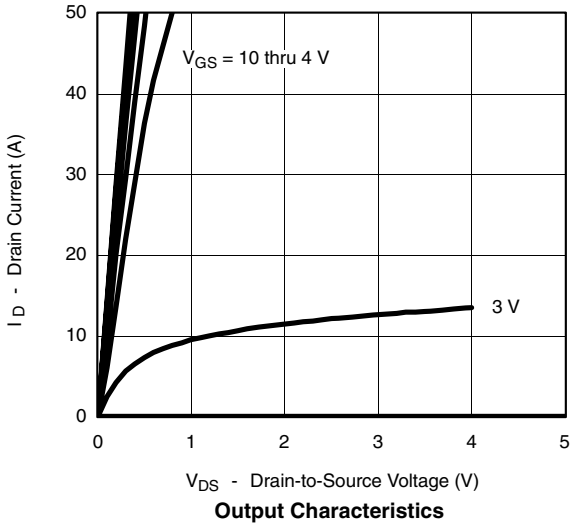
* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = – 250 µA	– 1.0		– 3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = – 30 V, V_{GS} = 0 V			– 1	µA
		V_{DS} = – 30 V, V_{GS} = 0 V, T_J = 70 °C			– 10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = – 5 V, V_{GS} = – 10 V	– 30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = – 10 V, I_D = – 18 A		0.007	0.0085	Ω
		V_{GS} = – 4.5 V, I_D = – 14 A		0.0105	0.013	
Forward Transconductance[a]	g_{fs}	V_{DS} = – 15 V, I_D = – 18 A		46		S
Diode Forward Voltage[a]	V_{SD}	I_S = – 4.5 A, V_{GS} = 0 V		– 0.74	– 1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = – 15 V, V_{GS} = – 5 V, I_D = – 18 A		56	85	nC
Gate-Source Charge	Q_{gs}			12		
Gate-Drain Charge	Q_{gd}			25		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = – 15 V, R_L = 15 Ω $I_D \cong$ – 1 A, V_{GEN} = – 4.5 V, R_G = 6 Ω		150	225	ns
Rise Time	t_r			190	290	
Turn-Off Delay Time	$t_{d(off)}$			120	180	
Fall Time	t_f			90	140	
Gate Resistance	R_g			2.5		
Source-Drain Reverse Recovery Time	t_{rr}	I_F = – 2.9 A, di/dt = 100 A/µs		50	80	

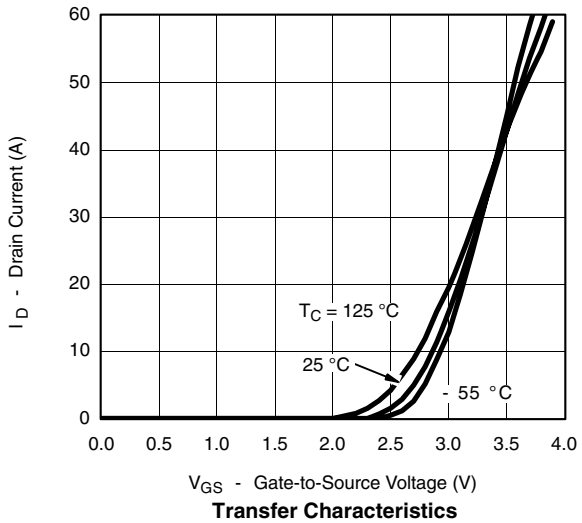
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless noted

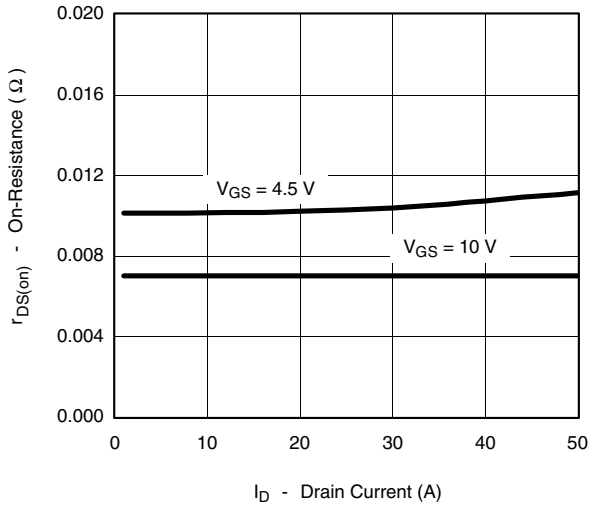


Output Characteristics

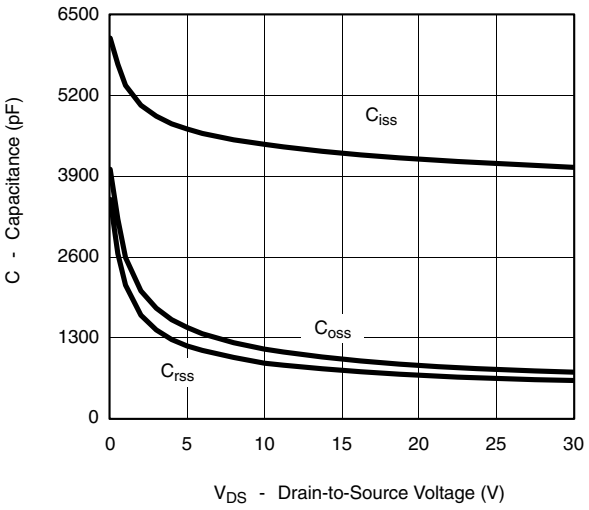


Transfer Characteristics

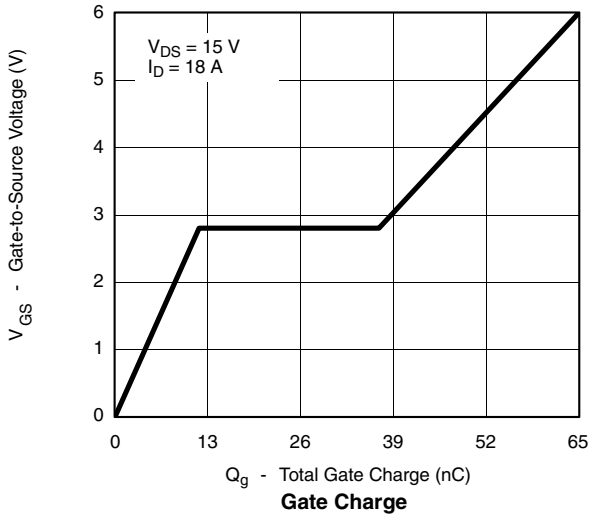
TYPICAL CHARACTERISTICS 25 °C, unless noted



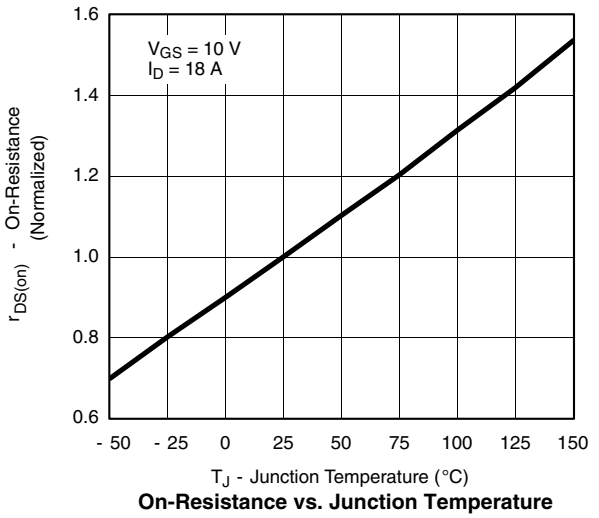
On-Resistance vs. Drain Current



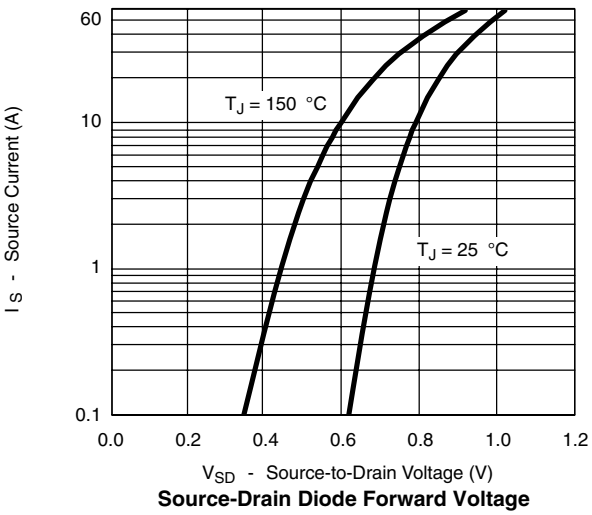
Capacitance



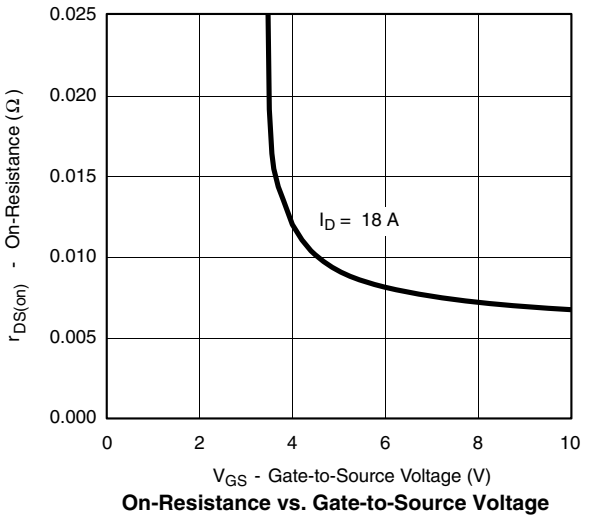
Gate Charge



On-Resistance vs. Junction Temperature

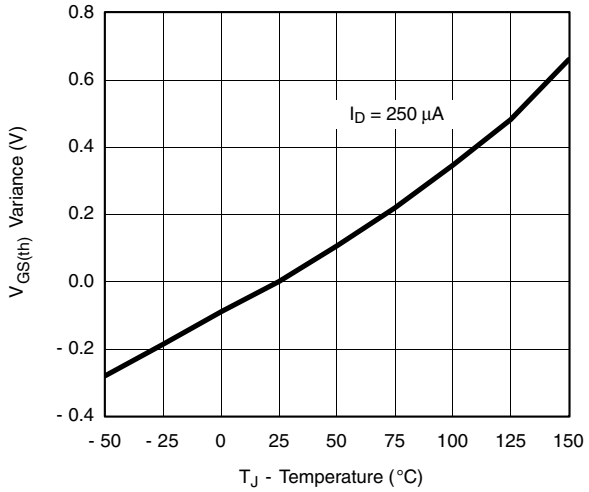


Source-Drain Diode Forward Voltage

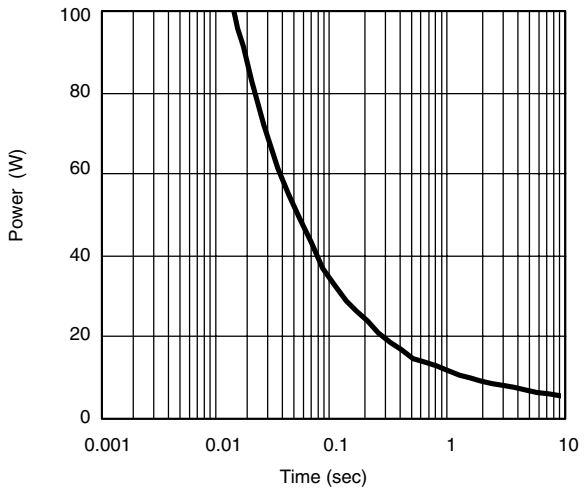


On-Resistance vs. Gate-to-Source Voltage

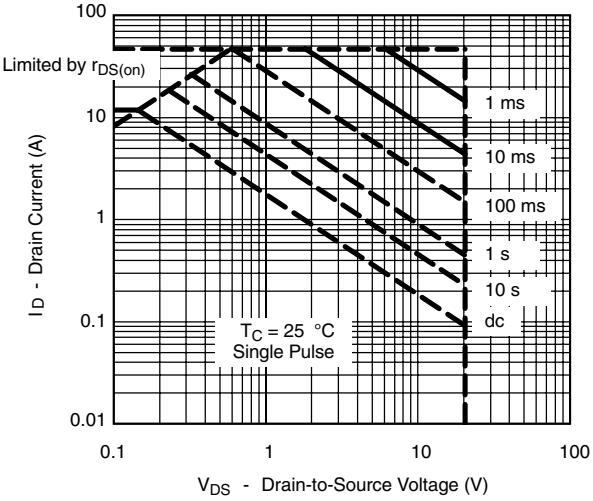
TYPICAL CHARACTERISTICS 25 °C, unless noted



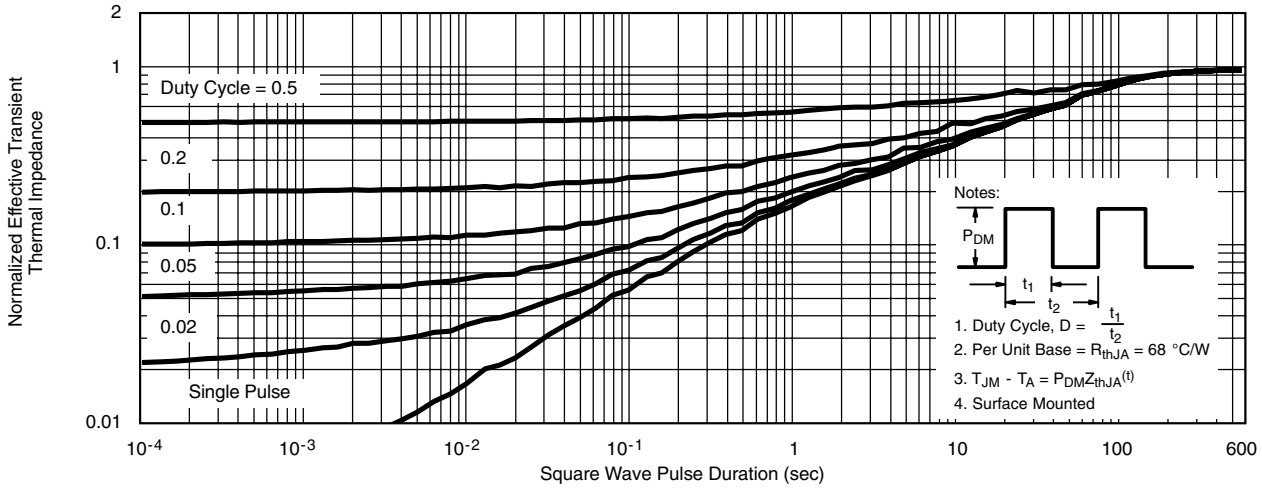
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

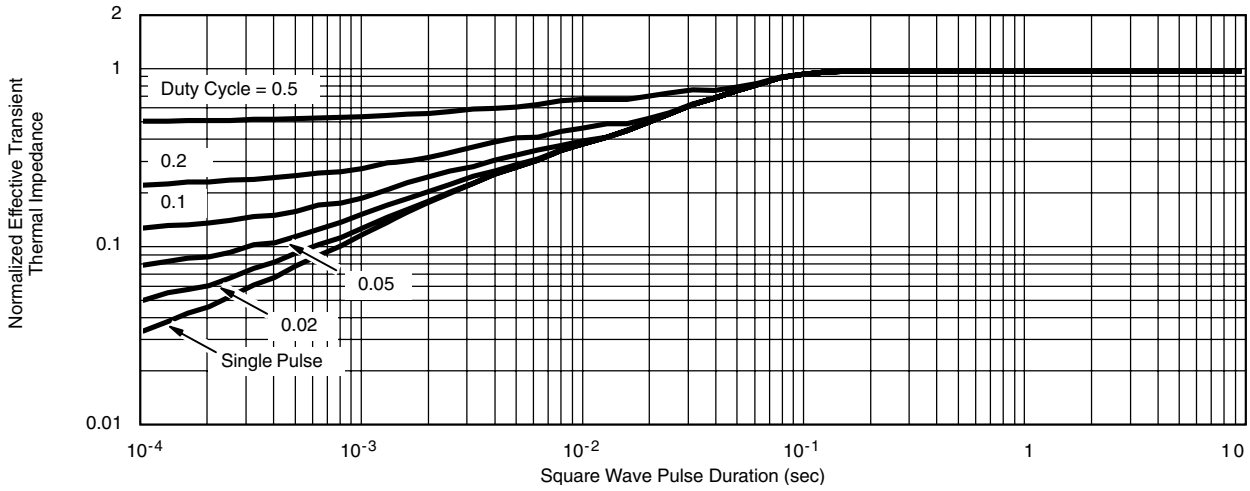


Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72276.

Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.