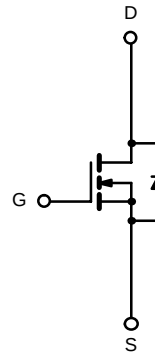
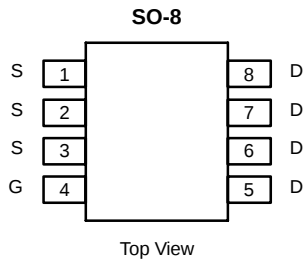




N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.034 @ $V_{GS} = 10$ V	6.9
	0.040 @ $V_{GS} = 6.0$ V	6.4

175°C Rated
Maximum Junction Temperature
High-Efficiency
PWM Optimized



Ordering Information: Si4484EY
Si4484EY-T1 (with Tape and Reel)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	10 secs	Steady State
Drain-Source Voltage		V_{DS}	100	
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	6.9	4.8
	$T_A = 85^\circ\text{C}$		5.4	3.7
Pulsed Drain Current		I_{DM}	30	
Avalanche Current		I_{AR}	25	
Repetitive Avalanche Energy (Duty Cycle $\leq 1\%$)		E_{AR}	31	
Continuous Source Current (Diode Conduction) ^a		I_S	3.1	1.5
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	3.8	1.8
	$T_A = 85^\circ\text{C}$		2.3	1.1
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	33	40	$^\circ\text{C/W}$
	Steady State		70	85	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	17	21	

Notes

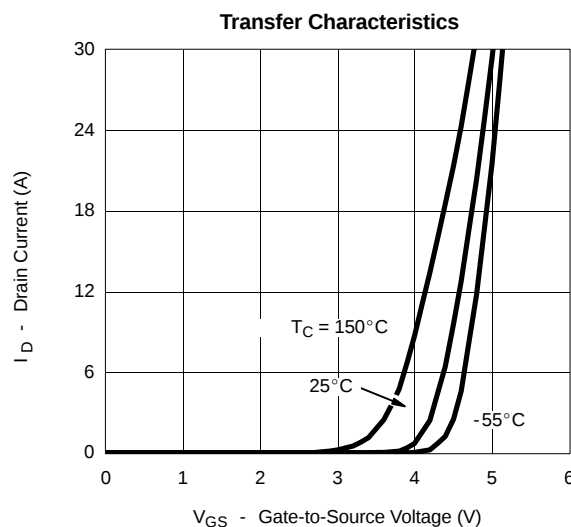
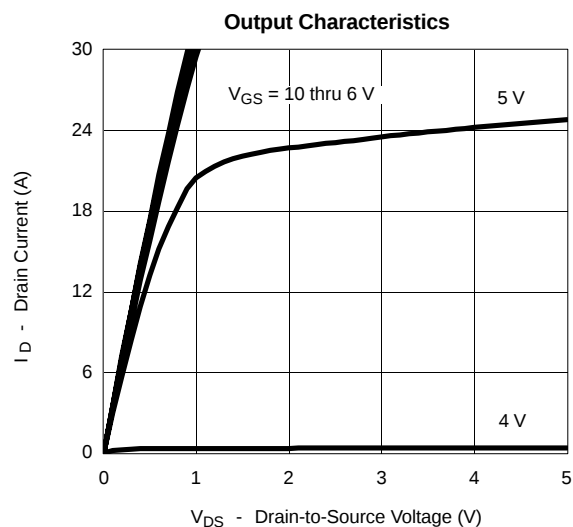
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 85^\circ\text{C}$			20	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 6.9\ \text{A}$		0.028	0.034	Ω
		$V_{GS} = 6.0\ \text{V}$, $I_D = 6.4\ \text{A}$		0.032	0.040	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 6.9\ \text{A}$		25		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.1\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 50\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 6.9\ \text{A}$		24	30	nC
Gate-Source Charge	Q_{gs}			7.6		
Gate-Drain Charge	Q_{gd}			5.4		
Gate Resistance	R_g		0.5	1.25	2.2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\ \text{V}$, $R_L = 50\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		16	30	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			35	70	
Fall Time	t_f			20	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.1\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		50	80	

Notes

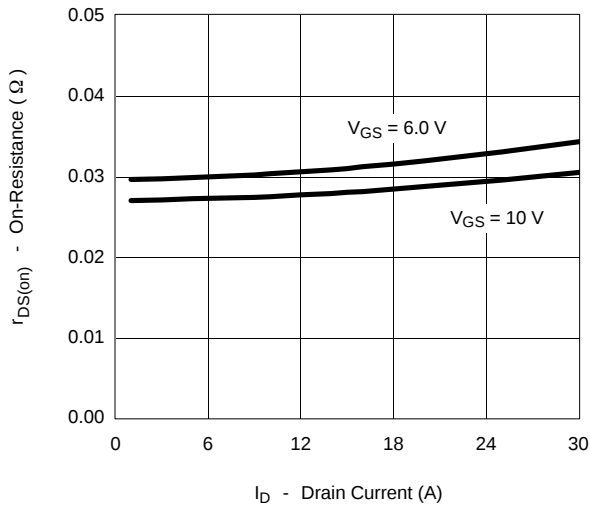
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

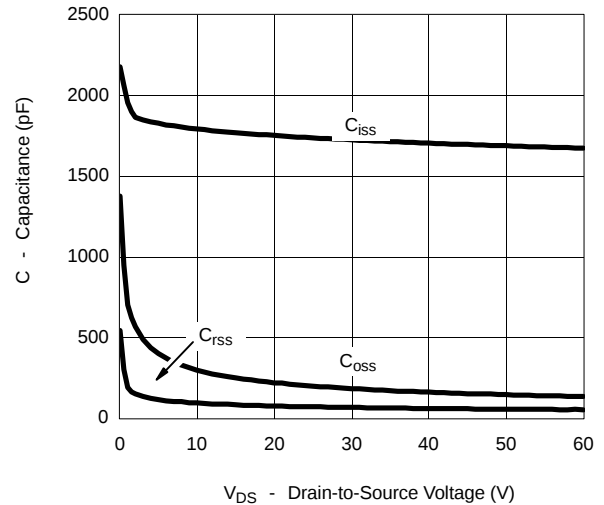


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

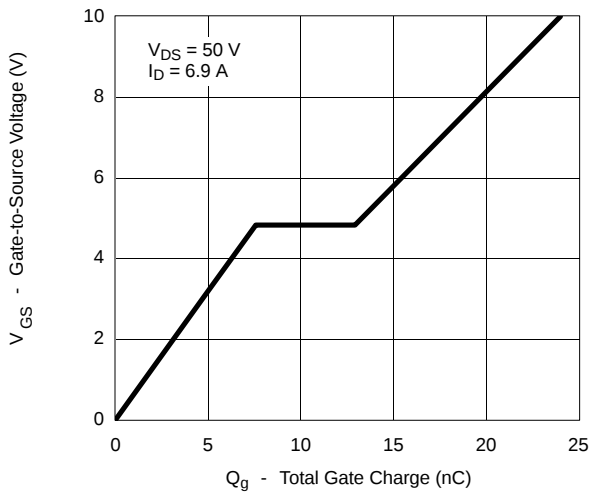
On-Resistance vs. Drain Current



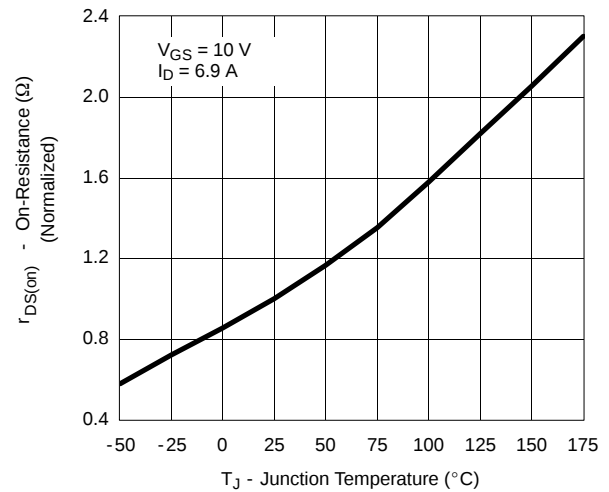
Capacitance



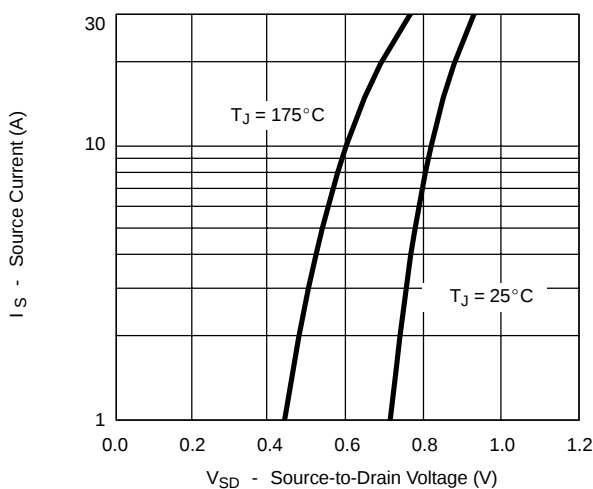
Gate Charge



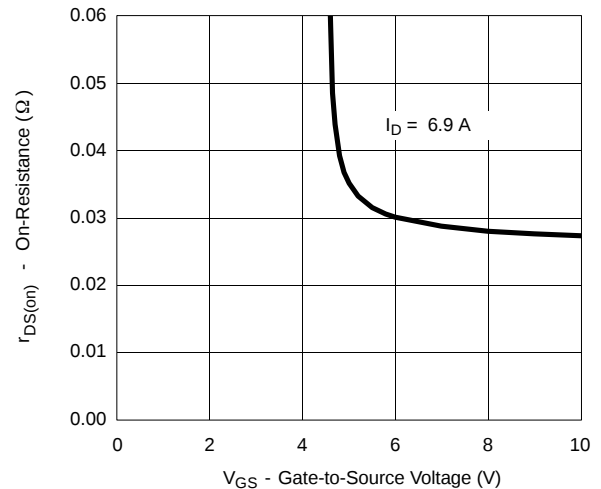
On-Resistance vs. Junction Temperature

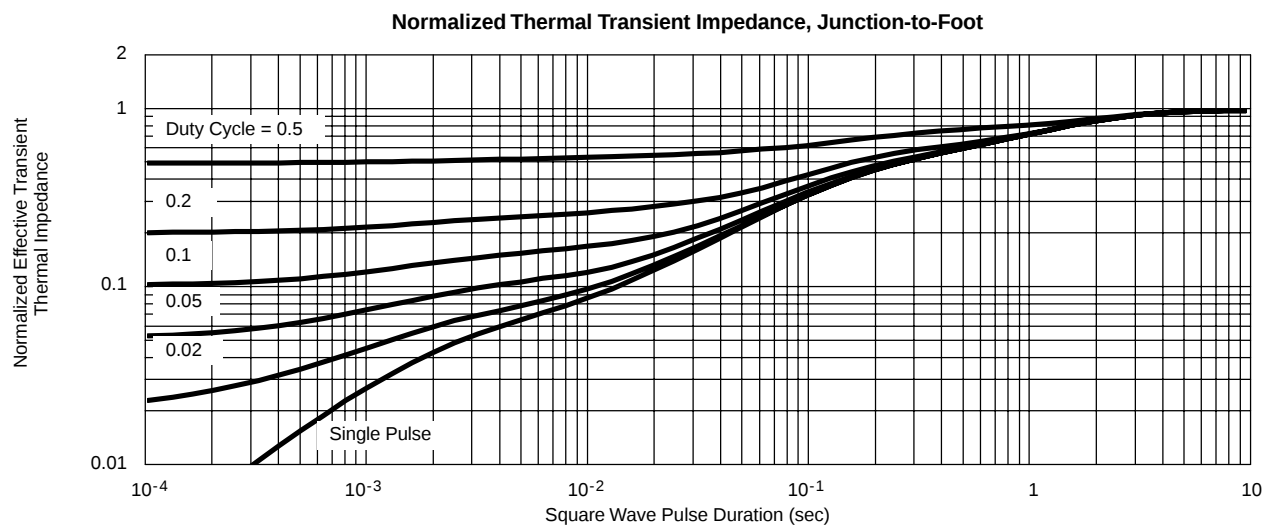
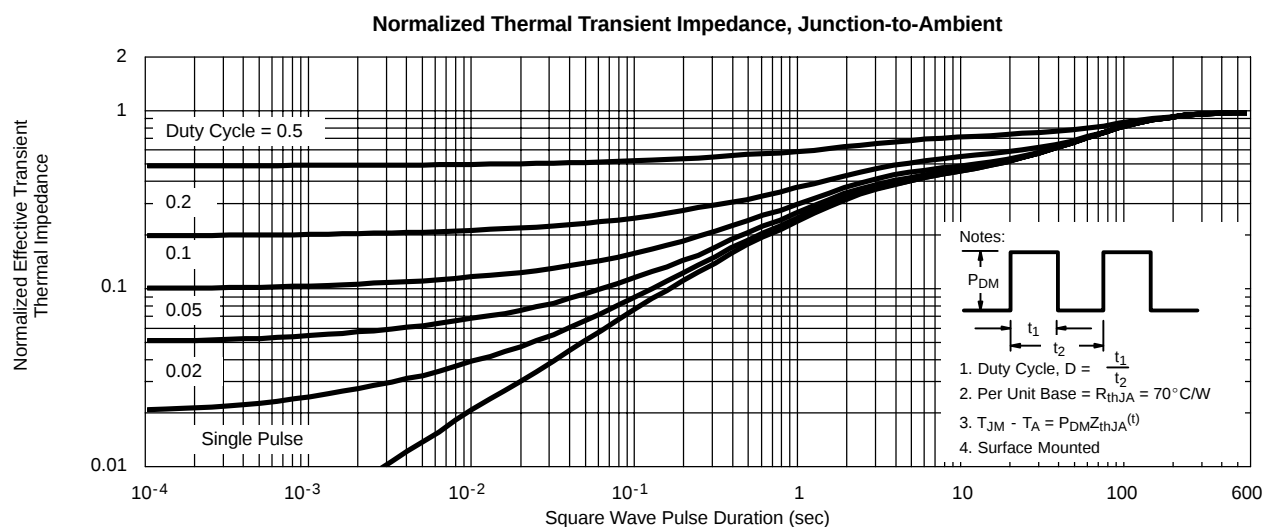
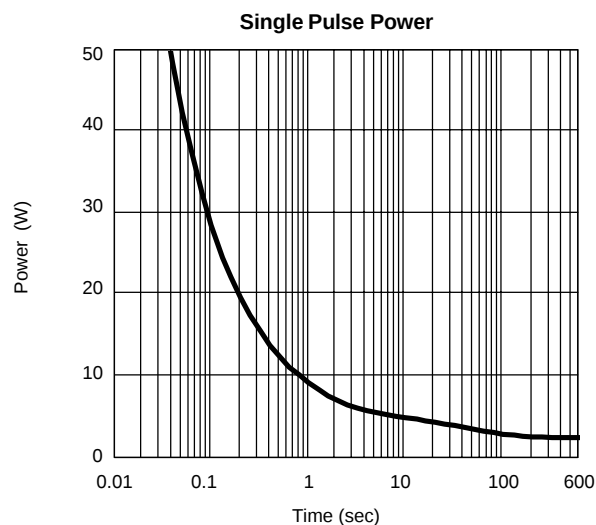
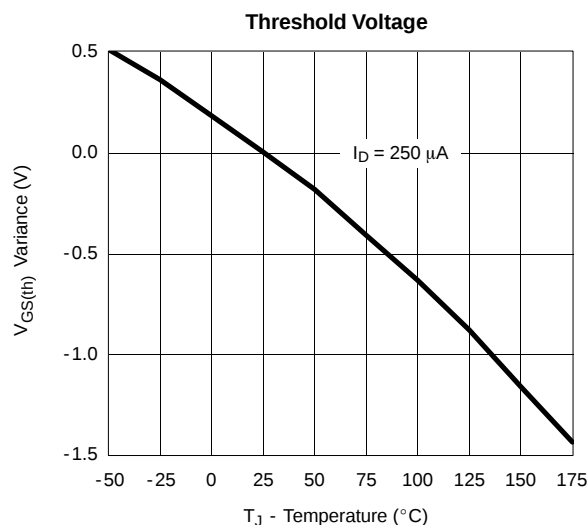


Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)




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