



New Product

Si4436DY
Vishay Siliconix

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ)
60	0.036 at $V_{GS} = 10$ V	8	10.5 nC
	0.043 at $V_{GS} = 4.5$ V	8	

FEATURES

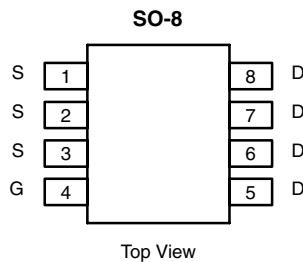
- TrenchFET® Power MOSFET
- Optimized for “Low Side” Synchronous Rectifier Operation
- 100 % R_g and UIS Tested

APPLICATIONS

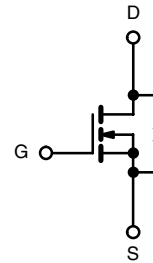
- CCFL Inverter



RoHS
COMPLIANT



Ordering Information: Si4436DY-T1-E3 (Lead-(Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	8 ^a	A
	$T_C = 70^\circ\text{C}$		6.8	
	$T_A = 25^\circ\text{C}$		6.1 ^{b, c}	
	$T_A = 70^\circ\text{C}$		4.8 ^{b, c}	
Pulsed Drain Current		I_{DM}	25	
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	I_S	4.2	
	$T_A = 25^\circ\text{C}$		2.1 ^{b, c}	
Avalanche Current		I_{AS}	15	mJ
Single Pulse Avalanche Energy		E_{AS}	11.2	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	5	W
	$T_C = 70^\circ\text{C}$		3.2	
	$T_A = 25^\circ\text{C}$		2.5 ^{b, c}	
	$T_A = 70^\circ\text{C}$		1.6 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	$t \leq 10$ sec	R_{thJA}	38	50	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	20	25	

Notes:

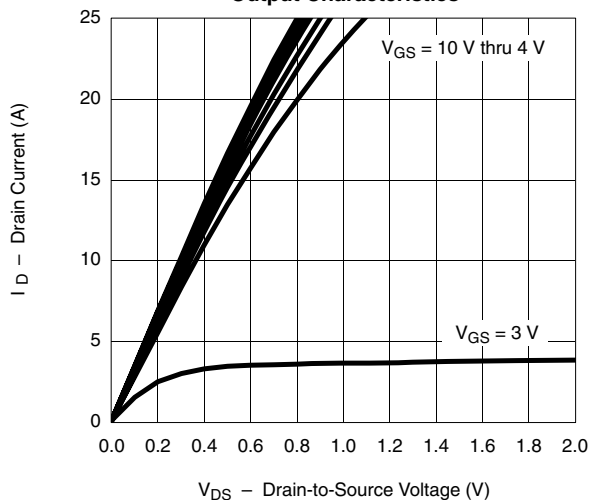
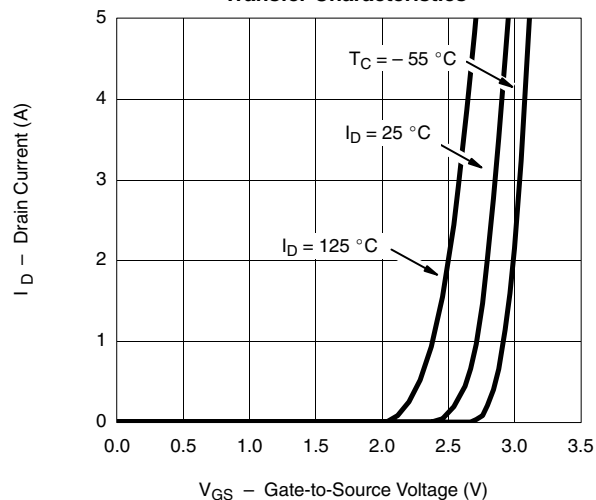
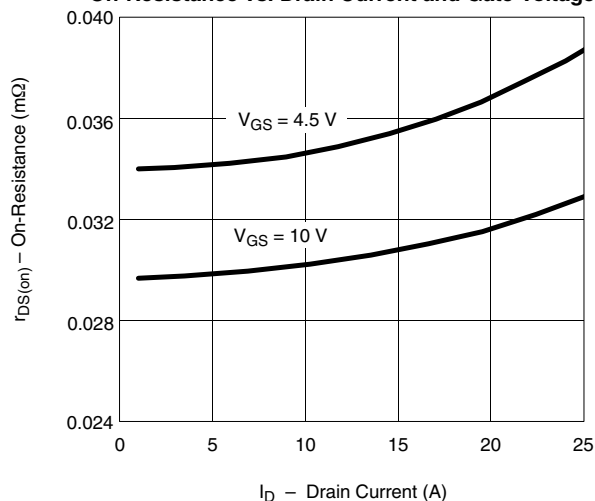
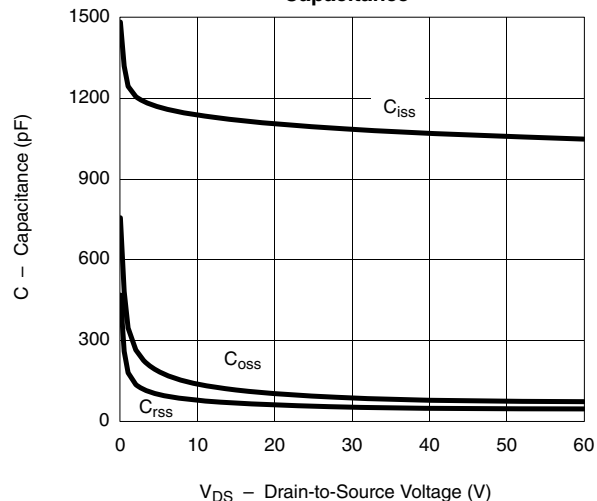
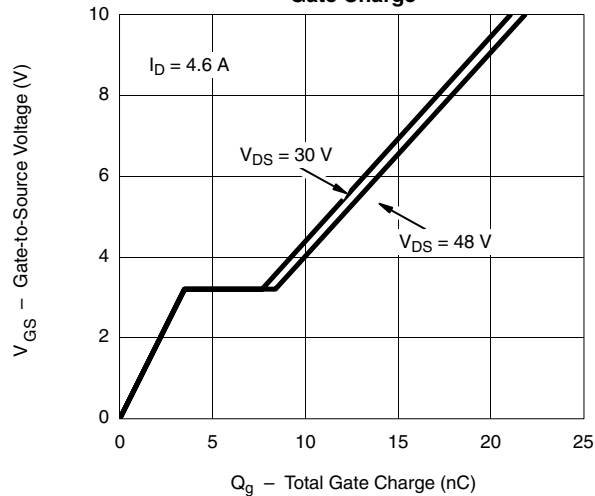
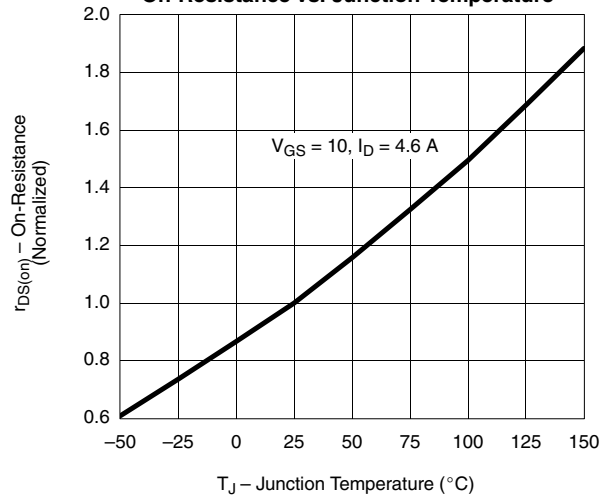
- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ sec.
- Maximum under steady state conditions is 85°C/W .

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	60			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		55		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			– 6.3		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5		2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	25			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.6 A		0.030	0.036	Ω
		V _{GS} = 4.5 V, I _D = 4.2 A		0.035	0.043	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 4.6 A		20		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		1100		pF
Output Capacitance	C _{oss}			90		
Reverse Transfer Capacitance	C _{rss}			55		
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4.6 A		21	32	nC
		V _{DS} = 30 V, V _{GS} = 4.5 V, I _D = 4.6 A		10.5	16	
Gate-Source Charge	Q _{gs}			3.5		
Gate-Drain Charge	Q _{gd}			4.2		
Gate Resistance	R _g	f = 1 MHz		3.3	5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 5.4 Ω I _D ≅ 5.6 A, V _{GEN} = 4.5 V, R _g = 1 Ω		20	30	ns
Rise Time	t _r			150	225	
Turn-Off Delay Time	t _{d(off)}			20	30	
Fall Time	t _f			60	90	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 5.4 Ω I _D ≅ 5.6 A, V _{GEN} = 10 V, R _g = 1 Ω		10	15	
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			25	40	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			4.2	A
Pulse Diode Forward Current ^a	I _{SM}				25	
Body Diode Voltage	V _{SD}	I _S = 2 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 5.5 A, di/dt = 100 A/μs, T _J = 25 °C		25	50	ns
Body Diode Reverse Recovery Charge	Q _{rr}			25	50	nC
Reverse Recovery Fall Time	t _a			19		ns
Reverse Recovery Rise Time	t _b			6		

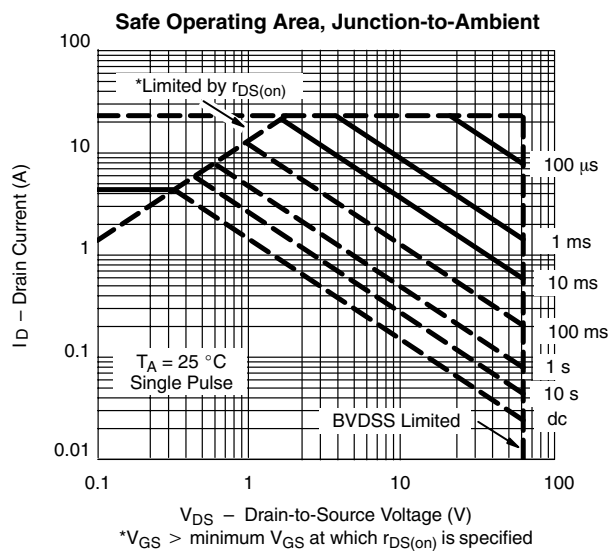
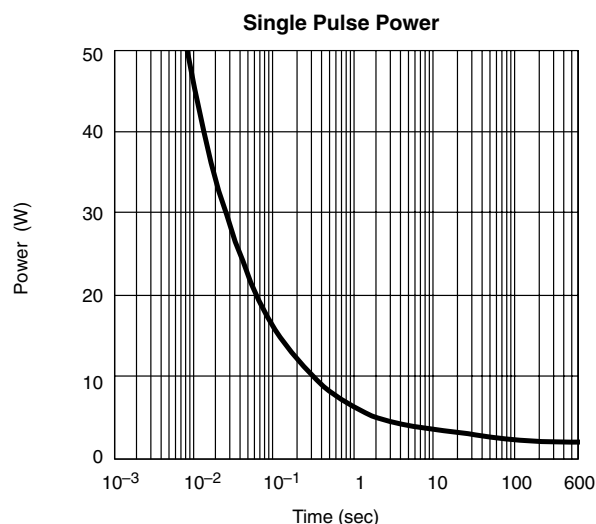
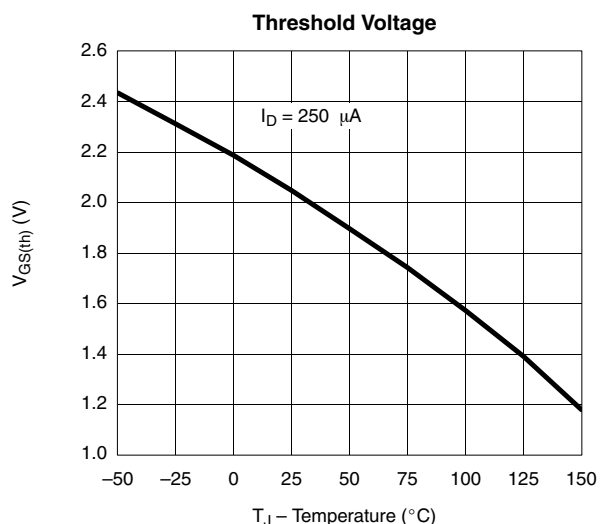
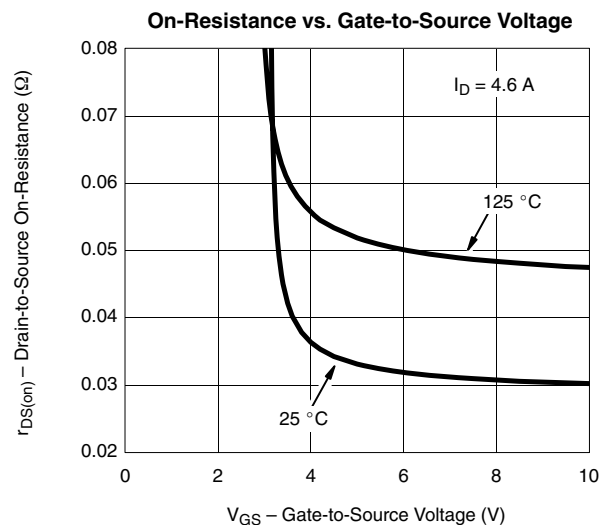
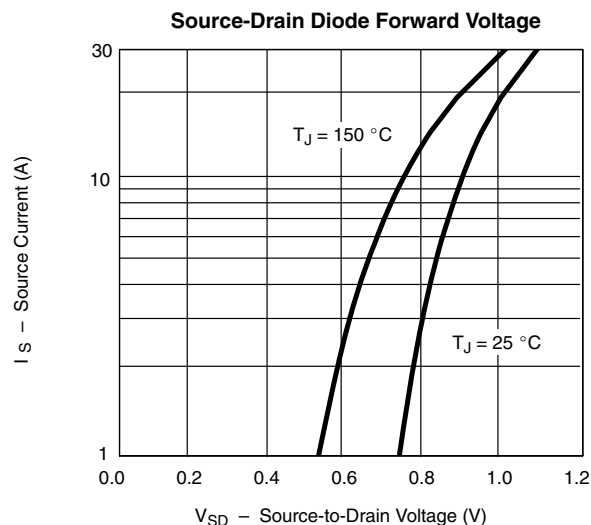
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

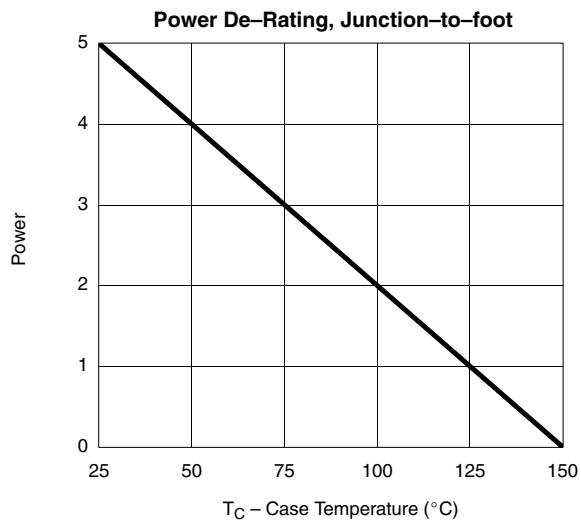
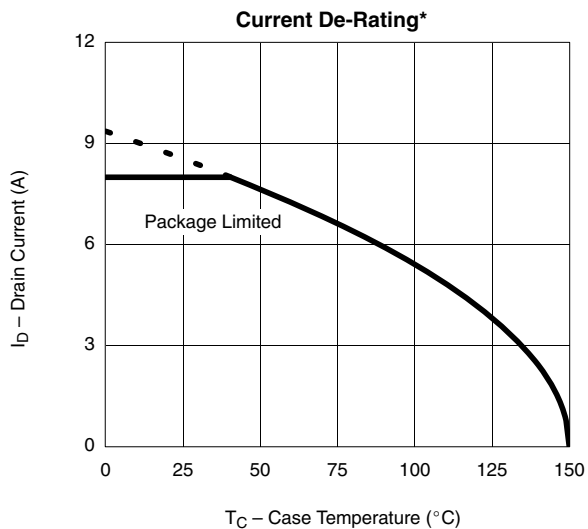
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)****Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

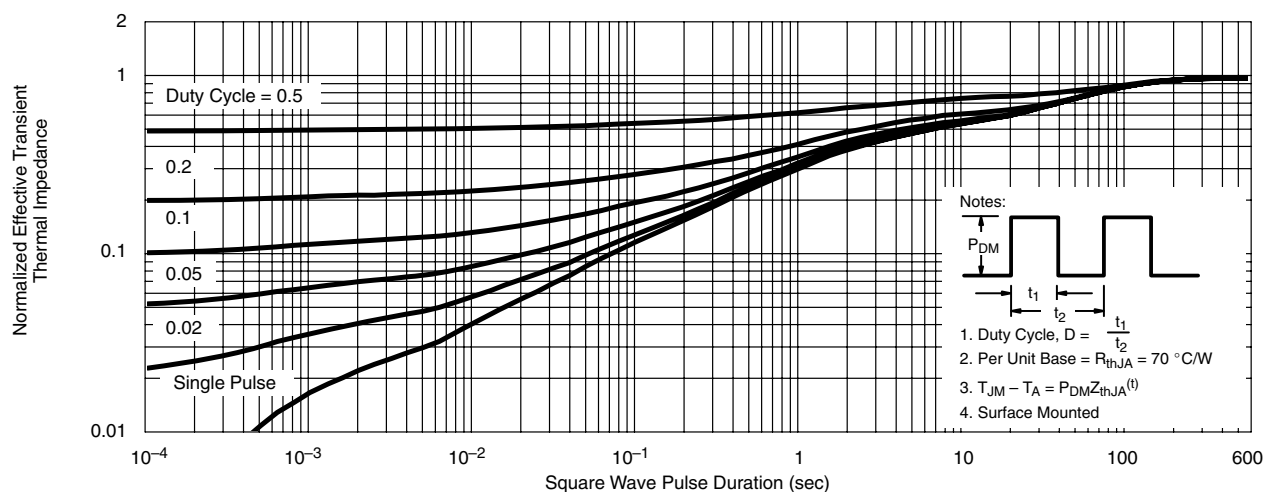
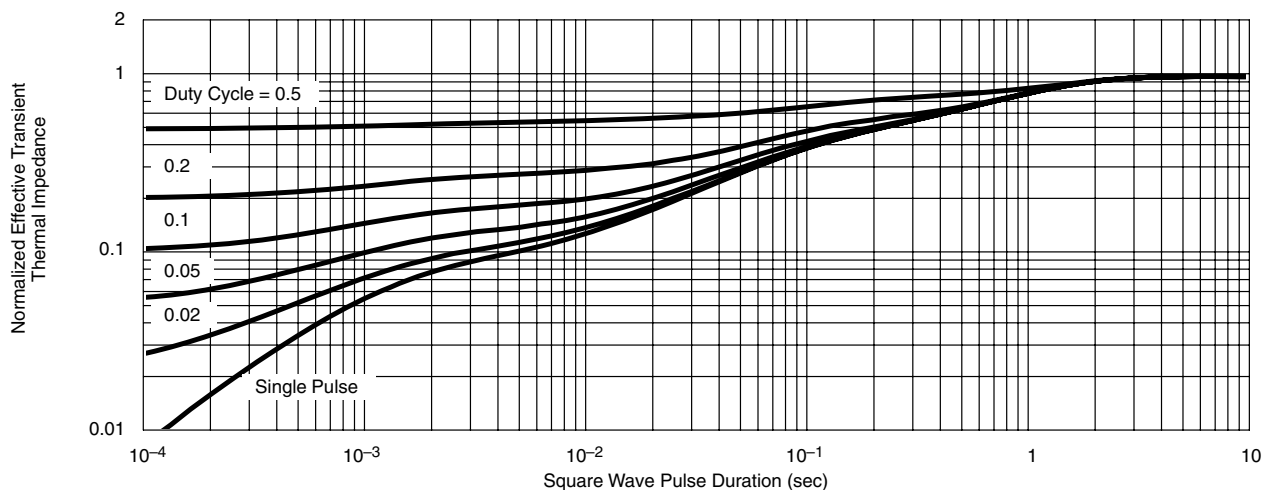




TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



*The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)
Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73664>.



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