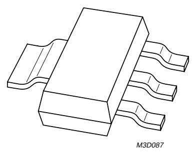


PHT6N06T

TrenchMOS™ standard level FET

Rev. 02 — 03 February 2003 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHT6N06T in SOT223.

1.2 Features

- Low on-state resistance
- Fast switching
- Low Q_{GD}
- Surface mounting package.

1.3 Applications

- DC to DC converters
- General purpose switching.

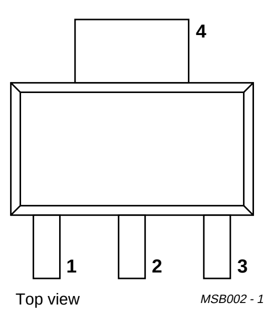
1.4 Quick reference data

- $V_{DS} \leq 55$ V
- $P_{tot} \leq 8.3$ W
- $I_D \leq 5.5$ A
- $R_{DSon} \leq 150$ mΩ

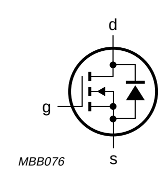
2. Pinning information

Table 1: Pinning - SOT223, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
4	drain (d)		



SOT223

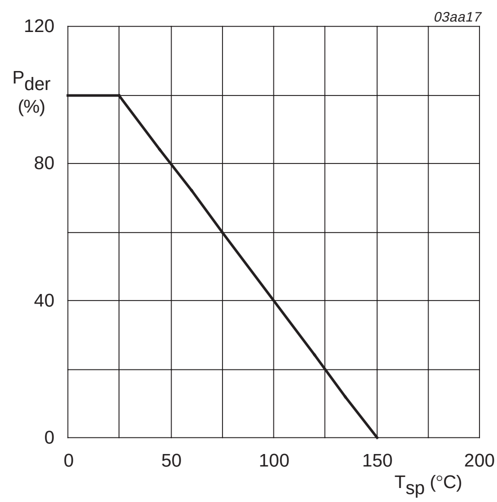


3. Limiting values

Table 2: Limiting values

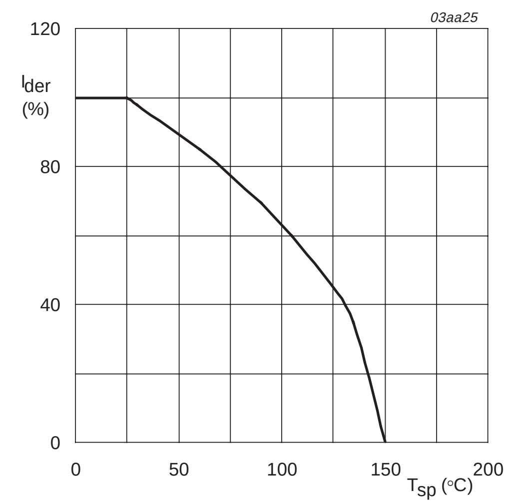
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C	-	55	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 10 V; Figure 2 and 3	-	5.5	A
		T_{sp} = 100 °C; V_{GS} = 10 V; Figure 2	-	3.8	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	22	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Figure 1	-	8.3	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{sp} = 25 °C	-	5.5	A
I_{SM}	peak source (diode forward) current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs	-	22	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

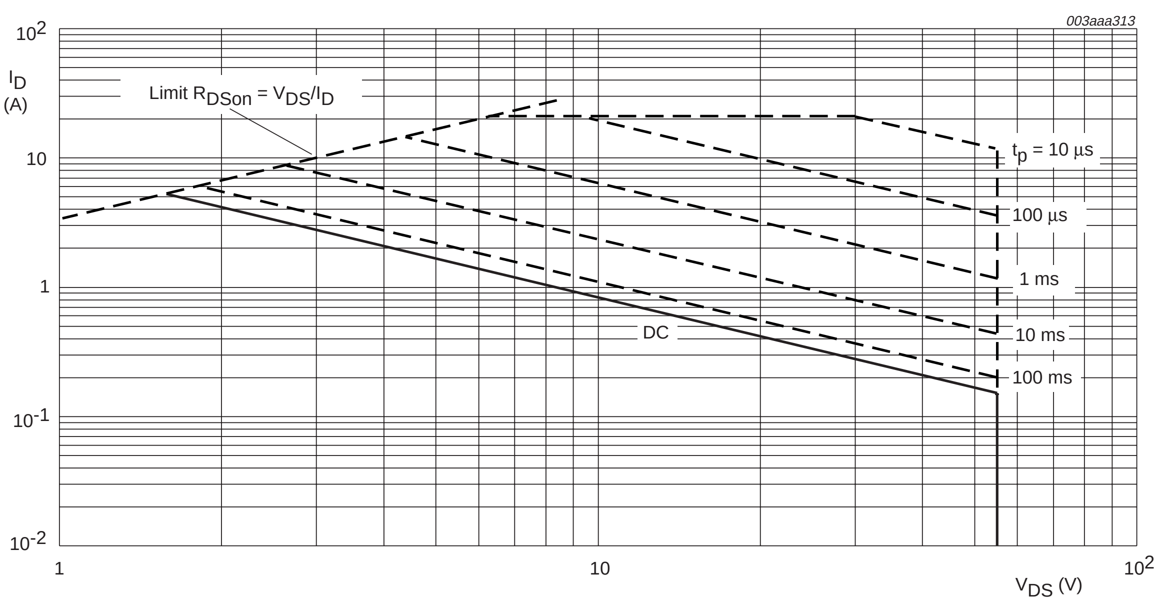
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 10$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25$ °C; I_{DM} is single pulse; $V_{GS} = 10$ V.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

9397 750 10633

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	70	-	K/W

4.1 Transient thermal impedance

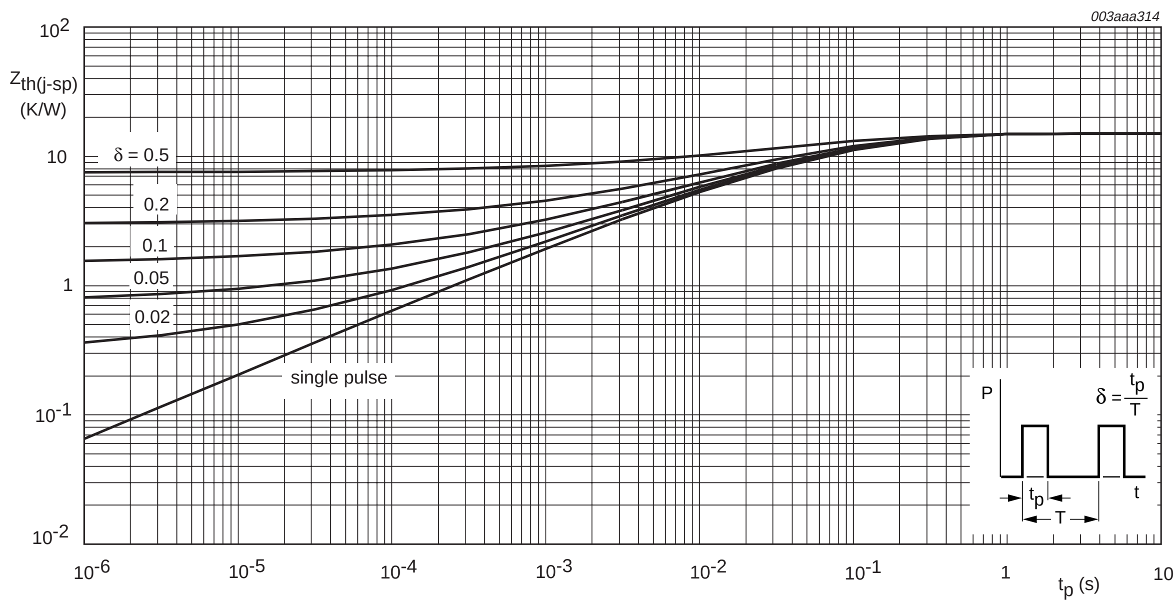


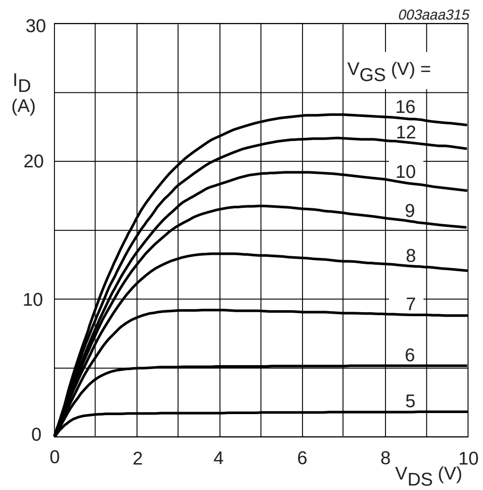
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

5. Characteristics

Table 4: Characteristics

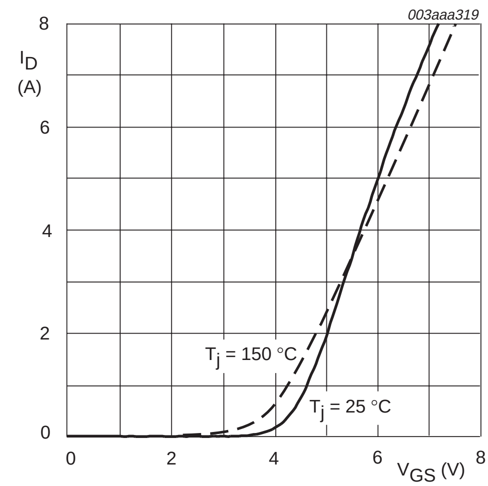
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	55	-	-	V
		T_j = –55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				V
		T_j = 25 °C	2	3	4	V
		T_j = 150 °C	1.2	–	–	V
		T_j = –55 °C	–	–	4.4	V
I_{DSS}	drain-source leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	10	µA
		T_j = 150 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; Figure 7 and 8				
		T_j = 25 °C	-	128	150	mΩ
		T_j = 150 °C	-	-	278	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 5 A; V_{DD} = 44 V; V_{GS} = 10 V; Figure 13	-	5.6	-	nC
Q_{gs}	gate-source charge		-	1.2	-	nC
Q_{gd}	gate-drain (Miller) charge		-	2.6	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 11	-	175	-	pF
C_{oss}	output capacitance		-	58	-	pF
C_{rss}	reverse transfer capacitance		-	40	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; I_D = 5 A; V_{GS} = 10 V; R_G = 6 Ω	-	4.9	-	ns
t_r	rise time		-	14.5	-	ns
$t_{d(off)}$	turn-off delay time		-	7.8	-	ns
t_f	fall time		-	4.5	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 5 A; V_{GS} = 0 V; Figure 12	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	32	-	ns
Q_r	recovered charge		-	50	-	nC



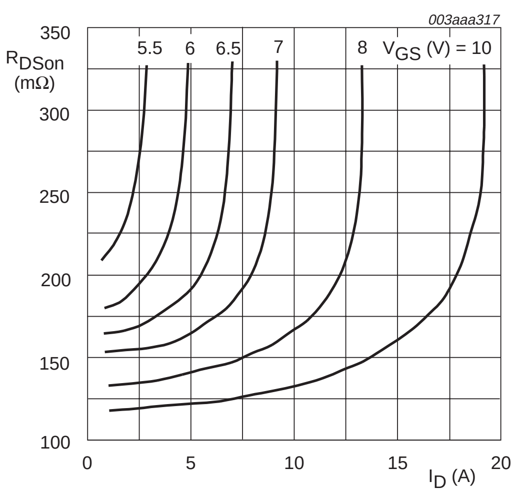
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



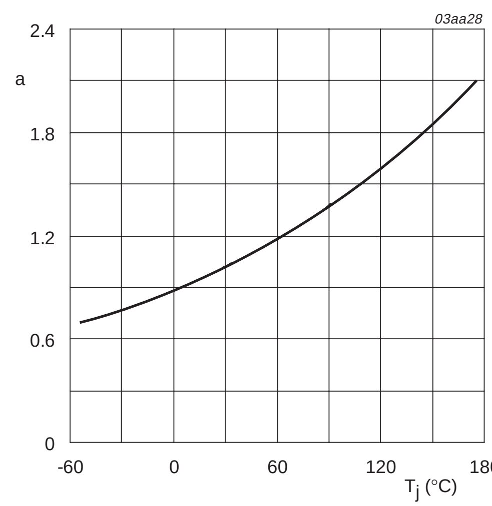
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



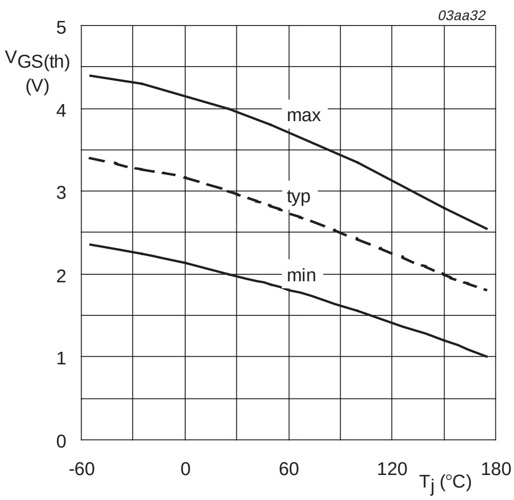
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



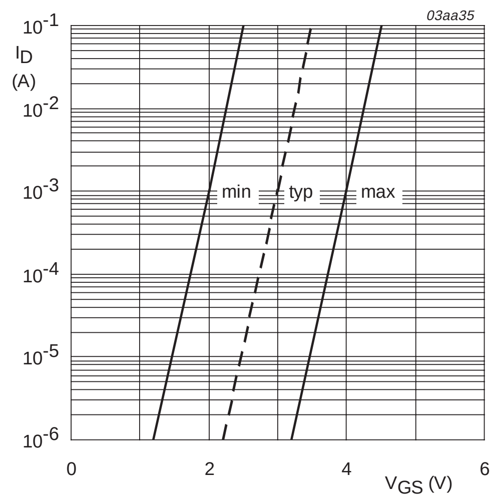
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



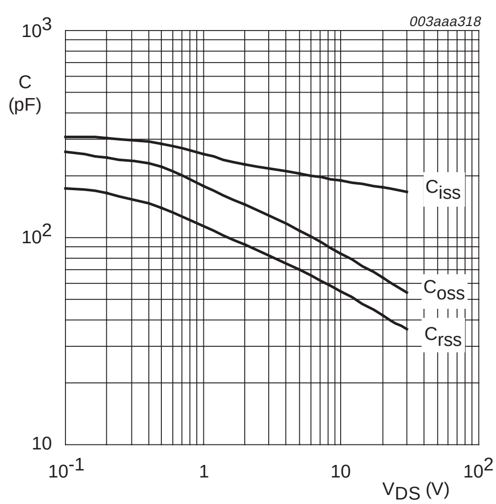
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



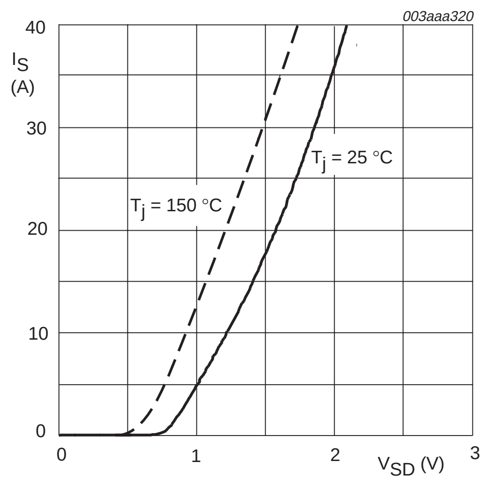
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



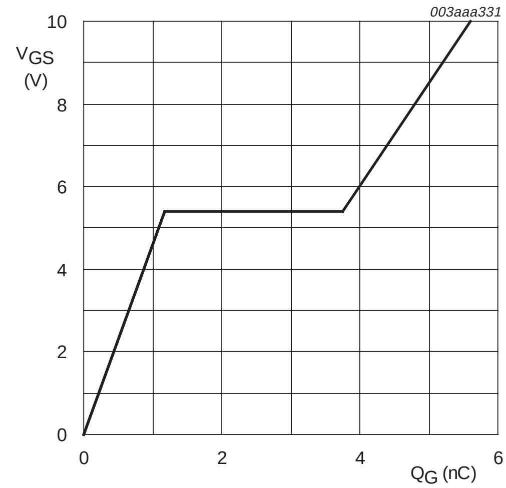
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

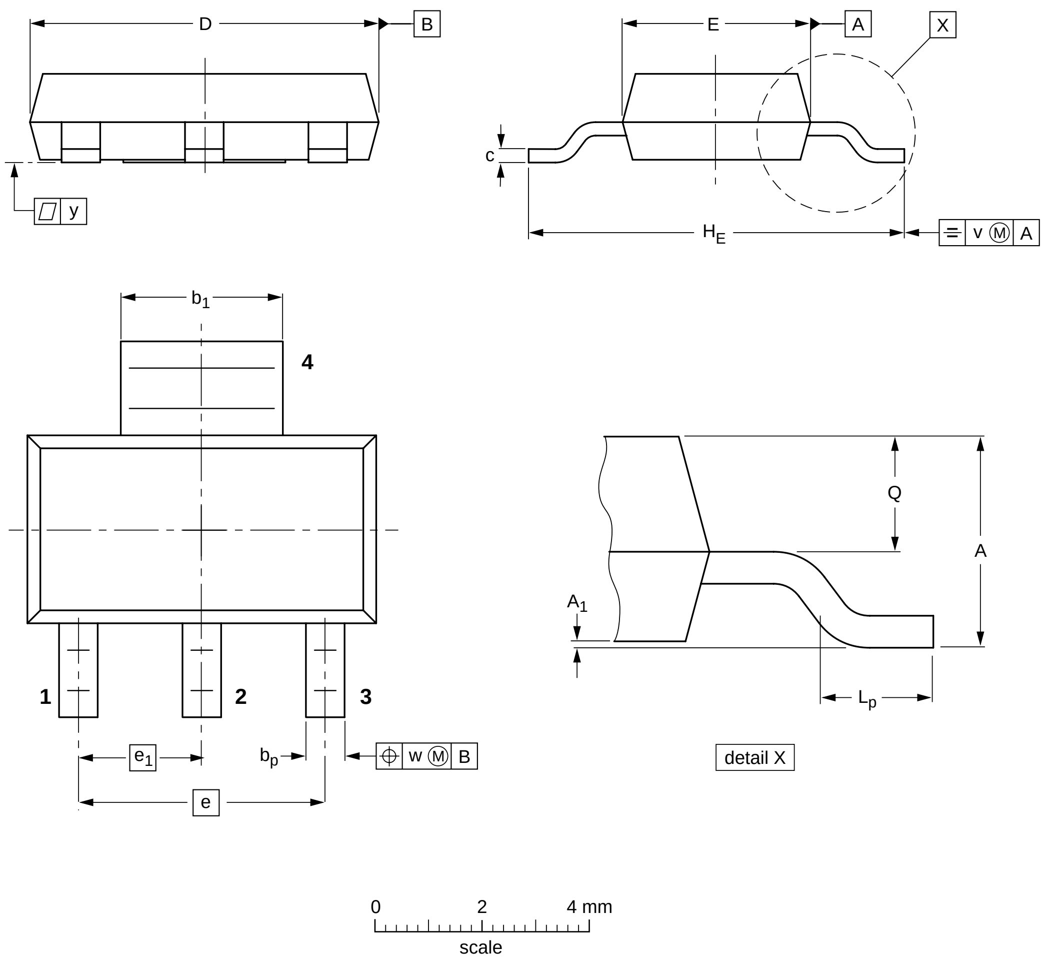


I_D = 5 A; V_{DD} = 44 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223			SC-73			~~97-02-28~~ 99-09-13

Fig 14. SOT223.

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
02	20030203	200209006	**Product data (9397 750 10633); supersedes product specification PHT6N06T Rev 1.000 of September 1997** Modifications: • The format of this specification has been redesigned to comply with Philips Semiconductors new presentation and information standard • ESD diodes removed from device and specification • Characteristics updated in Table 4.

8. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contents

1 Product profile 1
1.1 Description 1
1.2 Features 1
1.3 Applications 1
1.4 Quick reference data. 1
2 Pinning information 1
3 Limiting values. 2
4 Thermal characteristics. 4
4.1 Transient thermal impedance 4
5 Characteristics. 5
6 Package outline 9
7 Revision history. 10
8 Data sheet status 11
9 Definitions 11
10 Disclaimers. 11
11 Trademarks. 11

Date of release: 03 February 2003 **Document order number: 9397 750 10633**