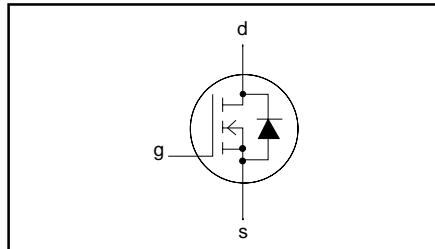


N-channel TrenchMOS™ transistor**PHB45NQ10T, PHP45NQ10T
PHW45NQ10T****FEATURES**

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL**QUICK REFERENCE DATA**

$V_{DSS} = 100 \text{ V}$
 $I_D = 47 \text{ A}$
 $R_{DS(ON)} \leq 25 \text{ m}\Omega$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope using 'trench' technology.

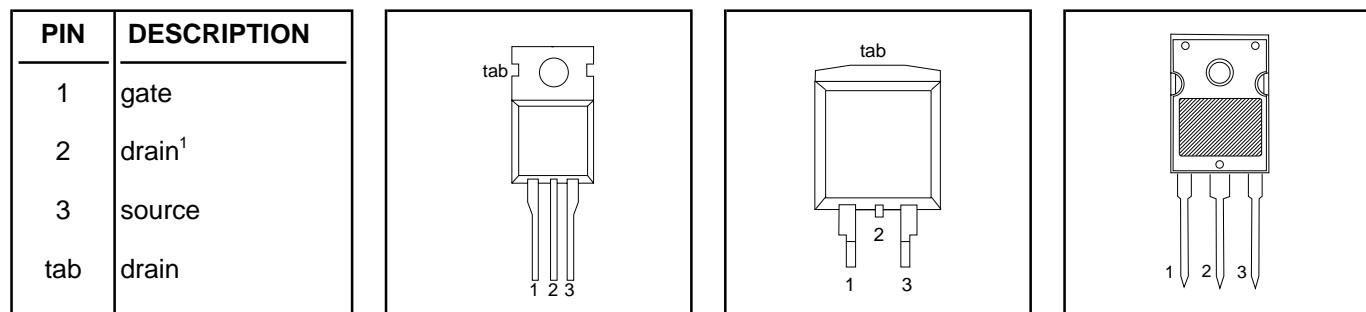
Applications:-

- d.c. to d.c. converters
- switched mode power supplies

The PHP45NQ10T is supplied in the SOT78 (TO220AB) conventional leaded package.

The PHB45NQ10T is supplied in the SOT404 (D²PAK) surface mounting package.

The PHW45NQ10T is supplied in the SOT429 (TO247) conventional leaded package.

PINNING**SOT78 (TO220AB)****SOT404 (D²PAK)****SOT429 (TO247)****LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25^\circ\text{C}$ to 175°C	-	100	V
V_{DGR}	Drain-gate voltage	$T_j = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 20 \text{ k}\Omega$	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	$T_{mb} = 25^\circ\text{C}$; $V_{GS} = 10 \text{ V}$	-	47	A
I_{DM}	Pulsed drain current	$T_{mb} = 100^\circ\text{C}$; $V_{GS} = 10 \text{ V}$	-	33	A
P_D	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	188	A
T_j, T_{stg}	Operating junction and storage temperature	$T_{mb} = 25^\circ\text{C}$	-	150	W
			-55	175	°C

¹ It is not possible to make connection to pin 2 of the SOT404 package.

N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
PHW45NQ10T**AVALANCHE ENERGY LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E _{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I _{AS} = 40 A; t _p = 100 µs; T _j prior to avalanche = 25°C; V _{DD} ≤ 25 V; R _{GS} = 50 Ω; V _{GS} = 10 V; refer to fig:15	-	260	mJ
I _{AS}	Non-repetitive avalanche current		-	47	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R _{th j-mb}	Thermal resistance junction to mounting base		-	-	1	K/W
R _{th j-a}	Thermal resistance junction to ambient	SOT78 package, in free air SOT429 package, in free air SOT404 package, pcb mounted, minimum footprint	-	60 45 50	- - -	K/W K/W K/W

ELECTRICAL CHARACTERISTICST_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA;	100	-	-	V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA	89 2	- 3	4	V
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A	1	-	-	V
I _{GSS}	Gate source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	-	22	25	mΩ
I _{DSS}	Zero gate voltage drain current	V _{DS} = 100 V; V _{GS} = 0 V;	-	-	68	mΩ
		T _j = 175°C	-	0.02	100	nA
			-	0.05	10	µA
			-	-	500	µA
Q _{g(tot)}	Total gate charge	I _D = 45 A; V _{DD} = 80 V; V _{GS} = 10 V	-	61	-	nC
Q _{gs}	Gate-source charge		-	13	-	nC
Q _{gd}	Gate-drain (Miller) charge		-	25	-	nC
t _{d on}	Turn-on delay time	V _{DD} = 50 V; R _D = 1.8 Ω;	-	18	-	ns
t _r	Turn-on rise time	V _{GS} = 10 V; R _G = 5.6 Ω	-	72	-	ns
t _{d off}	Turn-off delay time	Resistive load	-	69	-	ns
t _f	Turn-off fall time		-	58	-	ns
L _d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L _d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 and SOT429 packages)	-	4.5	-	nH
L _s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C _{iss}	Input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	2600	-	pF
C _{oss}	Output capacitance		-	340	-	pF
C _{rss}	Feedback capacitance		-	195	-	pF

N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
PHW45NQ10T**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS** $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_s	Continuous source current (body diode)		-	-	47	A
I_{sm}	Pulsed source current (body diode)		-	-	188	A
V_{sd}	Diode forward voltage	$I_F = 25 \text{ A}; V_{GS} = 0 \text{ V}$	-	0.87	1.2	V
t_{rr}	Reverse recovery time	$I_F = 20 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s};$	-	82	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0 \text{ V}; V_R = 25 \text{ V}$	-	0.26	-	μC

N-channel TrenchMOS™ transistor

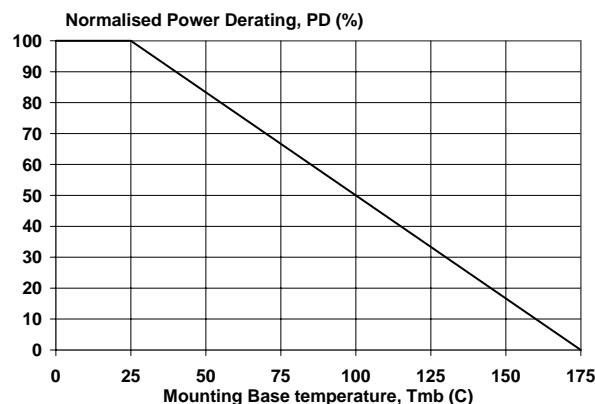
PHB45NQ10T, PHP45NQ10T
PHW45NQ10T

Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D, 25^\circ C} = f(T_{mb})$

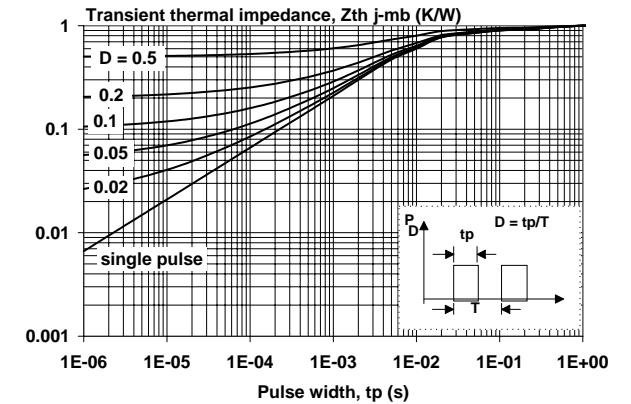


Fig.4. Transient thermal impedance.
 $Z_{th,j-mb} = f(t_p)$; parameter $D = t_p/T$

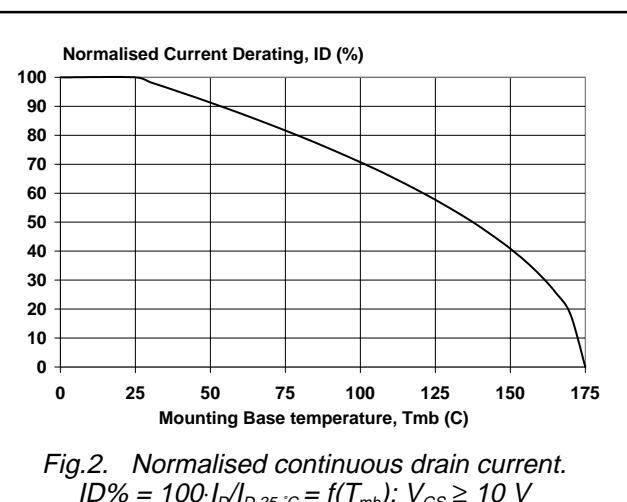


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D, 25^\circ C} = f(T_{mb})$; $V_{GS} \geq 10$ V

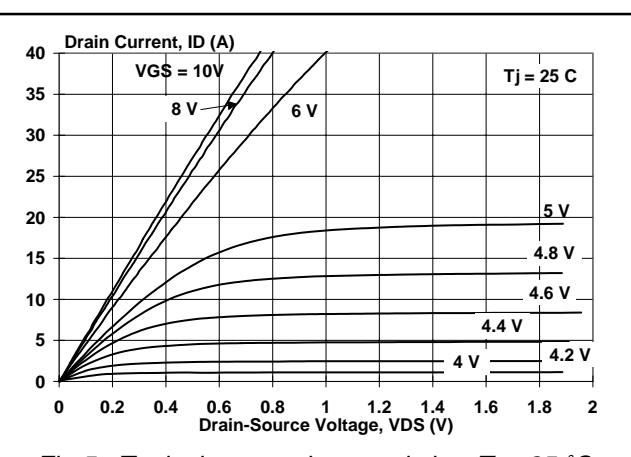


Fig.5. Typical output characteristics, $T_j = 25$ °C.
 $I_D = f(V_{DS})$

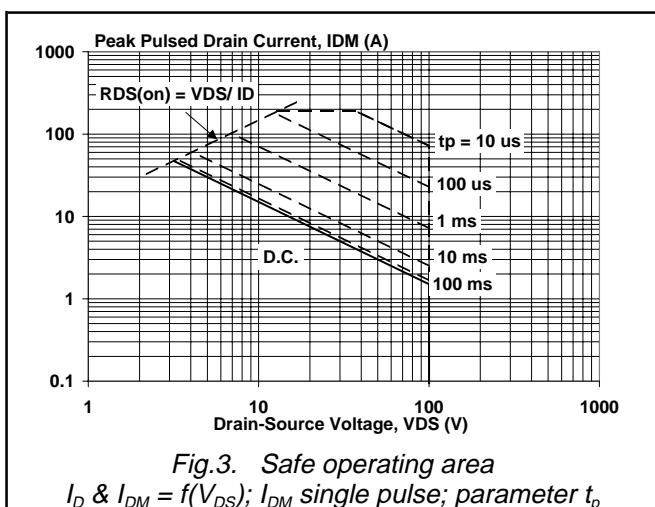


Fig.3. Safe operating area
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

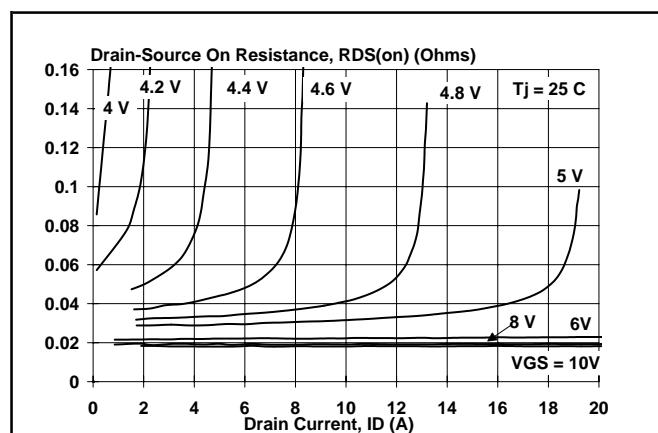


Fig.6. Typical on-state resistance, $T_j = 25$ °C.
 $R_{DS(ON)} = f(I_D)$

N-channel TrenchMOS™ transistor

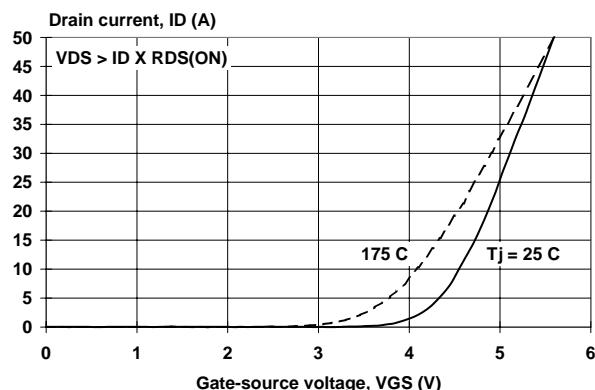
PHB45NQ10T, PHP45NQ10T
PHW45NQ10T

Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$

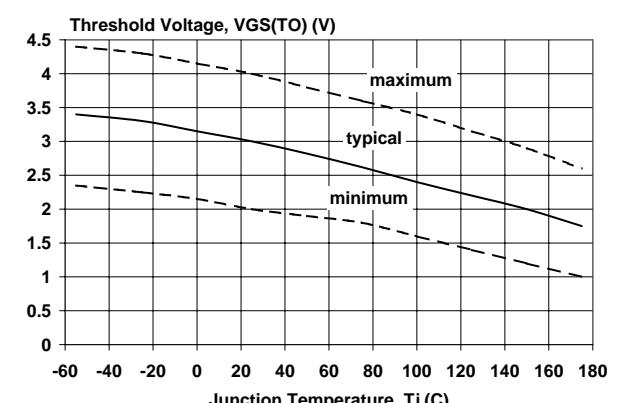


Fig.10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

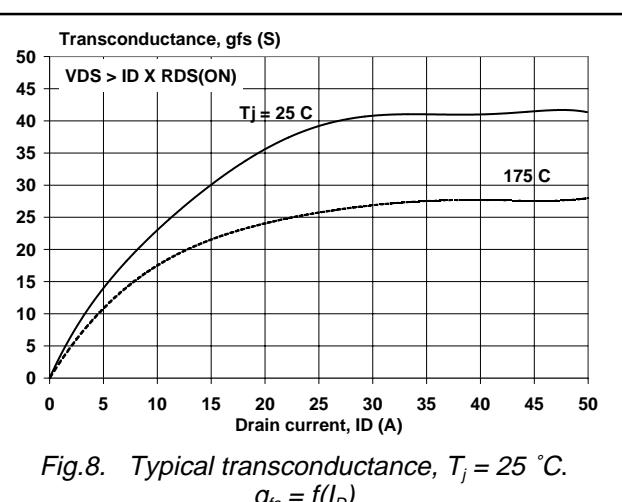


Fig.8. Typical transconductance, $T_j = 25^\circ\text{C}$.
 $g_{fs} = f(I_D)$

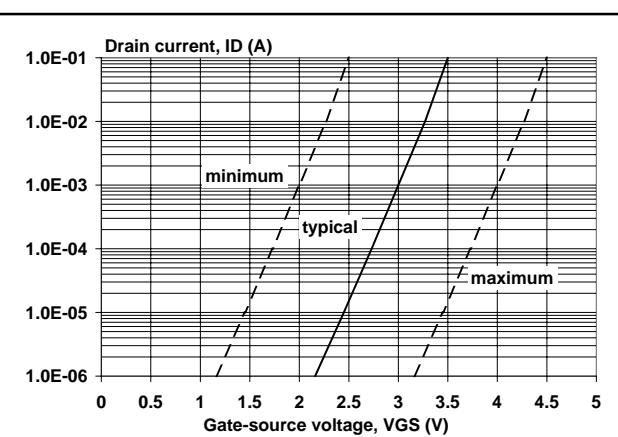


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ\text{C}$

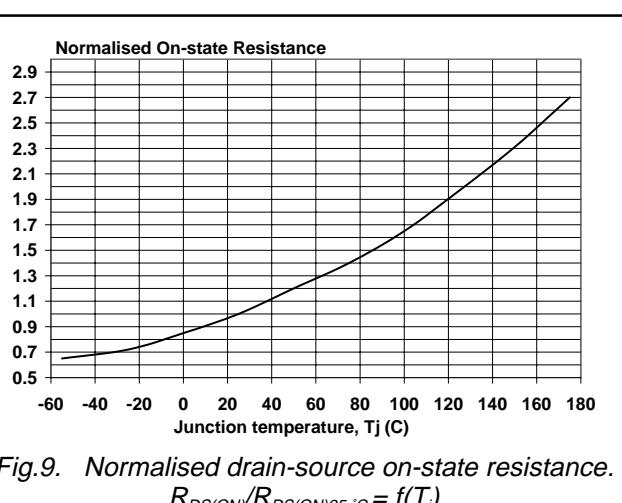


Fig.9. Normalised drain-source on-state resistance.
 $R_{DS(ON)}/R_{DS(ON)25^\circ\text{C}} = f(T_j)$

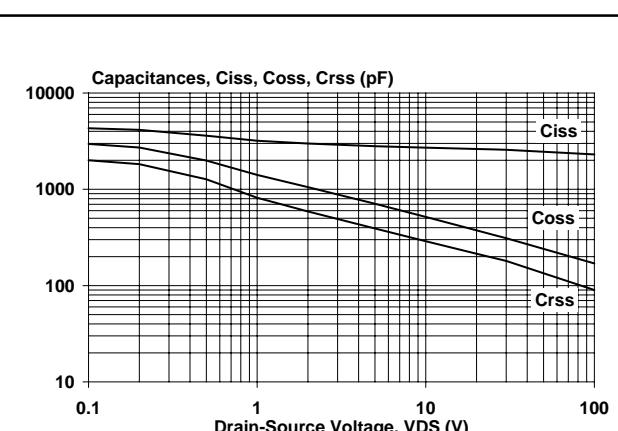


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

N-channel TrenchMOS™ transistor

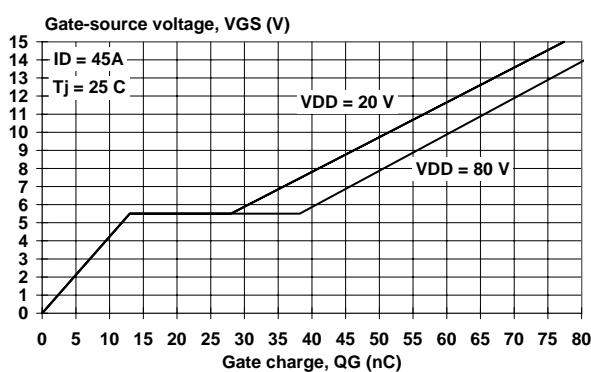
PHB45NQ10T, PHP45NQ10T
PHW45NQ10T

Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$

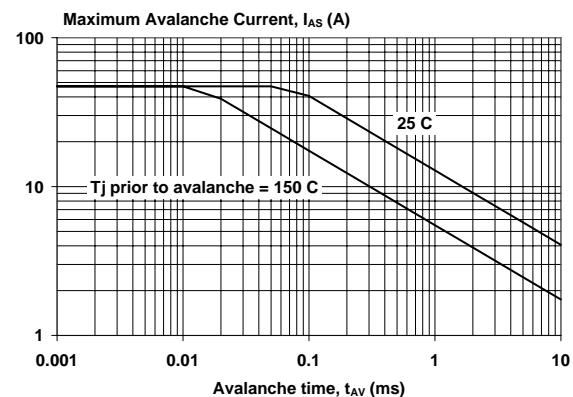


Fig.15. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_{AV}); unclamped inductive load

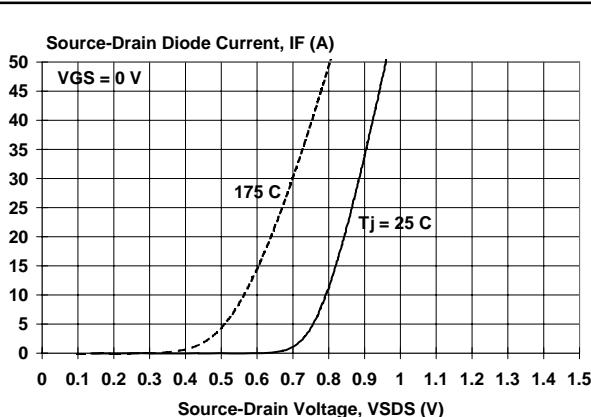


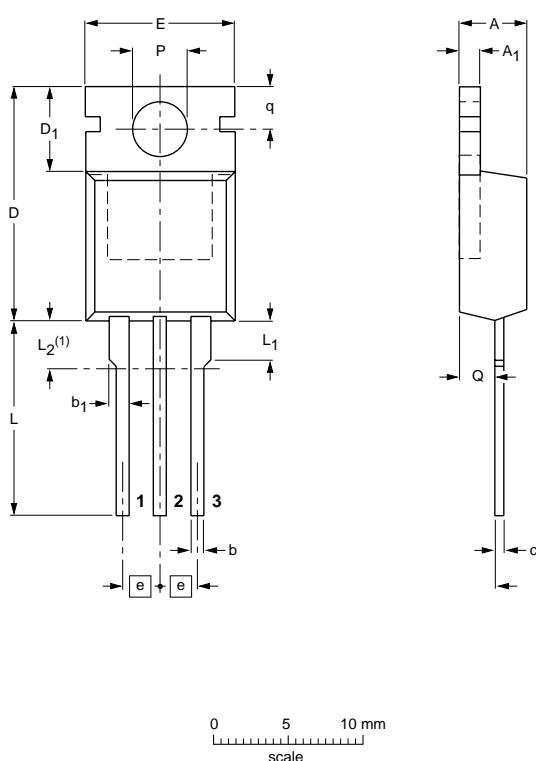
Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j

N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
PHW45NQ10T

MECHANICAL DATA

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220 SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁	L ₂ ⁽¹⁾ max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0 3.6	3.8 3.0	2.6 2.7	2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		TO-220				97-06-11

Fig. 16. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

Notes

- This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
- Refer to mounting instructions for SOT78 (TO220AB) package.
- Epoxy meets UL94 V0 at 1/8".

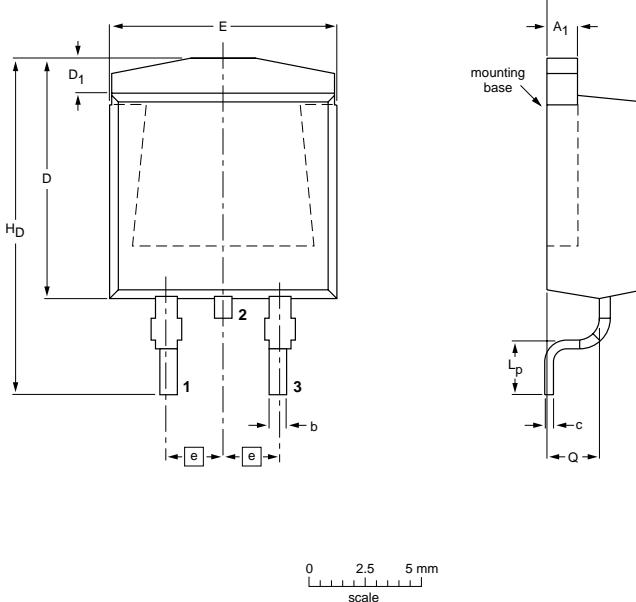
N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
PHW45NQ10T

MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D2-PAK); 3 leads
(one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.40 14.80	2.60 2.20

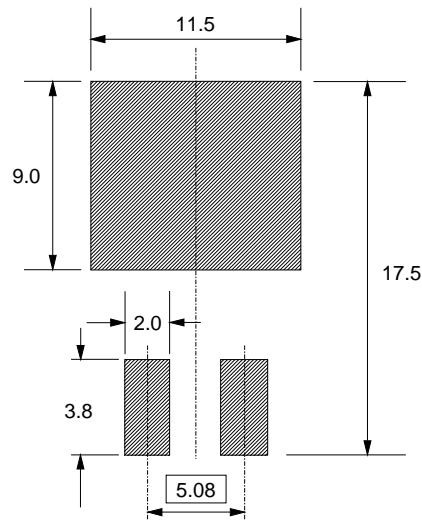
OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT404							-98-12-14- 99-06-25

Fig.17. SOT404 surface mounting package. Centre pin connected to mounting base.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
PHW45NQ10T**MOUNTING INSTRUCTIONS***Dimensions in mm**Fig.18. SOT404 : soldering pattern for surface mounting.*

N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
PHW45NQ10T

MECHANICAL DATA

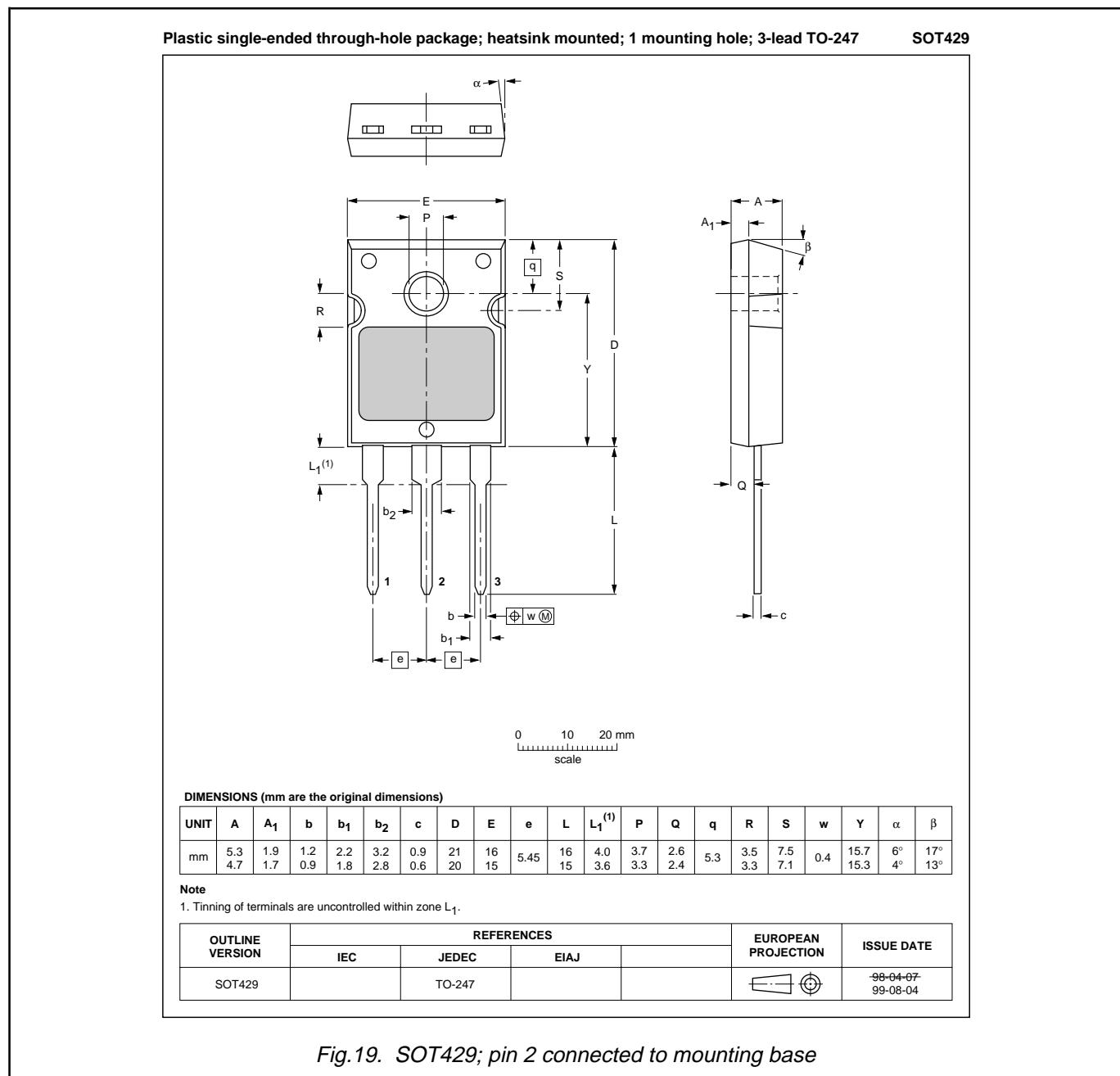


Fig.19. SOT429; pin 2 connected to mounting base

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT429 envelope.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor

PHB45NQ10T, PHP45NQ10T
PHW45NQ10T

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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