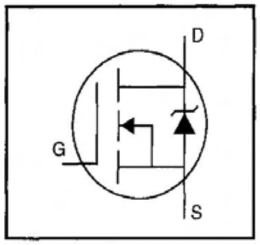
International Rectifier

PD-95980

IRLD110PbF

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at V_{GS}=4V & 5V
- 175°C Operating Temperature
- Lead-Free



V_{DSS} = 100V

$R_{DS(on)}$ = 0.54Ω

I_D = 1.0A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.

HD-1

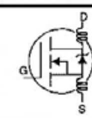
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 5.0 V	1.0	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 5.0 V	0.70	
I_{DM}	Pulsed Drain Current ①	8.0	
P_D @ T_C = 25°C	Power Dissipation	1.3	W
	Linear Derating Factor	0.0083	W/°C
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	490	mJ
I_{AR}	Avalanche Current ①	1.0	A
E_{AR}	Repetitive Avalanche Energy ①	0.13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

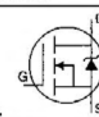
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS}=0V, I_D= 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.54	Ω	V_{GS}=5.0V, I_D=0.60A ④
		—	—	0.76		V_{GS}=4.0V, I_D=0.50A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS}=V_{GS}, I_D= 250µA
g_{fs}	Forward Transconductance	1.3	—	—	S	V_{DS}=50V, I_D=0.60A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS}=100V, V_{GS}=0V
		—	—	250		V_{DS}=80V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=10V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-10V
Q_g	Total Gate Charge	—	—	6.1	nC	I_D=5.6A
Q_{gs}	Gate-to-Source Charge	—	—	2.6		V_{DS}=80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	3.3		V_{GS}=5.0V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.3	—	ns	V_{DD}=50V
t_r	Rise Time	—	47	—		I_D=5.6A
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		R_G=12Ω
t_f	Fall Time	—	17	—		R_D=8.4Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	6.0	—		
C_{iss}	Input Capacitance	—	250	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	80	—		V_{DS}= 25V
C_{rss}	Reverse Transfer Capacitance	—	15	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	8.0		
V_{SD}	Diode Forward Voltage	—	—	2.5	V	T_J=25°C, I_S=1.0A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	110	130	ns	T_J=25°C, I_F=5.6A
Q_{rr}	Reverse Recovery Charge	—	0.50	0.65	µC	di/dt=100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=25V, starting T_J=25°C, L=183mH R_G=25Ω, I_{AS}=2.0A (See Figure 12)

③ $I_{SD}\leq$5.6A, di/dt≤75A/µs, $V_{DD}\leq V_{(BR)DSS}$, $T_J\leq$175°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

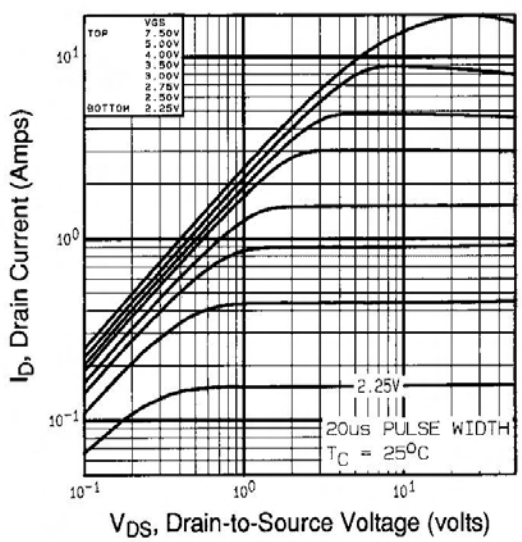


Fig 1. Typical Output Characteristics, T_C=25°C

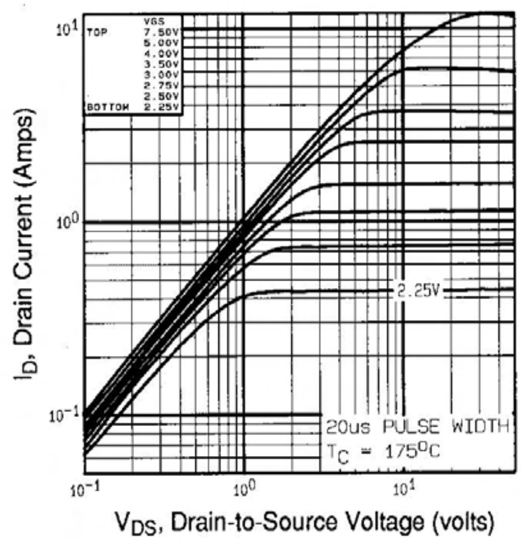


Fig 2. Typical Output Characteristics, T_C=175°C

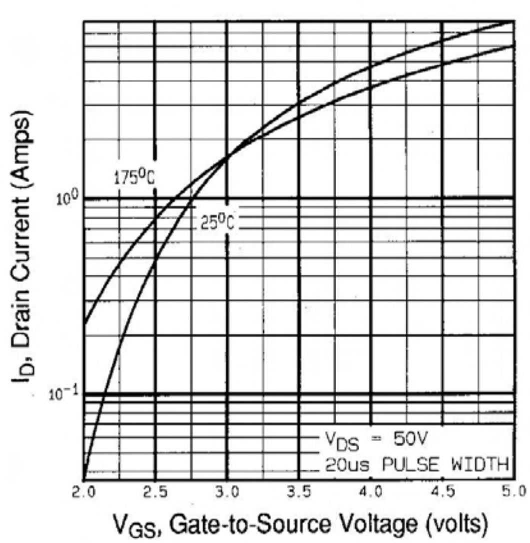


Fig 3. Typical Transfer Characteristics

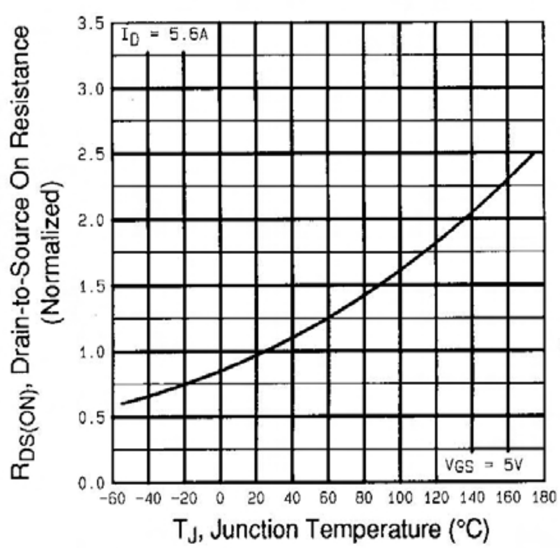


Fig 4. Normalized On-Resistance Vs. Temperature

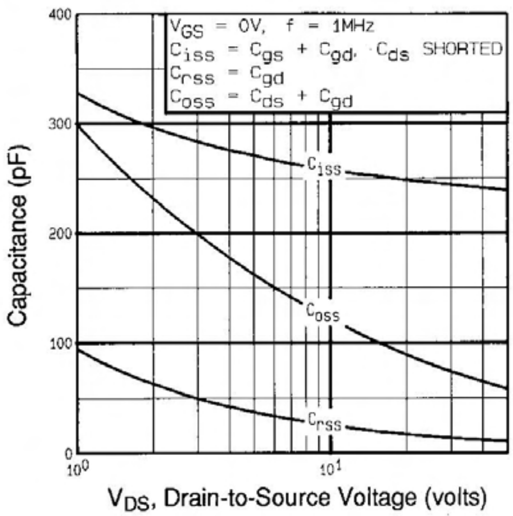


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

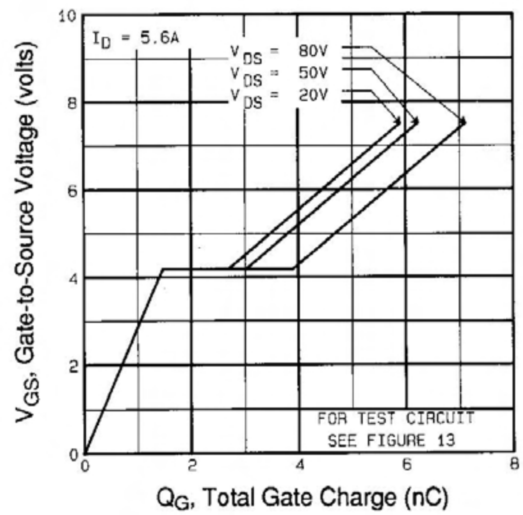


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

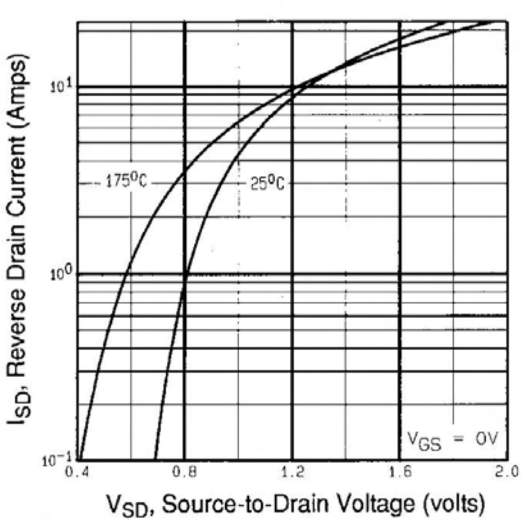


Fig 7. Typical Source-Drain Diode Forward Voltage

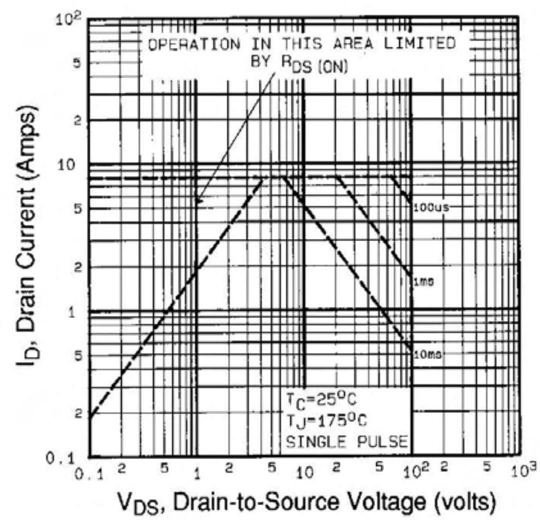


Fig 8. Maximum Safe Operating Area

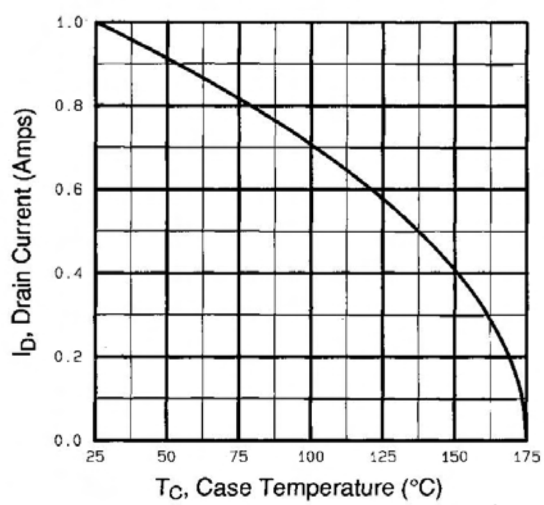


Fig 9. Maximum Drain Current Vs. Case Temperature

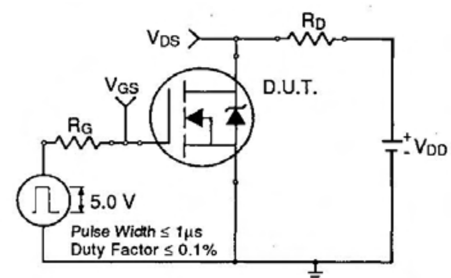


Fig 10a. Switching Time Test Circuit

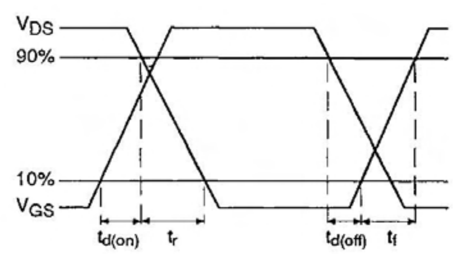


Fig 10b. Switching Time Waveforms

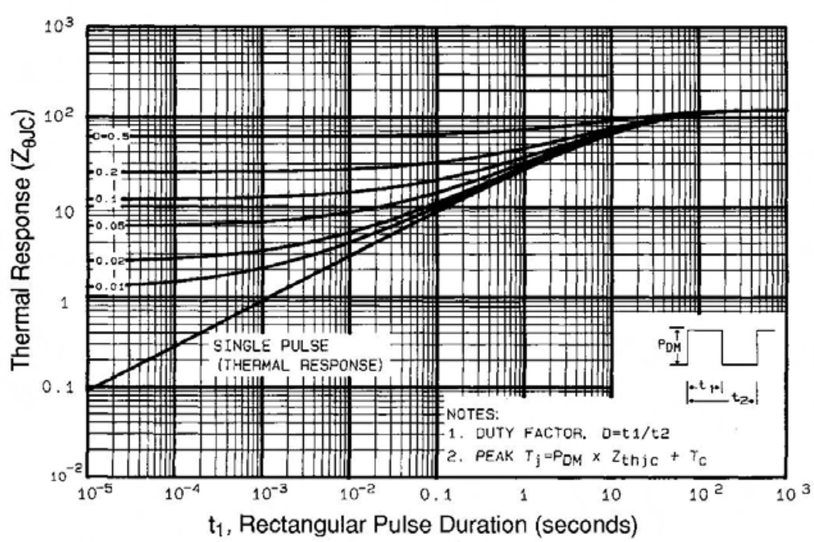


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

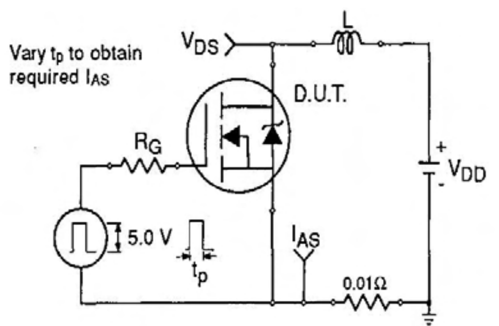


Fig 12a. Unclamped Inductive Test Circuit

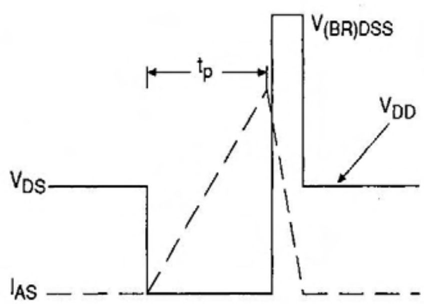


Fig 12b. Unclamped Inductive Waveforms

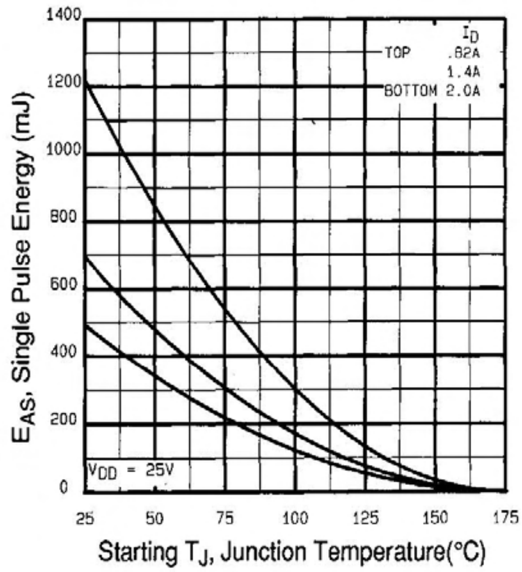


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

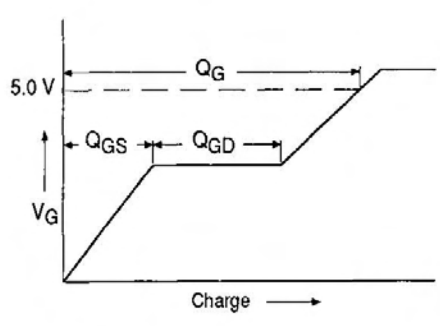


Fig 13a. Basic Gate Charge Waveform

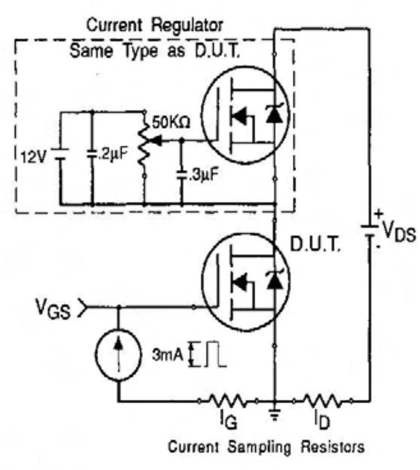
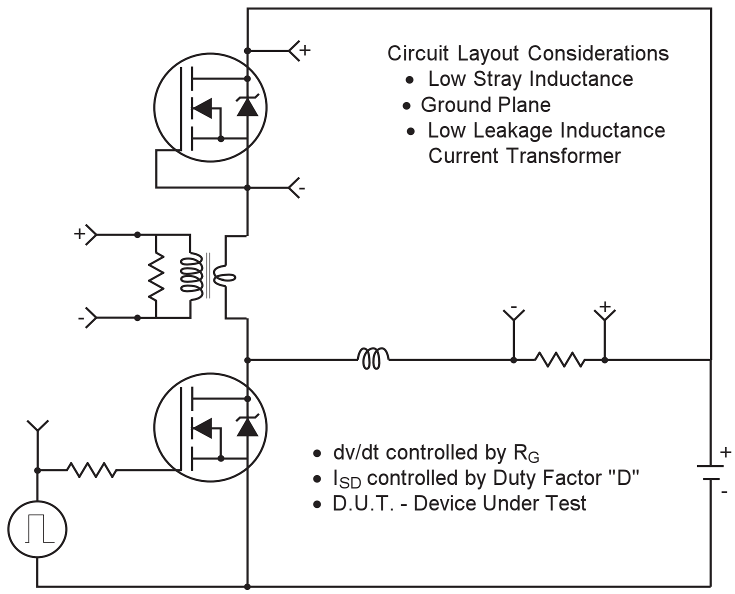


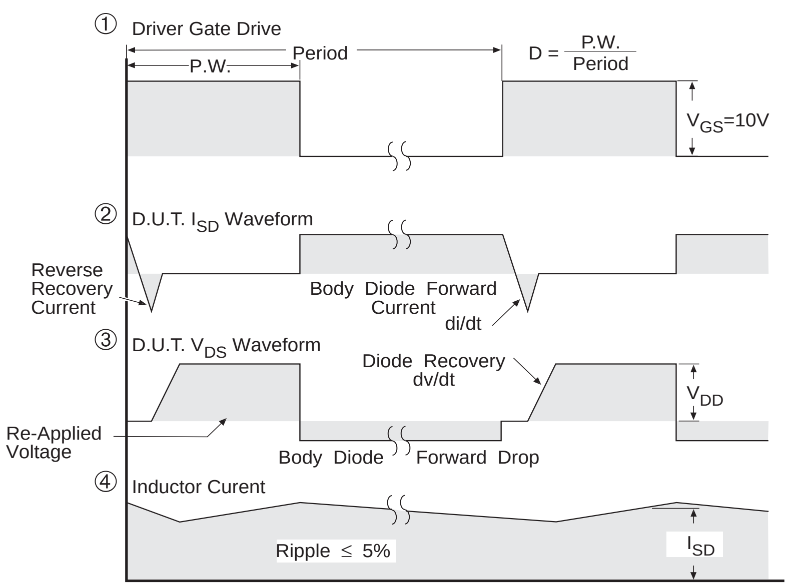
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

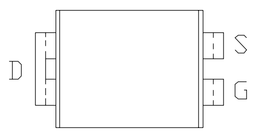
** Use P-Channel Driver for P-Channel Measurements



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

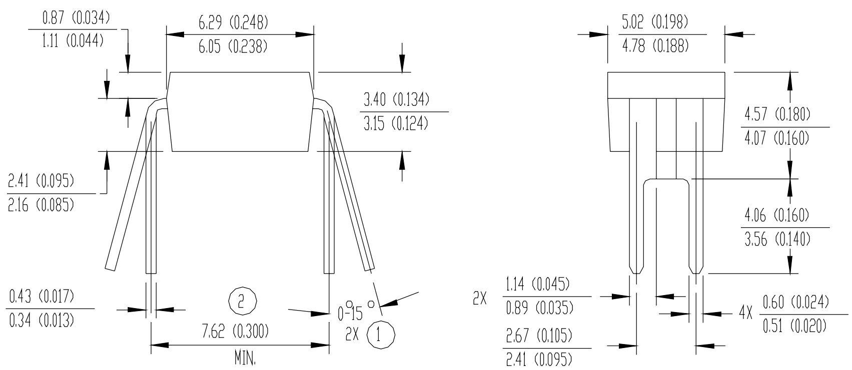
Fig 14 For N Channel HEXFETS

Hexdip Package Outline



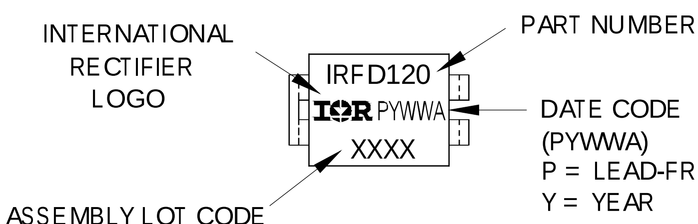
NOTES:

1. APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
2. APPLIES TO INSTALLED LEAD CENTERS
3. CONTROLLING DIMENSION: INCH.
4. DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
5. CASE STYLE HD-1 (SIMILAR TO JEDEC OUTLINE MO-001AN)
6. DIMENSIONS SHOWN ARE BEFORE SOLDER DIP
   SOLDER DIP MAX. + 0.16 (0.006)



Hexdip Part Marking Information

EXAMPLE: THIS IS AN IRFD120



P = LEAD-FREE (optional)
Y = YEAR
WW = WEEK
A = ASSEMBLY SITE CODE

Data and specifications subject to change without notice.

International
IOR Rectifier

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