International
IOR Rectifier

PD- 92005

SMPS MOSFET

IRF740AS/L

HEXFET® Power MOSFET

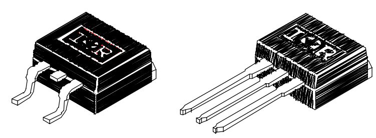
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching

V_{DSS}	Rds(on) max	I_D
400V	**0.55Ω**	**10A**

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss specified (See AN 1001)



D^2 Pak   TO-262

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V⑥	10	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V⑥	6.3	
I_{DM}	Pulsed Drain Current ①⑥	40	
P_D @T_A = 25°C	Power Dissipation	3.1	W
P_D @T_C = 25°C	Power Dissipation	125	
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③⑥	5.9	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies:

- Single transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset
  (Both for US Line Input only)

Notes ① through ⑤ are on page 10

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.48	——	V/°C	Reference to 25°C, I_D = 1mA⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.55	Ω	V_{GS} = 10V, I_D = 6.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 400V, V_{GS} = 0V
		——	——	250		V_{DS} = 320V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	4.9	——	——	S	V_{DS} = 50V, I_D = 6.0A⑥
Q_g	Total Gate Charge	——	——	36	nC	I_D = 10A
Q_{gs}	Gate-to-Source Charge	——	——	9.9		V_{DS} = 320V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	16		V_{GS} = 10V, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	——	10	——	ns	V_{DD} = 200V
t_r	Rise Time	——	35	——		I_D = 10A
$t_{d(off)}$	Turn-Off Delay Time	——	24	——		R_G = 10Ω
t_f	Fall Time	——	22	——		R_D = 19.5Ω,See Fig. 10 ④⑥
C_{iss}	Input Capacitance	——	1030	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	170	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	7.7	——		ƒ = 1.0MHz, See Fig. 5⑥
C_{oss}	Output Capacitance	——	1490	——		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	52	——		V_{GS} = 0V, V_{DS} = 320V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	61	——		V_{GS} = 0V, V_{DS} = 0V to 320V ⑤⑥

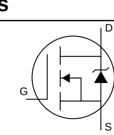
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②⑥	——	630	mJ
I_{AR}	Avalanche Current①	——	10	A
E_{AR}	Repetitive Avalanche Energy①	——	12.5	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	——	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	40		
V_{SD}	Diode Forward Voltage	——	——	2.0	V	T_J = 25°C, I_S = 10A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	240	360	ns	T_J = 25°C, I_F = 10A
Q_{rr}	Reverse RecoveryCharge	——	1.9	2.9	µC	di/dt = 100A/µs ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

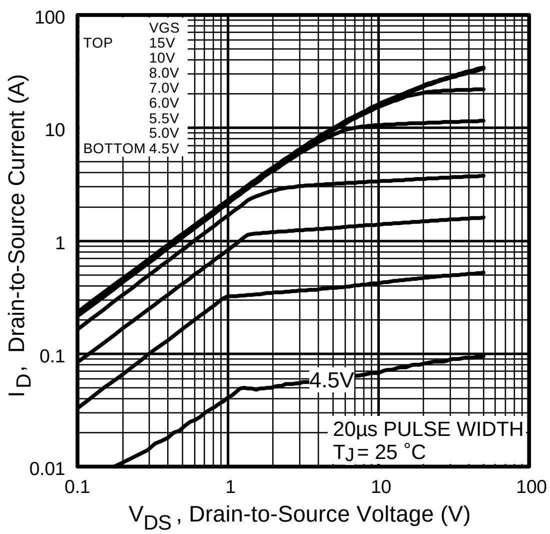


Fig 1. Typical Output Characteristics

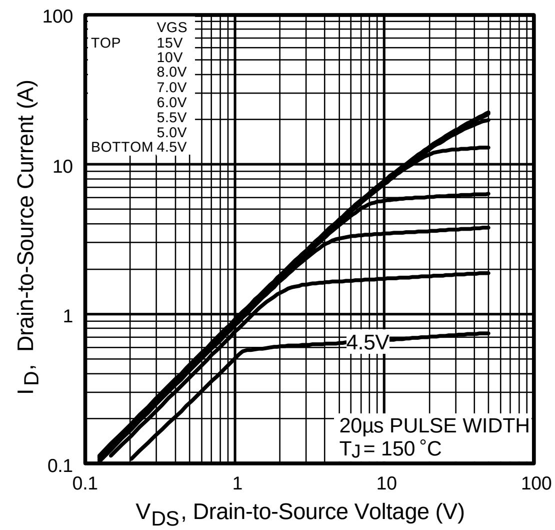


Fig 2. Typical Output Characteristics

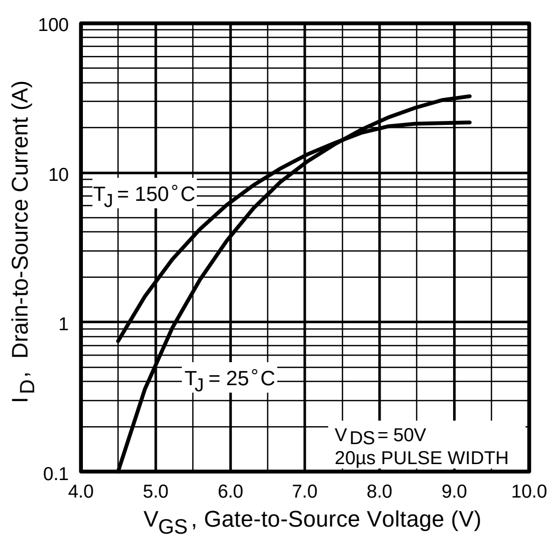


Fig 3. Typical Transfer Characteristics

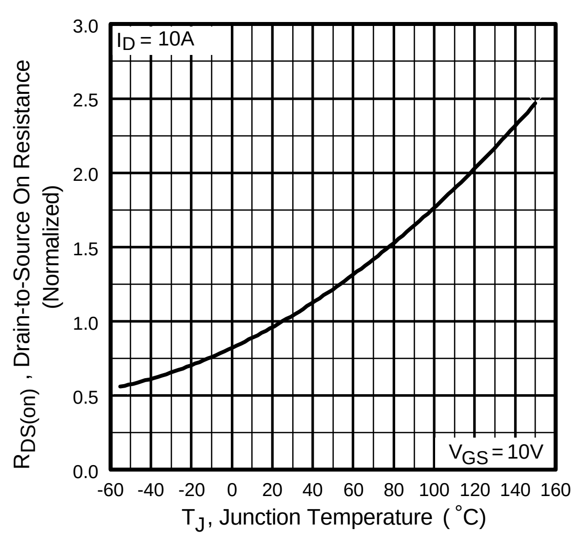


Fig 4. Normalized On-Resistance Vs. Temperature

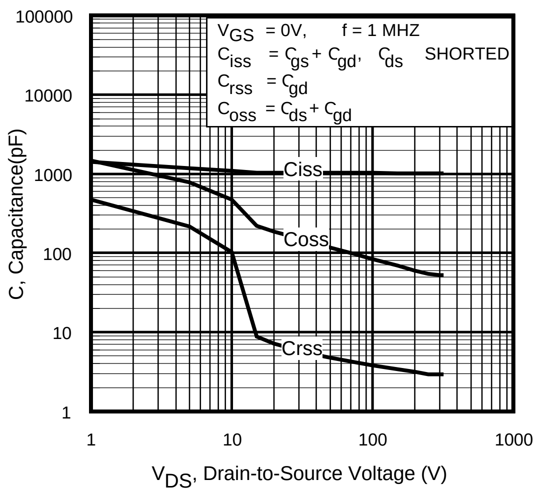


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

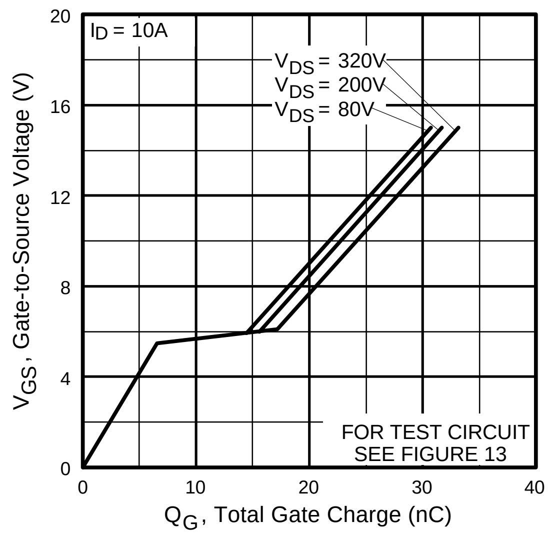


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

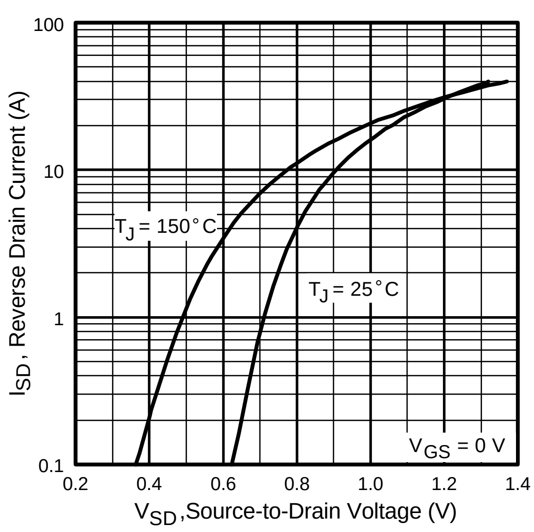


Fig 7. Typical Source-Drain Diode Forward Voltage

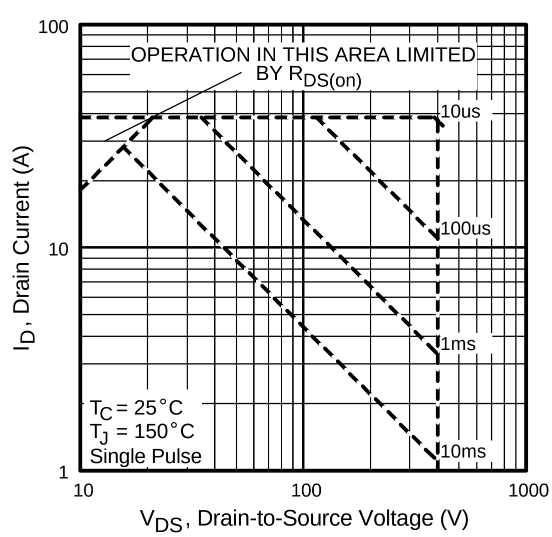


Fig 8. Maximum Safe Operating Area

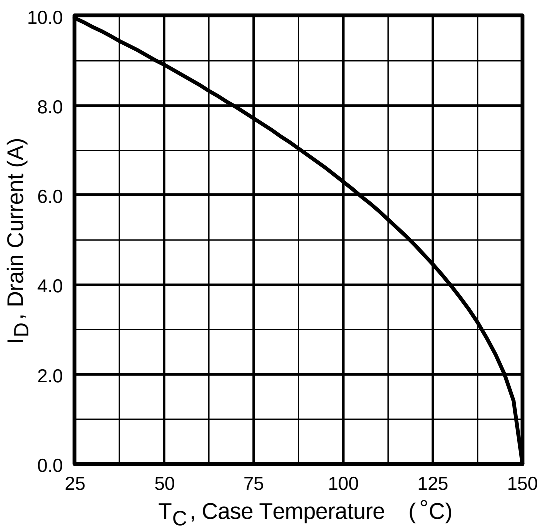


Fig 9. Maximum Drain Current Vs. Case Temperature

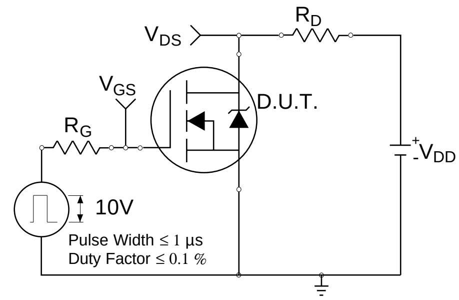


Fig 10a. Switching Time Test Circuit

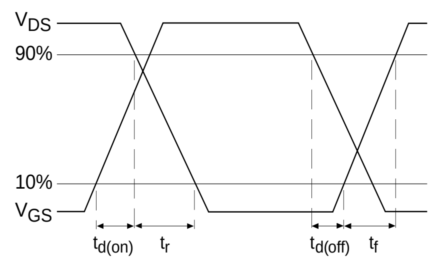


Fig 10b. Switching Time Waveforms

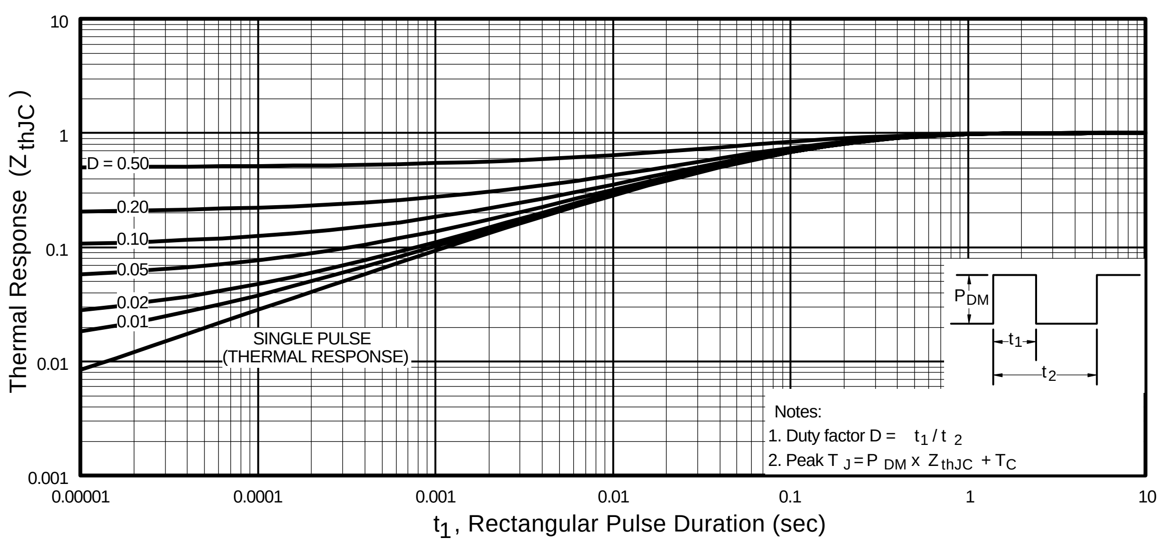


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

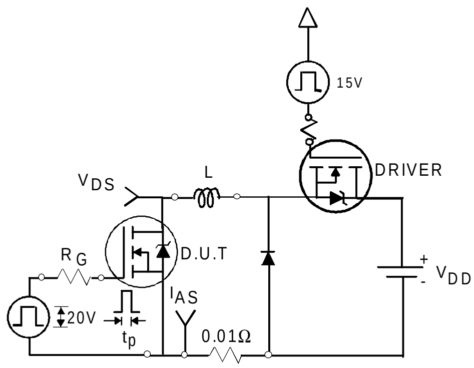


Fig 12a. Unclamped Inductive Test Circuit

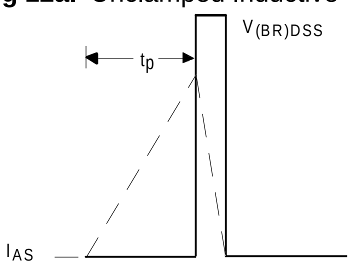


Fig 12b. Unclamped Inductive Waveforms

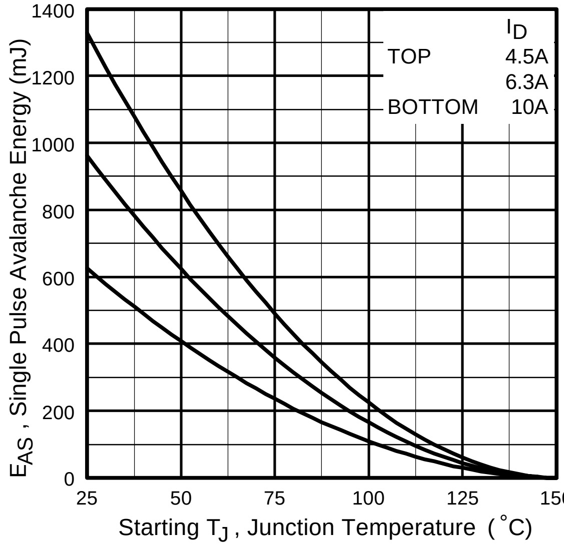


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

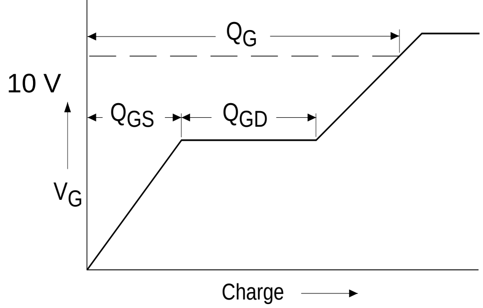


Fig 13a. Basic Gate Charge Waveform

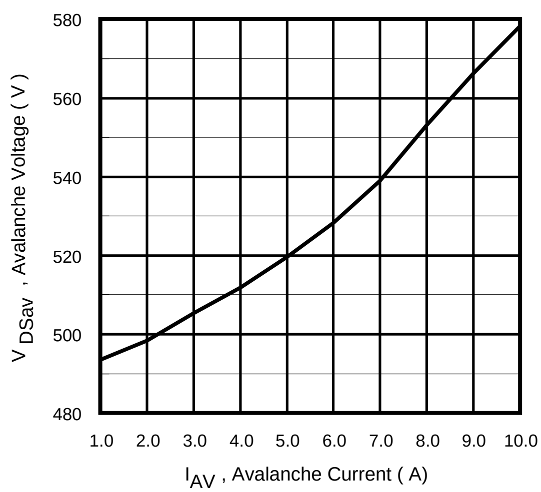


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

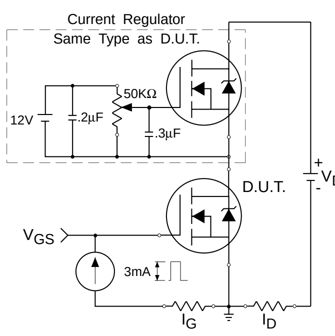
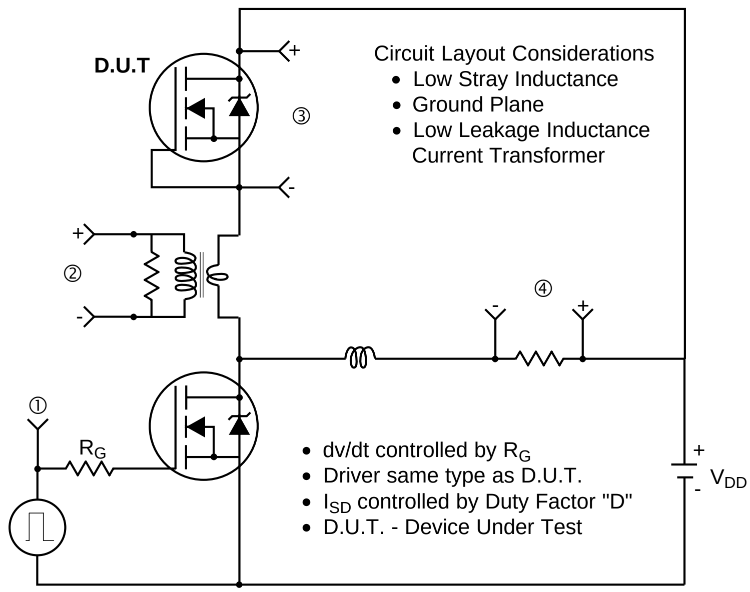
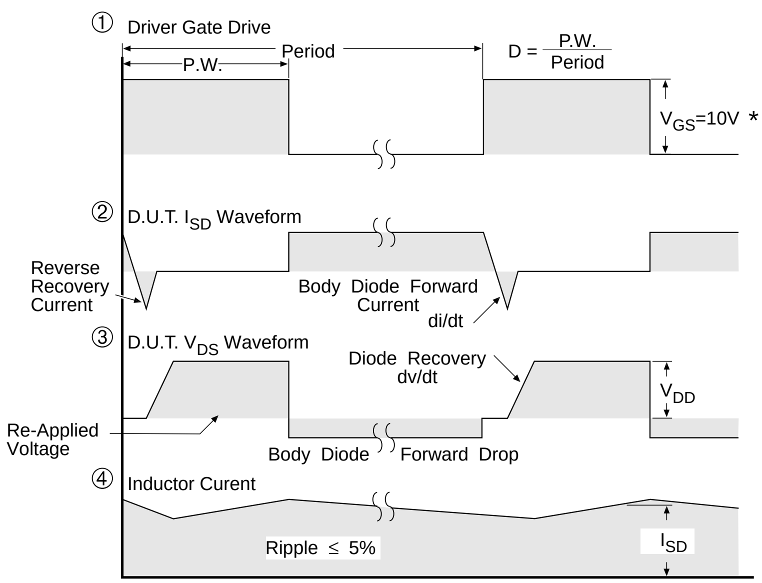


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

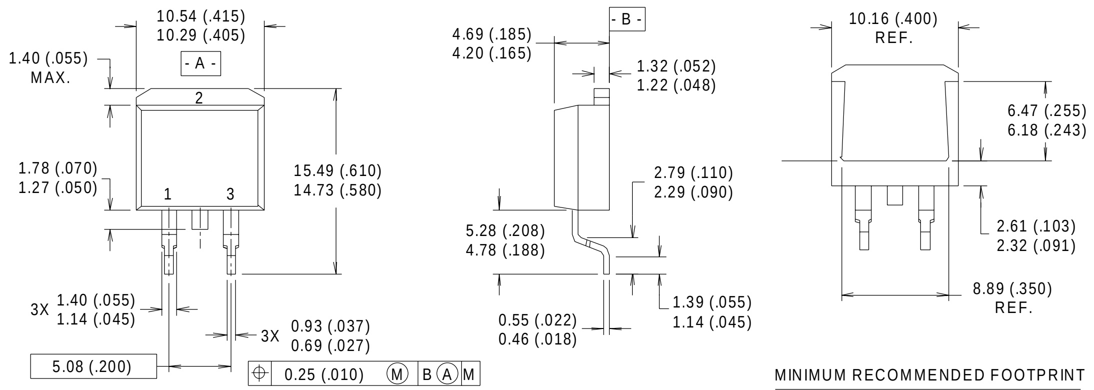




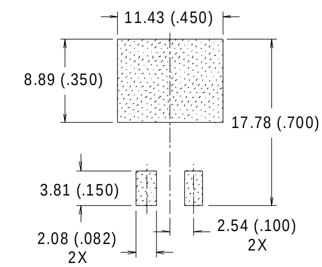
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

D^2Pak Package Outline



MINIMUM RECOMMENDED FOOTPRINT

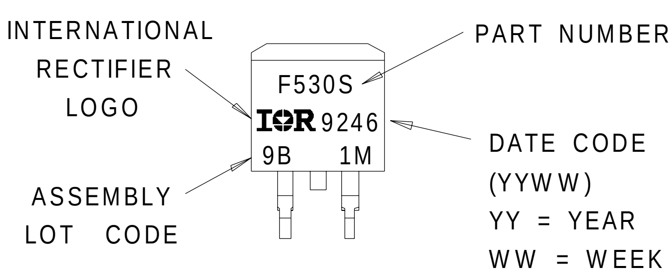


NOTES:
1. DIMENSIONS AFTER SOLDER DIP.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION : INCH.
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

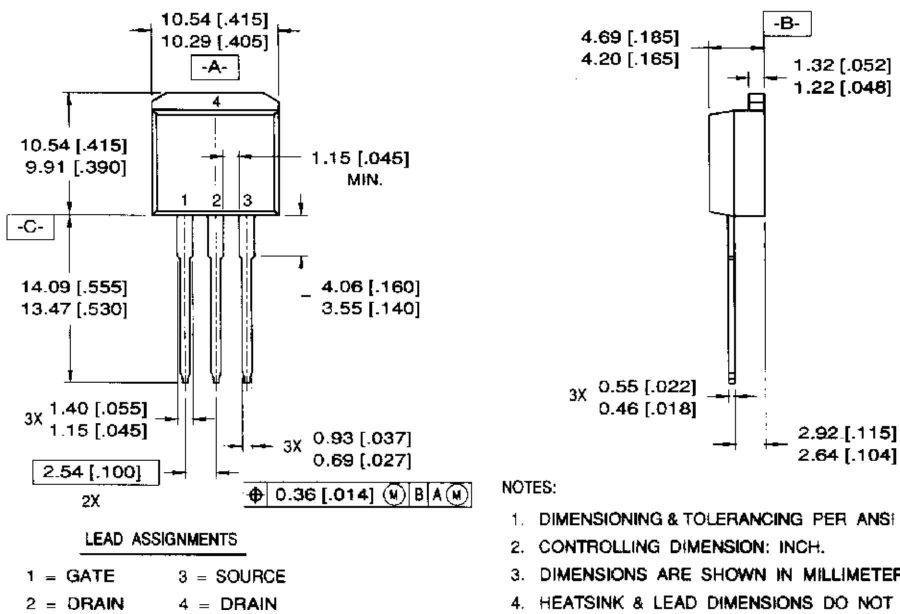
Part Marking Information

D^2Pak



Package Outline

TO-262 Outline



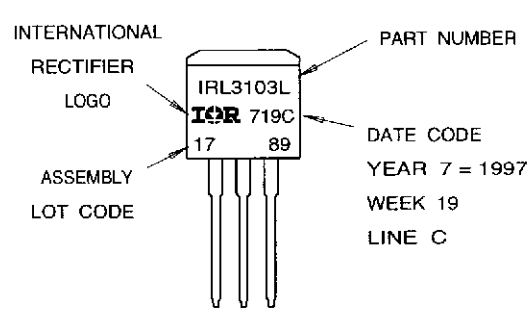
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

TO-262

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



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Tape & Reel Information

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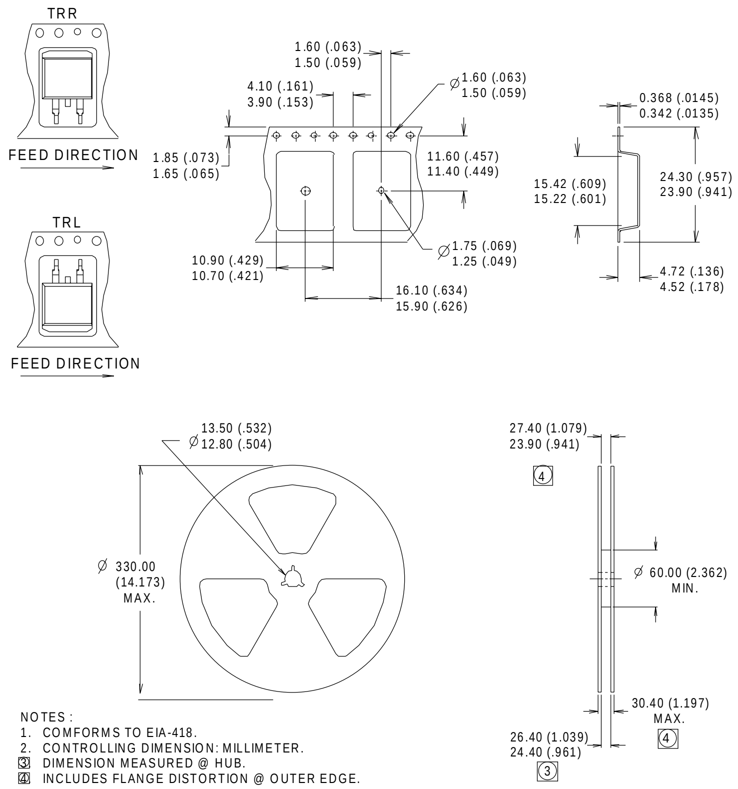

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25°C$, L = 12.6mH $R_G = 25\Omega$, $I_{AS} = 10A$. (See Figure 12)

③ $I_{SD} \leq 10A$, $di/dt \leq 330A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Uses IRF740A data and test conditions

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

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