International IƆR Rectifier

AUTOMOTIVE MOSFET

IRF4104PbF
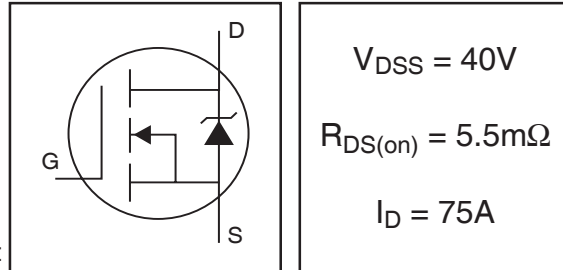IRF4104SPbF
IRF4104LPbF

HEXFET® Power MOSFET

Features
● Advanced Process Technology
● Ultra Low On-Resistance
● 175°C Operating Temperature
● Fast Switching
● Repetitive Avalanche Allowed up to Tjmax
● Lead-Free

Description
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

$V_{DSS} = 40V$

$R_{DS(on)} = 5.5m\Omega$

$I_D = 75A$

| TO-220AB | D²Pak | TO-262 |
| IRF4104 | IRF4104S | IRF4104L |
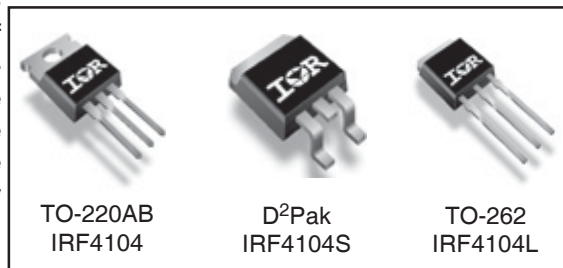
Absolute Maximum Ratings

|	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	120	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	84	A
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package limited)	75	
I_{DM}	Pulsed Drain Current ①	470	
P_D @T_C = 25°C	Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy②	120	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	220	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw ⑦	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.05	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface ⑦	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient ⑦	——	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧	——	40	

6/30/04

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.032	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	4.3	5.5	mΩ	V_{GS} = 10V, I_D = 75A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
gfs	Forward Transconductance	63	——	——	V	V_{DS} = 10V, I_D = 75A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	250		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V
Q_g	Total Gate Charge	——	68	100		I_D = 75A
Q_{gs}	Gate-to-Source Charge	——	21	——	nC	V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	27	——		V_{GS} = 10V ③
$t_{d(on)}$	Turn-On Delay Time	——	16	——		V_{DD} = 20V
t_r	Rise Time	——	130	——		I_D = 75A
$t_{d(off)}$	Turn-Off Delay Time	——	38	——	ns	R_G = 6.8 Ω
t_f	Fall Time	——	77	——		V_{GS} = 10V ③
L_D	Internal Drain Inductance	——	4.5	——		Between lead,
					nH	6mm (0.25in.)
L_S	Internal Source Inductance	——	7.5	——		from package
						and center of die contact
C_{iss}	Input Capacitance	——	3000	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	660	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	380	——	pF	f = 1.0MHz
C_{oss}	Output Capacitance	——	2160	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	560	——		V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	850	——		V_{GS} = 0V, V_{DS} = 0V to 32V ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	75	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	470		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 75A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	23	35	ns	T_J = 25°C, I_F = 75A, V_{DD} = 20V
Q_{rr}	Reverse Recovery Charge	——	6.8	10	nC	di/dt = 100A/μs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

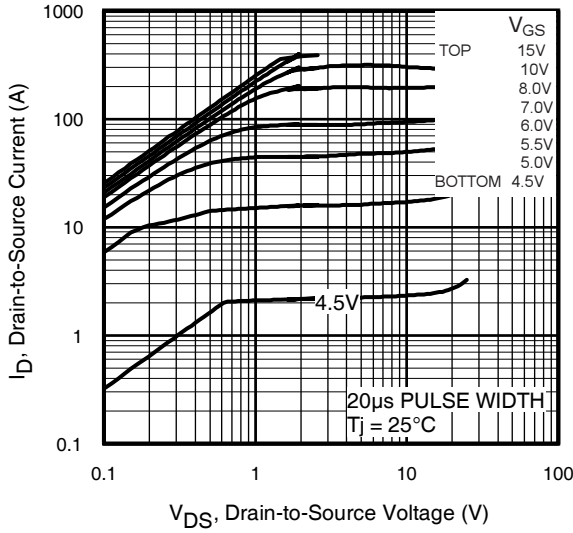# International **I⧸R** Rectifier
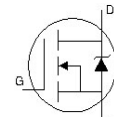
IRF4104S/LPbF

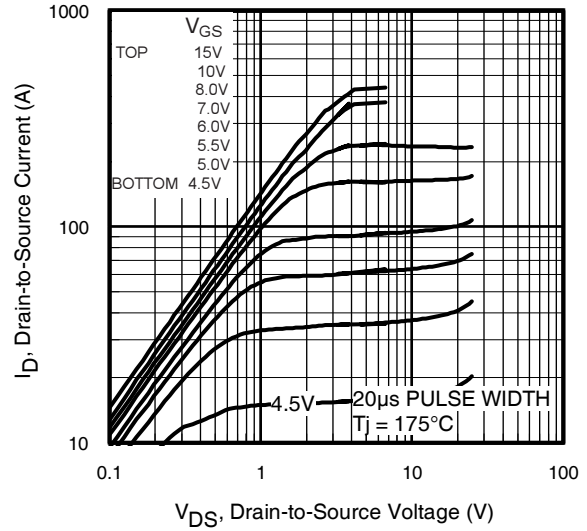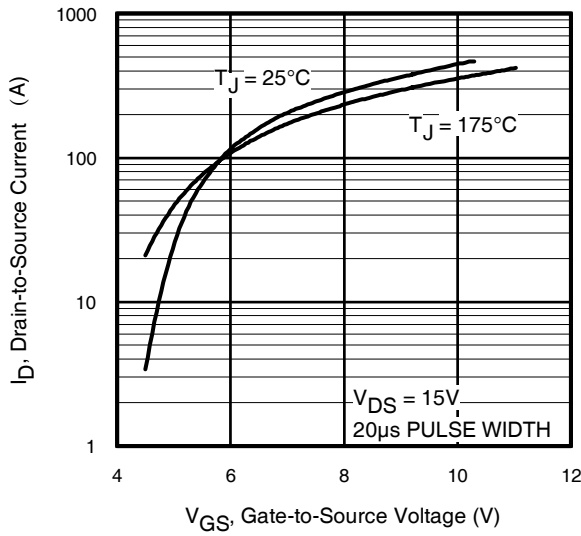Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Typical Forward Transconductance
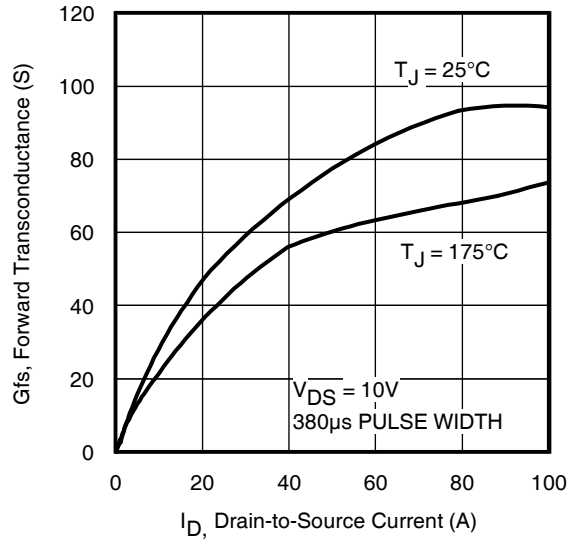Vs. Drain Current

IRF4104S/LPbF
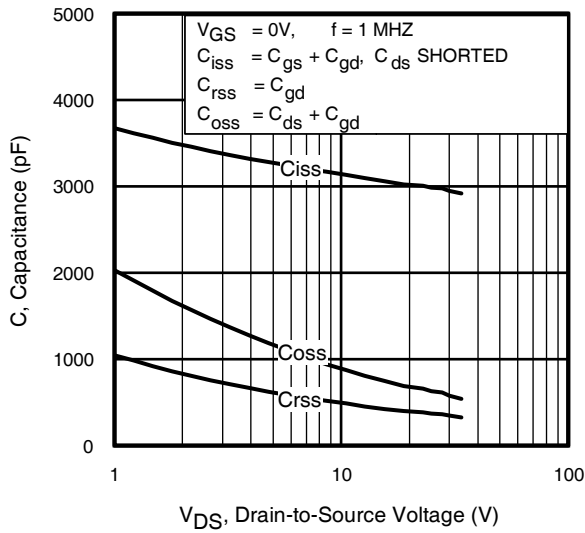

International IOR Rectifier

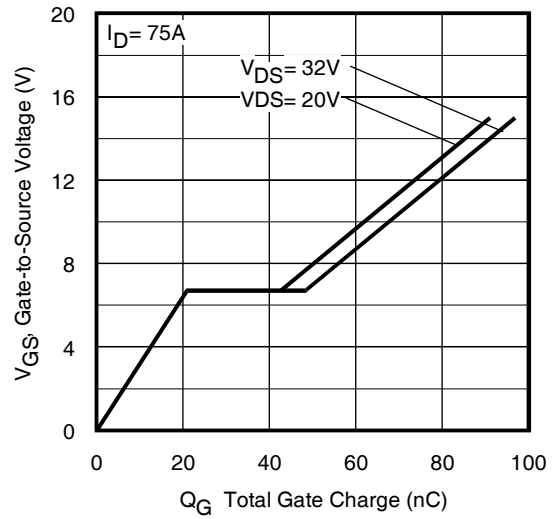Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

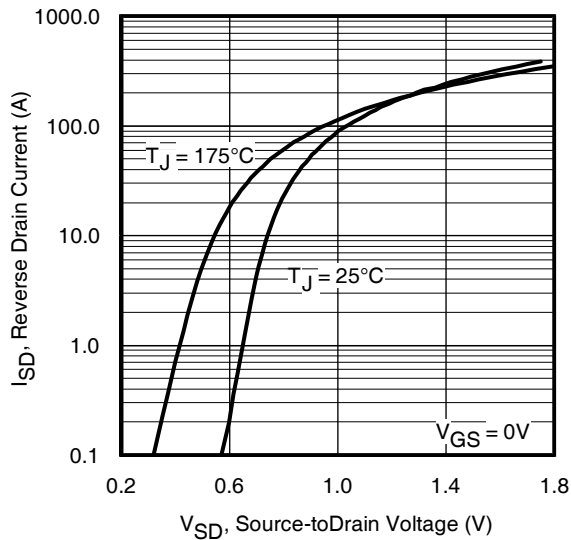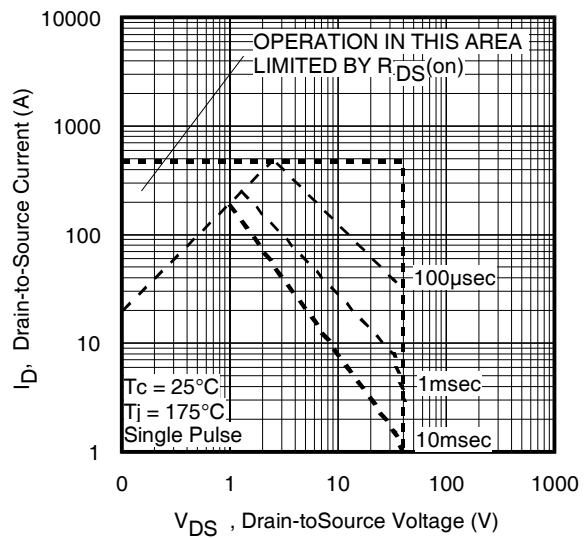Fig 7. Typical Source-Drain Diode Forward Voltage
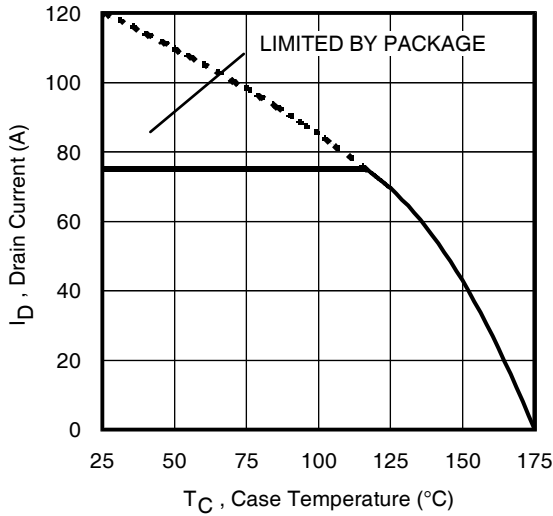
Fig 8. Maximum Safe Operating Area

4

IRF4104S/LPbF

Fig 9. Maximum Drain Current Vs. Case Temperature
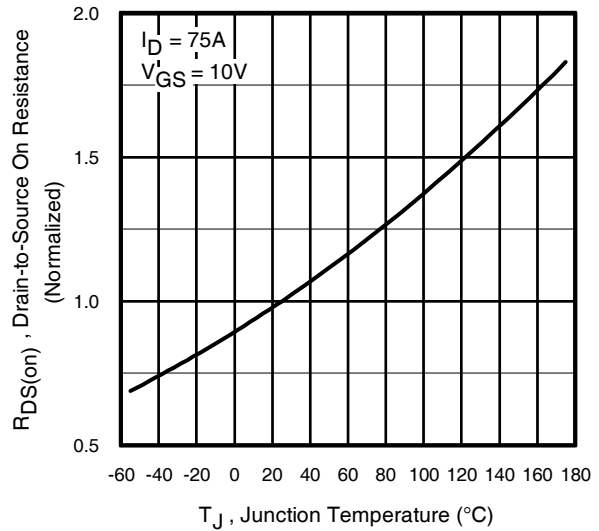
Fig 10. Normalized On-Resistance Vs. Temperature

Ri (°C/W)	τi (sec)
0.371	0.000272
0.337	0.001375
0.337	0.018713

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

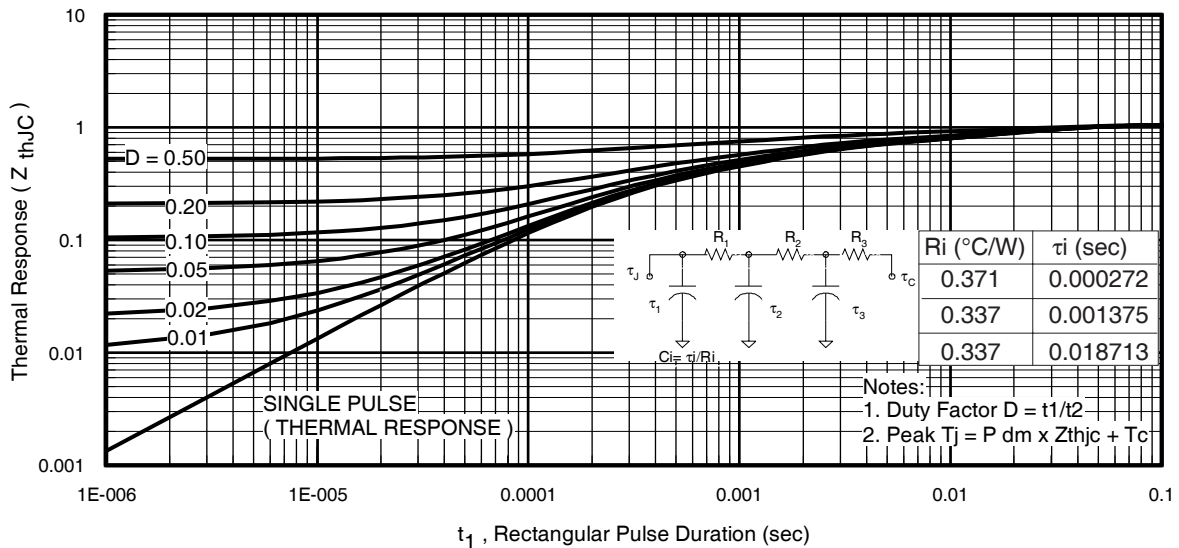**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case
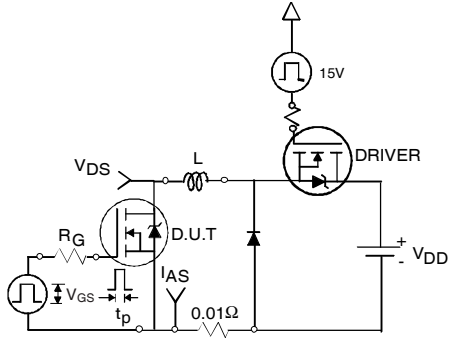
IRF4104S/LPbF

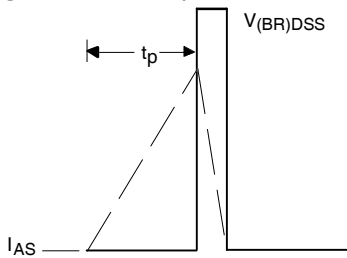**Fig 12a.** Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms
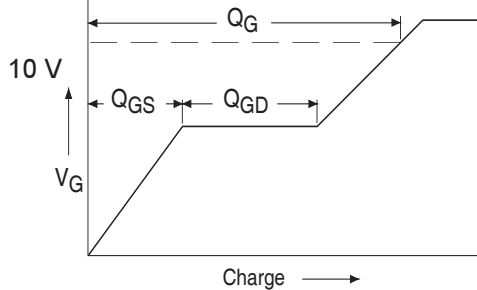

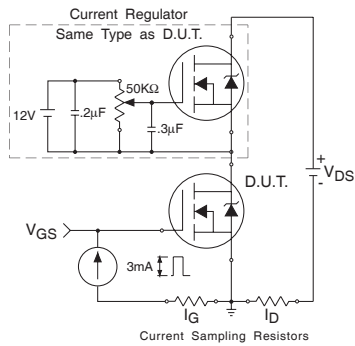**Fig 13a.** Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

6
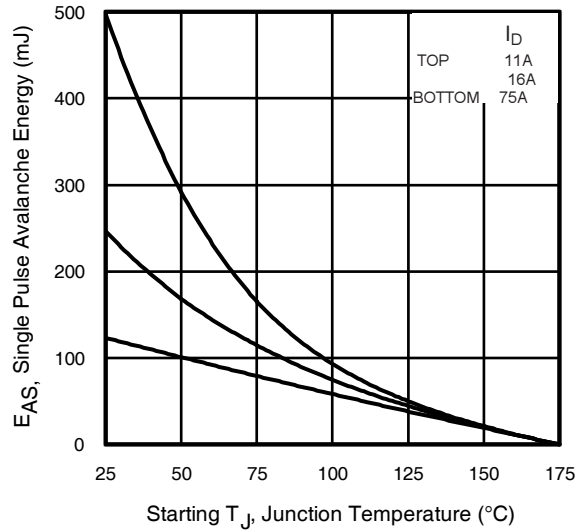
Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

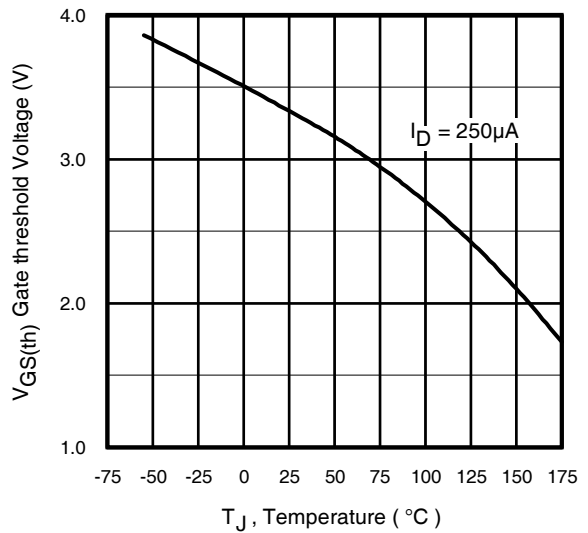**Fig 14.** Threshold Voltage Vs. Temperature

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IRF4104S/LPbF
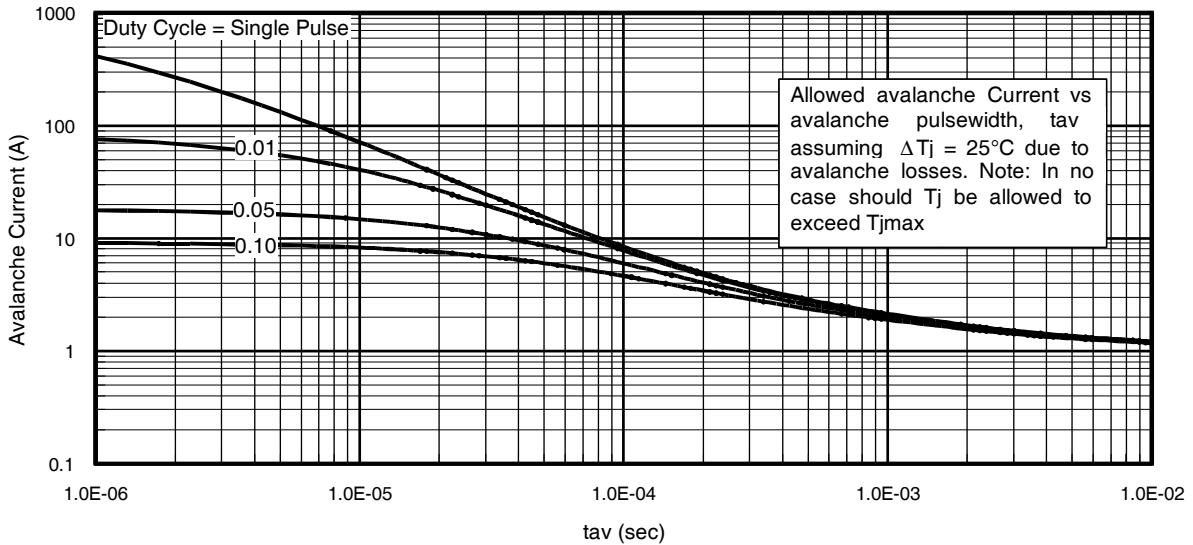
Fig 15. Typical Avalanche Current Vs.Pulsewidth
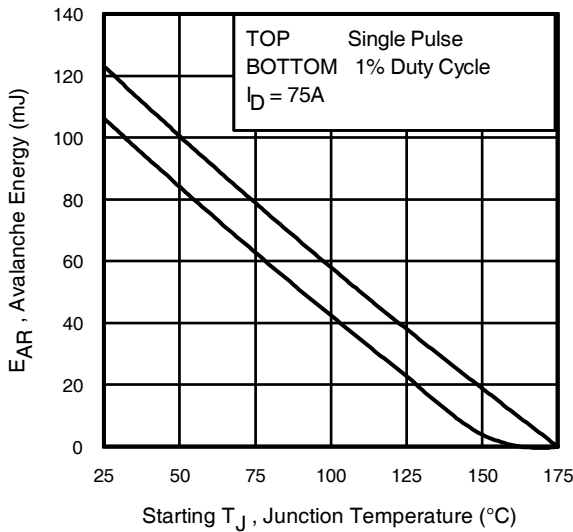
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T/\ Z_{thJC}$$
$$I_{av} = 2\Delta T/\ [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

IRF4104S/LPbF

D.U.T

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance
  Current Transformer

① ② ③ ④

R_G

V_{DD}

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

① Driver Gate Drive

P.W. — Period — $D = \dfrac{P.W.}{Period}$

$V_{GS}=10V$ *

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current
di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

V_{DS} R_D

V_{GS} D.U.T.

R_G $^+$V_{DD}$

10V
Pulse Width ≤ 1 μs
Duty Factor ≤ 0.1 %
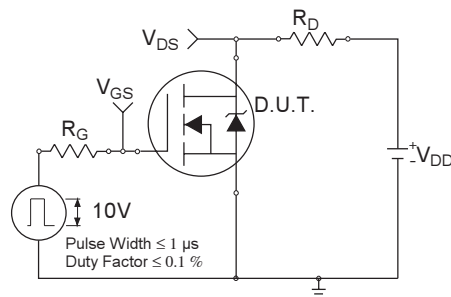
Fig 18a. Switching Time Test Circuit

V_{DS}
90%
10%
V_{GS}

$t_{d(on)}$ t_r $t_{d(off)}$ t_f
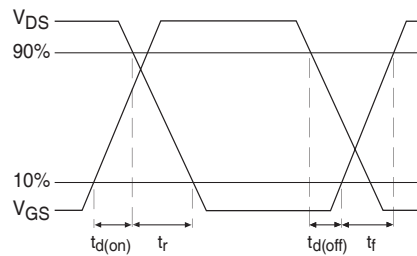
Fig 18b. Switching Time Waveforms

TO-220AB Package Outline
Dimensions are shown in millimeters (inches)

2.87 (.113)
2.62 (.103)

10.54 (.415)
10.29 (.405)

3.78 (.149)
3.54 (.139)

- A -

6.47 (.255)
6.10 (.240)

15.24 (.600)
14.84 (.584)

1.15 (.045)
MIN

14.09 (.555)
13.47 (.530)

4.06 (.160)
3.55 (.140)

3X 0.93 (.037)
0.69 (.027)

3X 1.40 (.055)
1.15 (.045)

| ⊕ | 0.36 (.014) | Ⓜ | B | A | Ⓜ |

2.54 (.100)
2X

- B -

4.69 (.185)
4.20 (.165)

1.32 (.052)
1.22 (.048)
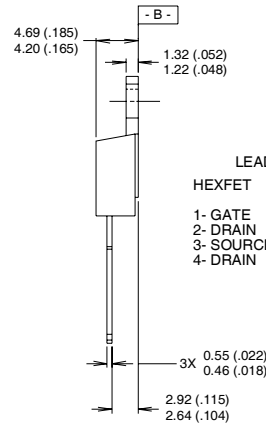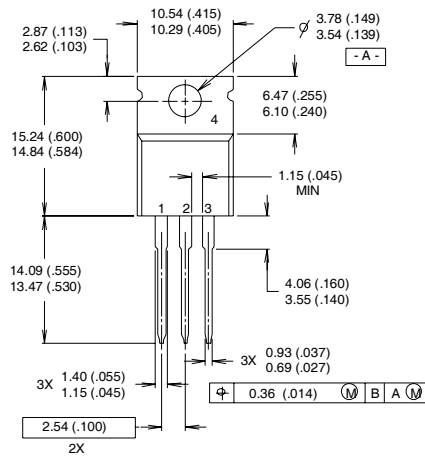
LEAD ASSIGNMENTS

HEXFET   IGBTs, CoPACK

1- GATE   1- GATE
2- DRAIN   2- COLLECTOR
3- SOURCE   3- EMITTER
4- DRAIN   4- COLLECTOR

3X 0.55 (.022)
0.46 (.018)

2.92 (.115)
2.64 (.104)

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
          LOT CODE 1789
          ASSEMBLED ON WW 19, 1997
          IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line
position indicates "Lead-Free"

INTERNATIONAL
RECTIFIER
LOGO

IRF1010

IQR 719C

17   89

ASSEMBLY
LOT CODE

PART NUMBER

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C
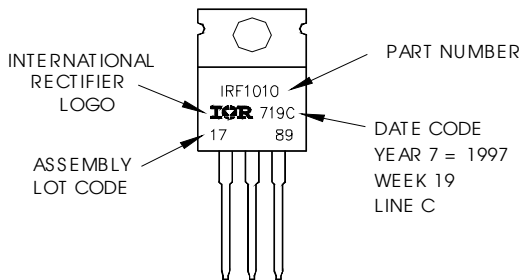
D²Pak Package Outline

Dimensions are shown in millimeters (inches)

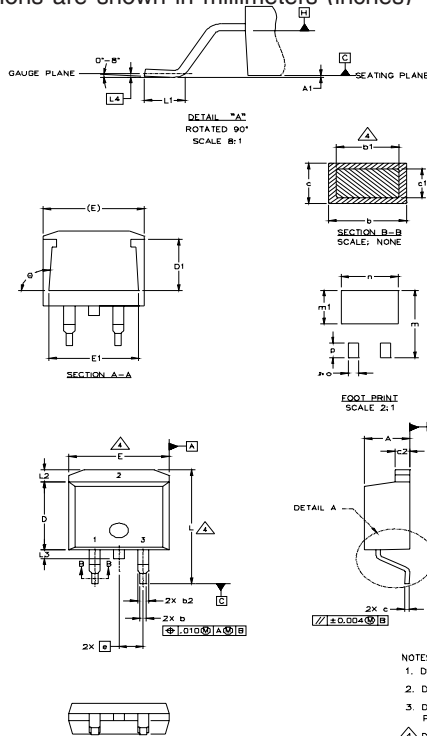| SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

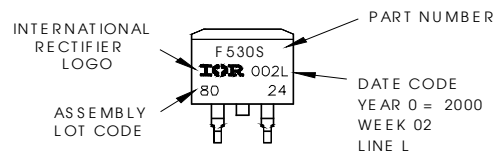| HEXFET	IGBTs, CoPACK	DIODES
1.— GATE	1.— GATE	1.— ANODE *
2.— DRAIN	2.— COLLECTOR	2.— CATHODE
3.— SOURCE	3.— EMITTER	3.— ANODE

* PART DEPENDENT.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE

PART NUMBER

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

OR

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE

PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 0 = 2000
WEEK 02
A = ASSEMBLY SITE CODE

TO-262 Package Outline
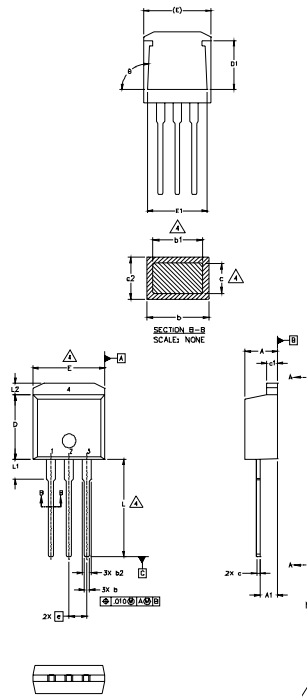
S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

1.— GATE
2.— DRAIN
3.— SOURCE
4.— DRAIN

IGBT

1- GATE
2- COLLECTOR
3- EMITTER

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
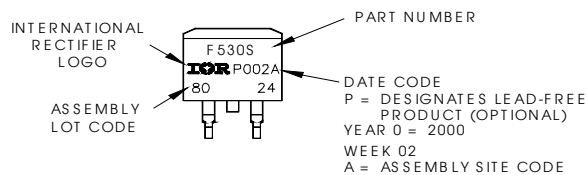5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

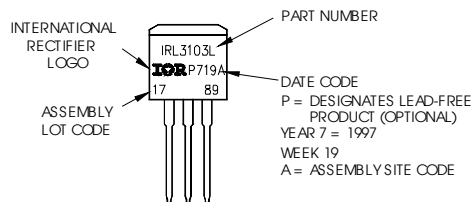Note: "P" in assembly line
position indicates "Lead-Free"

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE

PART NUMBER

IRL3103L
IΩR 719C
17   89

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

OR

INTERNATIONAL
RECTIFIER
LOGO

ASSEMBLY
LOT CODE

PART NUMBER

IRL3103L
IΩR P719A
17   89

DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 7 = 1997
WEEK 19
A = ASSEMBLY SITE CODE

D²Pak Tape & Reel Infomation

TRR

FEED DIRECTION

TRL

FEED DIRECTION

1.60 (.063)
1.50 (.059)

4.10 (.161)
3.90 (.153)

1.85 (.073)
1.65 (.065)

ø 1.60 (.063)
1.50 (.059)

11.60 (.457)
11.40 (.449)

10.90 (.429)
10.70 (.421)

ø 1.75 (.069)
1.25 (.049)

16.10 (.634)
15.90 (.626)

0.368 (.0145)
0.342 (.0135)

15.42 (.609)
15.22 (.601)

24.30 (.957)
23.90 (.941)

4.72 (.136)
4.52 (.178)

13.50 (.532)
ø 12.80 (.504)

ø 330.00
(14.173)
MAX.

27.40 (1.079)
23.90 (.941)
[4]

ø 60.00 (2.362)
MIN.

30.40 (1.197)
MAX.
[4]

26.40 (1.039)
24.40 (.961)
[3]

NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
[3] DIMENSION MEASURED @ HUB.
[4] INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting $T_J = 25°C$, L = 0.04mH $R_G = 25\Omega$, $I_{AS} = 75A$, $V_{GS} =10V$. Part not recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ This is only applied to TO-220AB pakcage.

⑧ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

TO-220AB package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101]market.
Qualification Standards can be found on IR's Web site.

International
IƏR Rectifier

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/