

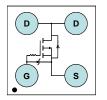
Features

- Ultra Low Qg & Qgd
- Small Footprint
- Low Profile 0.65mm height
- Pb Free
- Gate ESD Protection 3kV
- RoHS Compliant
- Halogen Free



CSP 1.0 x 1.0 mm Wafer

Level Package



Тор

Product Summary

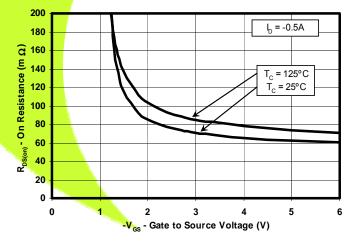
V _{DS}	-12	V	
Q_g	1.8	nC	
Q_{gd}	0.4	nC	
$R_{\text{DS(on)}}$	V _{GS} = -1.5V	110	mΩ
	V _{GS} =-2.5V	77	mΩ
	V _{GS} =-4.5V	mΩ	
V_{th}	-0.6	V	

Maximum Values (T_A =25°C unless otherwise stated)

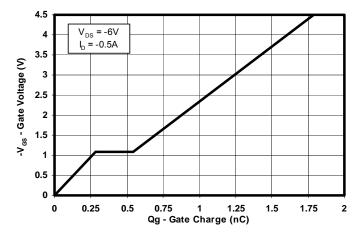
Symbol	Parameter	Value	Units
V _{DS}	Drain to Source Voltage	-12	V
V _{GS}	Gate to Source Voltage	-5	V
I _D	Continuous Drain Current, T _A = 25°C¹	-1.1	А
I _{DM}	Pulsed Drain Current, T _A = 25°C ^{1,2}	-4.4	А
P _D	Power Dissipation ¹	1.0	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

- 1. $R_{thJA} = 100^{\circ} C/W$ on 1 in² Cu (2 oz.) on 0.060" thick FR4 PCB
- 2. Pulse width ≤300 µs, duty cycle ≤ 2%

R_{DS(ON)} vs. V_{GS}



Gate Charge



Ordering Information

Туре	Package	Package Media	Qty	Ship
CSD23201W10	1.0 X 1.0 Wafer Level Package	7 inch reel	3000	Tape and Reel



Electrical Characteristics (T_A = 25°C unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Static Ch	aracteristics		'			
BV _{DSS}	Drain to Source Voltage	V _G s = 0V, I _D = -250μA	-12	—	_	V
IDSS	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = -9.6V	_	_	-1	μA
Igss	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = -5V	—	_	-100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.6	-1.0	V
		V _{GS} = -1.5V, I _D = -0.5A	_	110	138	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = -2.5V, I _D = -0.5A	_	77	96	mΩ
		V _{GS} = -4.5V, I _D = -0.5A	_	66	82	mΩ
G fs	Transconductance	$V_{DS} = -6.0V, I_D = -0.5A$	_	9.0	_	S
Dynamic	Characteristics					
Ciss	Input Capacitance	V 9VV 99V	_	250	325	pF
Coss	Output Capacitance	$V_{GS} = 0V, V_{DS} = -6.0V$ f = 1MHz	_	125	155	pF
Crss	Reverse Transfer Capacitance	T = TIVITZ	_	32	42	pF
Qg	Gate Charge Total (-4.5V)		_	1.8	2.4	nC
Q_{gd}	Gate Charge Gate to Drain	7	_	0.26	_	nC
Q _{gs}	Gate Charge Gate to Source	$V_{DS} = -6.0V, I_D = -0.5A$	_	0.28	_	nC
Q _{g(th)}	Gate Charge at Vth		_	0.11	_	nC
Qoss	Output Charge	V _{DS} = -6.0V, V _{GS} = 0V	_	1.7	_	nC
t _{d(on)}	Turn On Delay Time		_	24	_	ns
t r	Rise Time	$V_{DS} = -6.0V$	_	19	_	ns
t _{d(off)}	Turn Off Delay Time	$V_{GS} = -2.5 V I_{D} = -0.5 A$ $R_{G} = 20 \Omega$	_	68	_	ns
t _f	Fall Time	- 1\G - 20\s2	_	29	_	ns
Diode Ch	naracteristics		•	•	-	-
V _{SD}	Diode Forward Voltage	I _S = -0.5A, V _{GS} = 0V	_	-0.77	-1.0	V
Q _{rr}	Reverse Recovery Charge	V _{dd} =-4.0V, I _F = -0.5A, di/dt = 100A/μs	_	2.0	_	nC
t _{rr}	Reverse Recovery Time	V_{dd} =-4.0V, I_F = -0.5A, di/dt = 100A/ μ s	_	9.5	_	ns



Thermal Characteristics (T_A = 25°C unless otherwise stated)

Symbol	Parameter	Min	Тур	Max	Units
Thermal Characteristics					
R _{θJA}	Thermal Resistance Junction to Ambient (Minimum Cu area)	_	_	245	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient (1 in² Cu area)		_	125	°C/W



Max R_{θ}ja =125 °C/W when mounted on 1in² of 2 oz. Cu.



Max Reja =245 $^{\circ}$ C/W when mounted on min pad area of 2 oz. Cu.

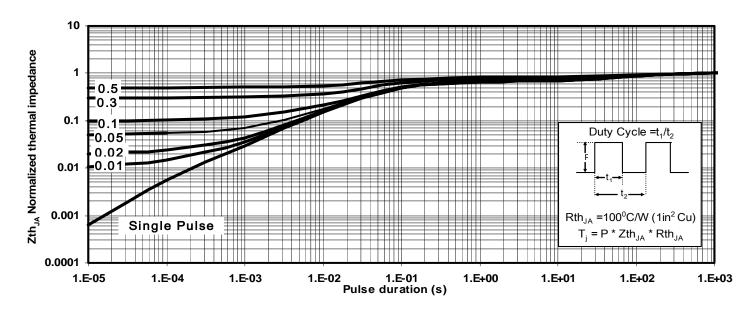
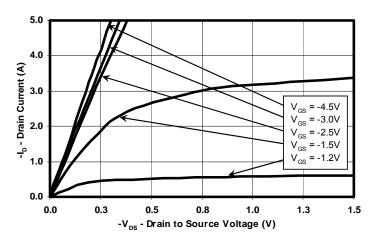


Figure 1: Transient Thermal Impedance



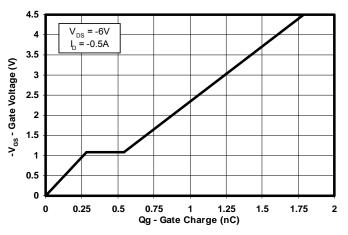
Typical MOSFET Characteristics (T_A = 25°C unless otherwise stated)



5.0 4.5 4.0 3.5 3.0 2.5 T_J = -55°C T_J = 25°C T_J = 25°C T_J = 125°C T_J = 125°C 1.0 0.5 0.75 1 1.25 1.75 2 2 1.75 1.75 1.75 1.75 1.75 2 2 1.75

Figure 2: Saturation Characteristics

Figure 3: Transfer Characteristics



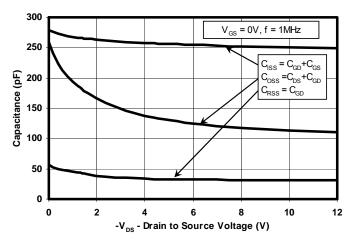
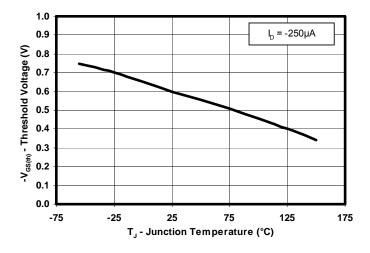


Figure 4: Gate Charge

Figure 5: Capacitance



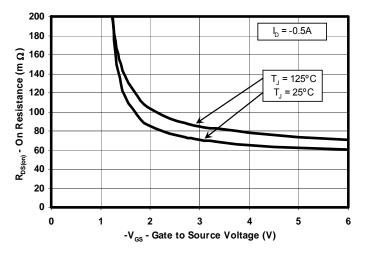
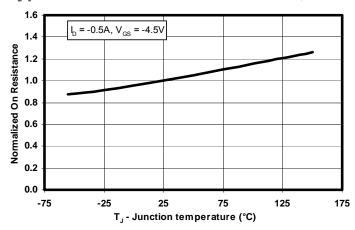


Figure 6: Threshold Voltage vs. Temperature

Figure 7: On Resistance vs. Gate Voltage



Typical MOSFET Characteristics (T_A = 25°C unless otherwise stated)



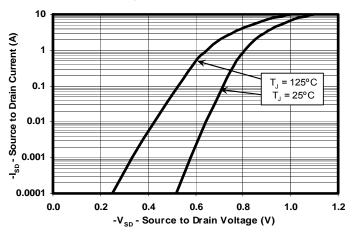


Figure 8: On Resistance vs. Temperature

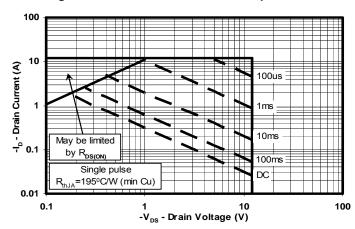


Figure 10: Maximum Safe Operating Area

Figure 9: Typical Diode Forward Voltage

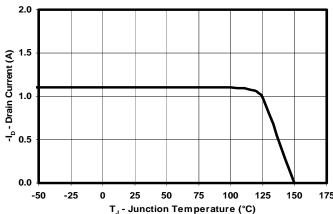
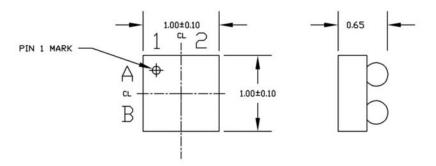
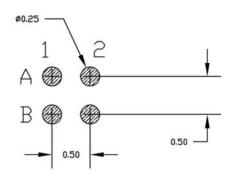


Figure 11: Maximum Drain Current vs. Temperature

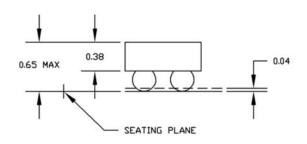


CSD23201W10 Package Dimensions

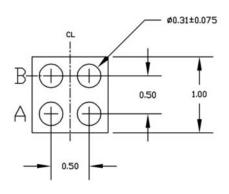




LAND PATTERN RECOMMENDATION



SOLDER BALL



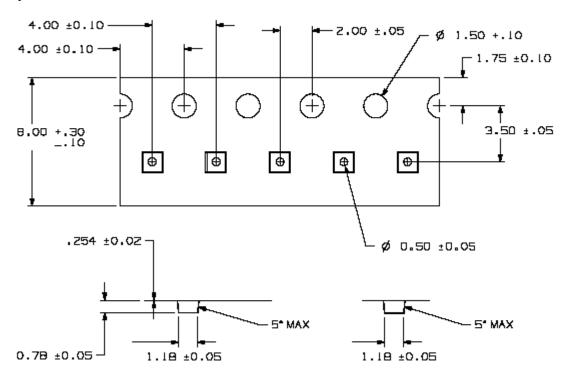
NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS B) TERMINAL CONFIGURATION TABLE.

POSITION	DESIGNATION
A2, B2	DRAIN
A1	GATE
B1	SOURCE



Tape and Reel Information



Package Marking Information

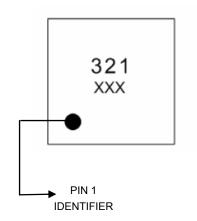
Location:

1st Line

Product Code = 321 (Fixed Text)

2nd Line

XXX = Last 3 digits of wafer lot number





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PACKAGE OPTION ADDENDUM

www.ti.com 11-May-2009

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins Pa	ackage Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CSD23201W10	ACTIVE	DSBGA	YZB	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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