CPC5602

N Channel Depletion Mode FET

Parameter	Rating	Units
Drain-to-Source Voltage (V_{DS})	350	V
Max On-Resistance ($R_{on\text{-}max}$)	14	Ω
Max Power	2.5	W

Features

- 350V Drain-to-Source Voltage
- Low On-resistance: 8 Ohms (Typical)
- High input impedance
- Low input and output leakage
- Small package size SOT-223
- PC Card (PCMCIA) Compatible
- PCB Space and Cost Savings

Applications

- Support Component for LITELINK™ Data Access Arrangement (DAA)
- Telecommunications

Description

The CPC5602 is an “N” channel depletion mode Field Effect Transistor (FET) that utilizes Clare’s proprietary third generation vertical DMOS process. The third generation process realizes world class, high voltage MOSFET performance in an economical silicon gate process. The vertical DMOS process yields a highly reliable device, particularly in difficult application environments such as telecommunications.

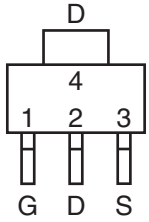
One of the primary applications for the CPC5602 is as a linear regulator/hook switch for the LITELINK family of Data Access Arrangements (DAA) Devices CPC5610A, CPC5611A, CPC5620A, CPC5621A, and CPC5622A.

The CPC5602 has a typical on-resistance of 8Ω, a drain-to-source voltage of 350V, and is available in an SOT-223 package. As with all MOS devices, the FET structure prevents thermal runaway and thermal-induced secondary breakdown.

Ordering Information

Part Number	Description
CPC5602C	N-Channel Depletion Mode FET, SOT-223 Package (80/tube)
CPC5602CTR	N-Channel Depletion Mode FET, SOT-223 Package Tape and Reel (1000/reel)

Package Pinout



Pin Number	Name
1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

Absolute Maximum Ratings

Parameter	Min	Max	Units
Drain-to-Source Voltage (V_{DS})	350	-	V
Total Package Dissipation	-	2.5	W
Operational Temperature	-40	+85	°C
Storage Temperature	-40	+125	°C

Electrical absolute maximum ratings are at 25°C.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Electrical Characteristics (@25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gate-to-Source Off Voltage	$V_{GS(off)}$	I_D= 2µA, V_{DS}=10V, V_{DS}=100V	-2	-	-3.6	V
Drain-to-Source Leakage Current	$I_{DS(off)}$	V_{GS}= -5V, V_{DS}=190V	-	-	20	nA
		V_{GS}= -5V, V_{DS}=350V	-	-	1	µA
Drain Current	I_D	V_{GS}= -2.7V, V_{DS}=5V, V_{DS}=50V	-	-	5	mA
		V_{GS}= -0.57V, V_{DS}=5V	130	-	-	mA
On Resistance	$R_{DS(on)}$	V_{GS}= -0.35V, I_{DS}=50mA	-	8	14	Ω
Gate Leakage Current	I_{GSS}	V_{GS}=10V, V_{GS}=-10V	-	-	0.1	µA
Gate Capacitance	C_{ISS}	V_{DS}= V_{GS}=0V	-	-	300	pF

Thermal Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal Resistance	$R_{\theta JC}$	-	-	-	14	°C/W

MANUFACTURING INFORMATION

Soldering

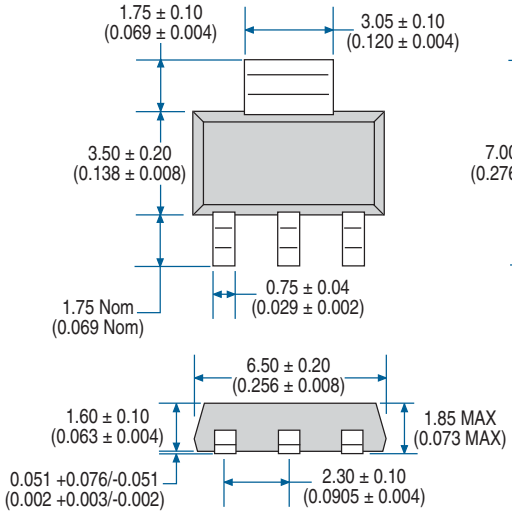
For proper assembly, the component must be processed in accordance with the current revision of IPC/JEDEC standard J-STD-020. Failure to follow the recommended guidelines may cause permanent damage to the device resulting in impaired performance and/or a reduced lifetime expectancy.

Washing

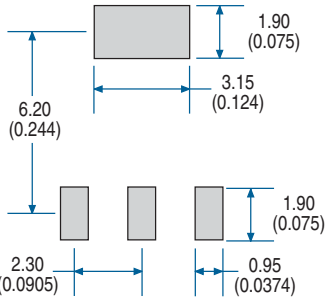
Clare does not recommend ultrasonic cleaning or the use of chlorinated solvents.

MECHANICAL DIMENSIONS

SOT-223 Package

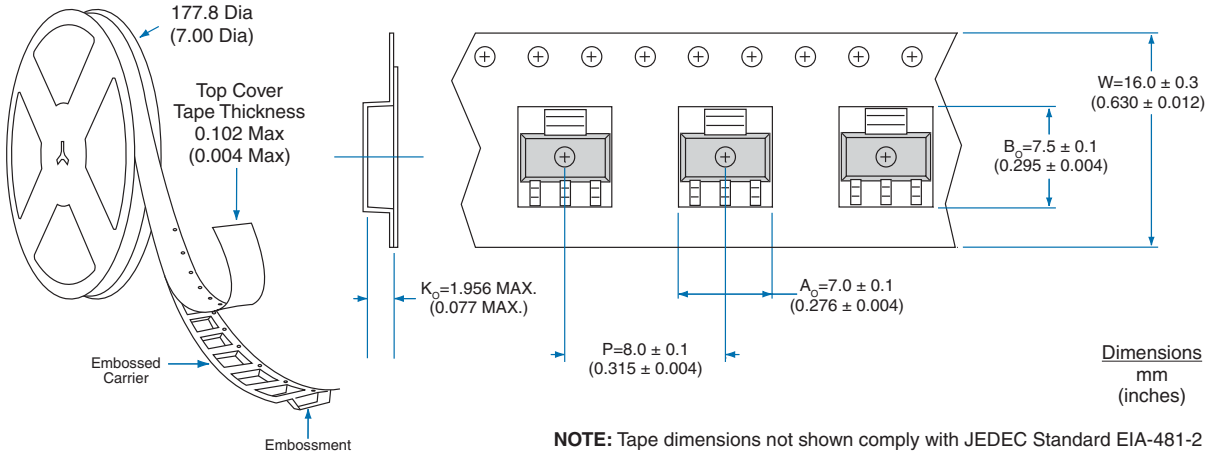


Recommended PCB Land Pattern



Dimensions
mm
(inches)

7" Tape and Reel Packaging for the SOT-223 Package



Dimensions
mm
(inches)

NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

For additional information please visit our website at: www.clare.com

Specification: DS-CPC5602-R05

9/30/08