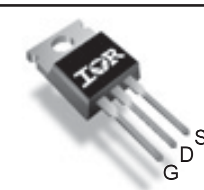
International
IOR Rectifier

SMPS MOSFET

IRFB16N50KPbF

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ typ.	I_D
500V	**285mΩ**	**17A**



TO-220AB

Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits
- Lead-Free

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low $R_{DS(on)}$

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, VGS @ 10V	17	A
I_D @ T_C = 100°C	Continuous Drain Current, VGS @ 10V	11	
I_{DM}	Pulsed Drain Current ①	68	
P_D @T_C = 25°C	Power Dissipation	280	W
	Linear Derating Factor	2.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	11	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	–––	310	mJ
I_{AR}	Avalanche Current ①	–––	17	A
E_{AR}	Repetitive Avalanche Energy ①	–––	28	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	0.44	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient	–––	62	

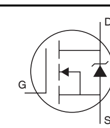
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.58	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	285	350	mΩ	V_{GS} = 10V, I_D = 10A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	V_{DS} = 500V, V_{GS} = 0V
		—	—	250		V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	5.7	—	—	S	V_{DS} = 50V, I_D = 10A
Q_g	Total Gate Charge	—	60	89	nC	I_D = 17A
Q_{gs}	Gate-to-Source Charge	—	18	27		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	28	43		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	V_{DD} = 250V
t_r	Rise Time	—	77	—		I_D = 17A
$t_{d(off)}$	Turn-Off Delay Time	—	38	—		R_G = 8.8Ω
t_f	Fall Time	—	30	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	2210	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	240	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	26	—		ƒ = 1.0MHz
C_{oss}	Output Capacitance	—	2620	—		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	—	63	—		V_{GS} = 0V, V_{DS} = 400V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	120	—		V_{GS} = 0V, V_{DS} = 0V to 400V ③

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the 
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	68	A	integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J = 25°C, I_S = 17A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	490	730	ns	T_J = 25°C, I_F = 17A
Q_{rr}	Reverse Recovery Charge	—	5710	8560	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 2.2mH, R_G = 25Ω, I_{AS} = 17A.

③ $I_{SD} \leq$ 17A, di/dt ≤ 500A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C.

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

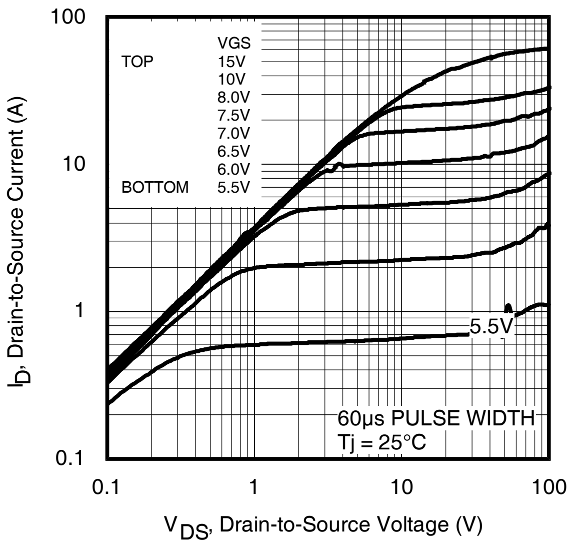


Fig 1. Typical Output Characteristics

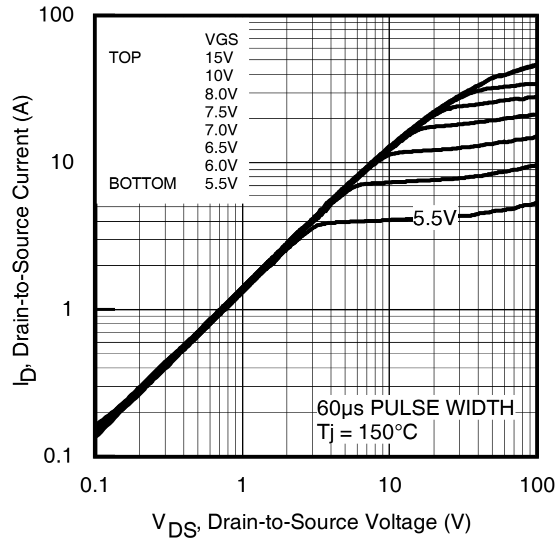


Fig 2. Typical Output Characteristics

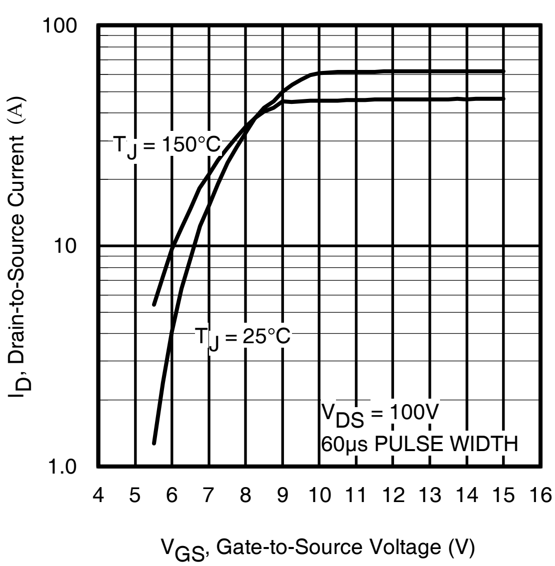


Fig 3. Typical Transfer Characteristics

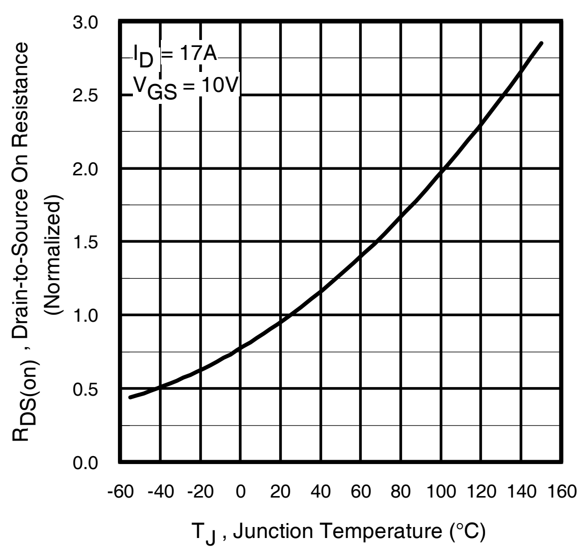


Fig 4. Normalized On-Resistance vs. Temperature

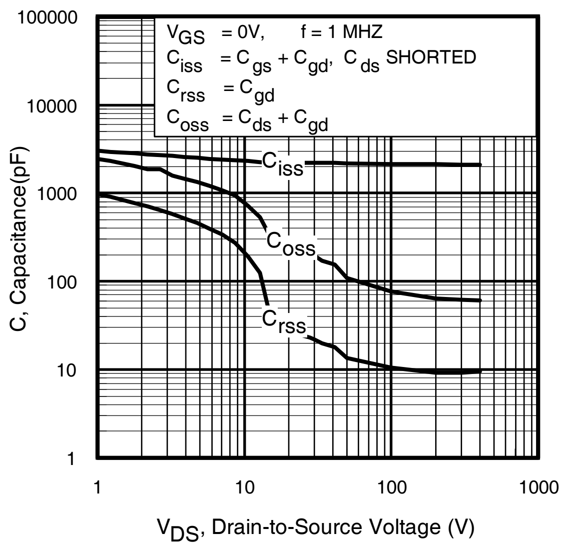


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

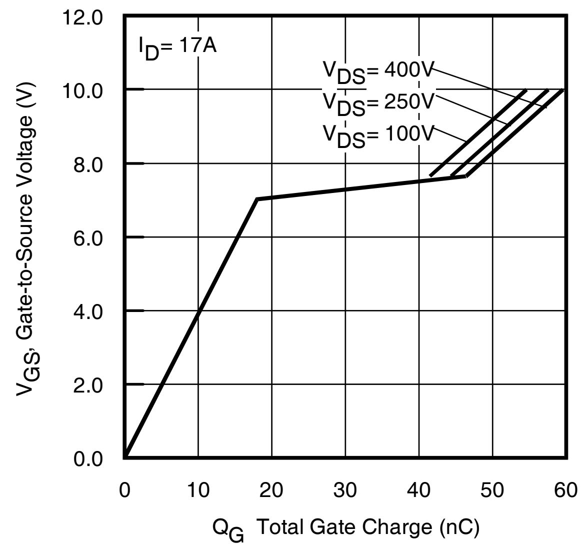


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

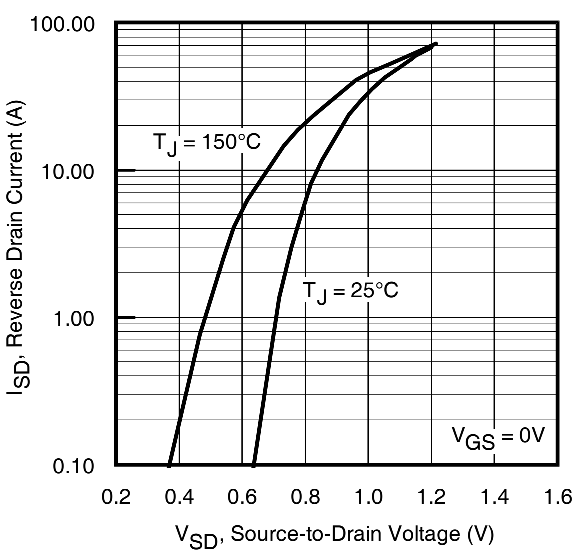


Fig 7. Typical Source-Drain Diode Forward Voltage

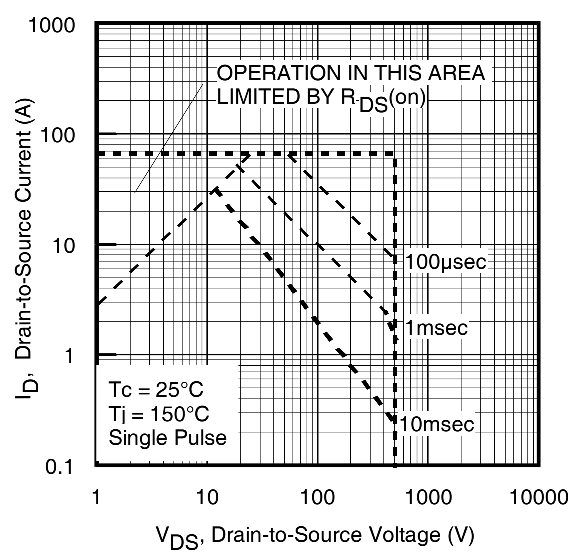


Fig 8. Maximum Safe Operating Area

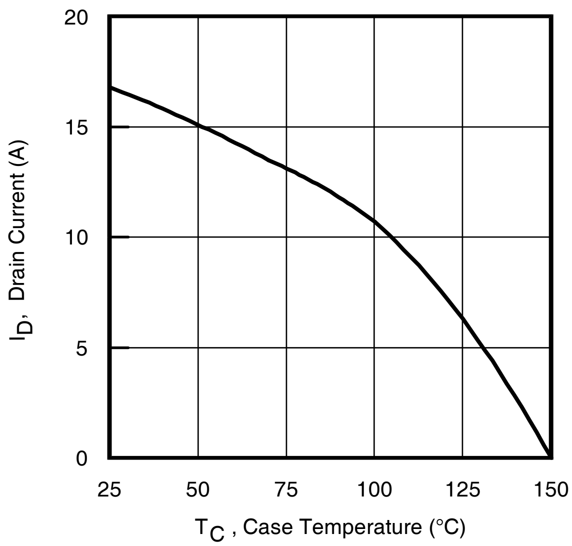


Fig 9. Maximum Drain Current vs. Case Temperature

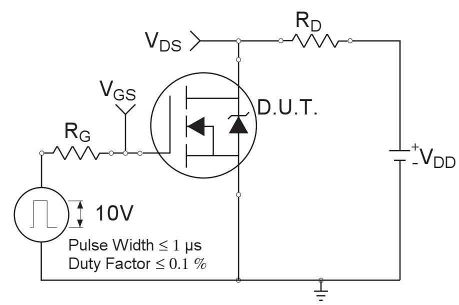


Fig 10a. Switching Time Test Circuit

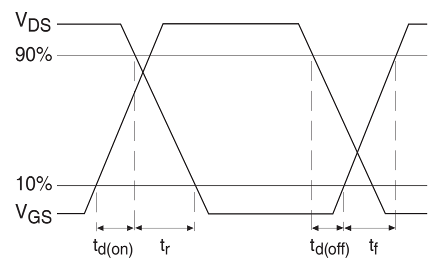


Fig 10b. Switching Time Waveforms

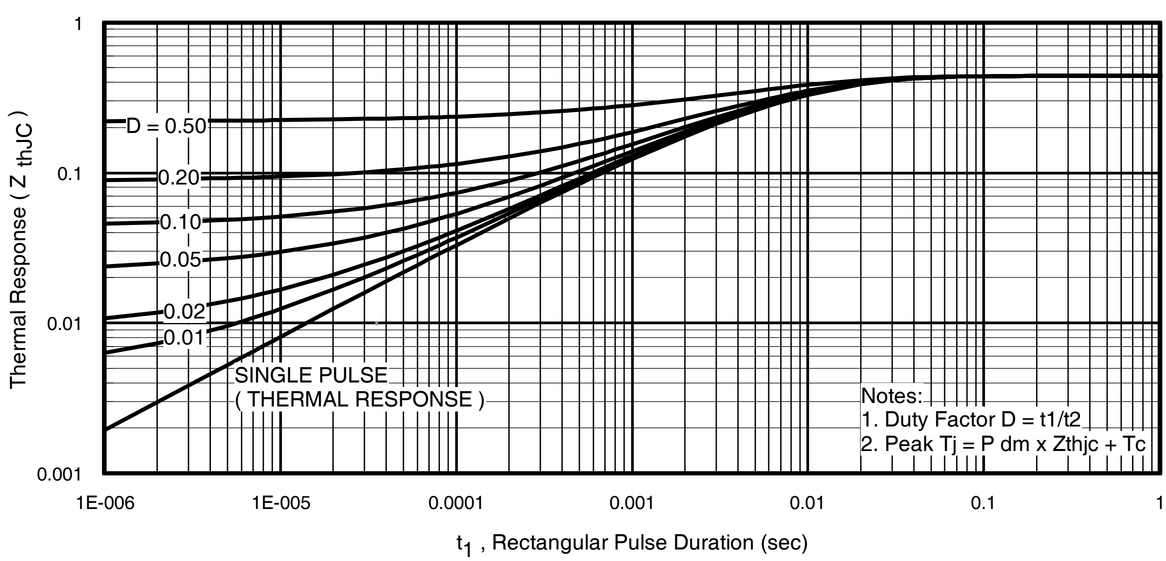


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

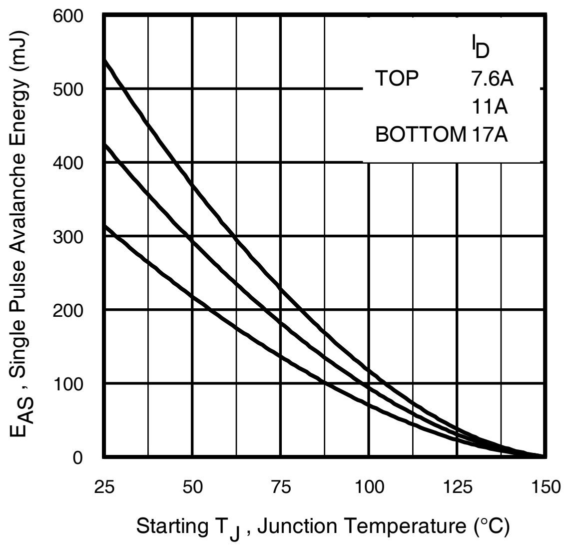


Fig 12. Maximum Avalanche Energy vs. Drain Current

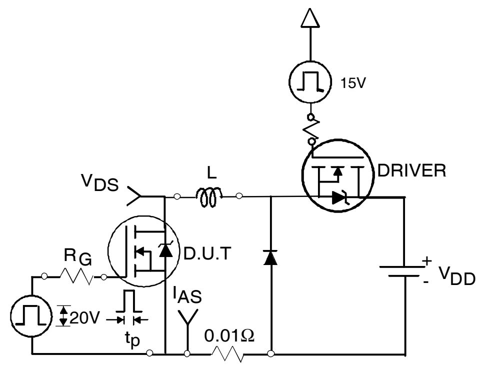


Fig 13a. Unclamped Inductive Test Circuit

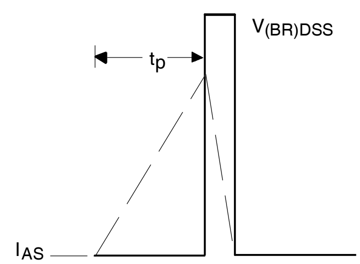


Fig 13b. Unclamped Inductive Waveforms

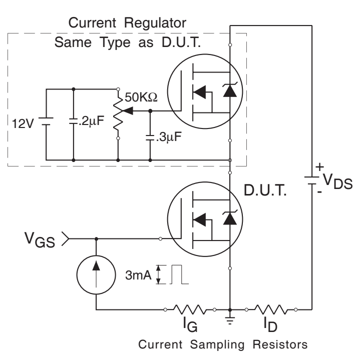


Fig 14a. Gate Charge Test Circuit

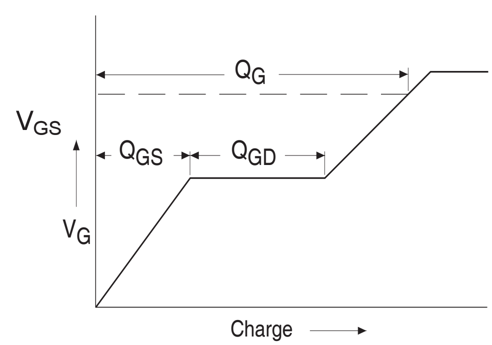
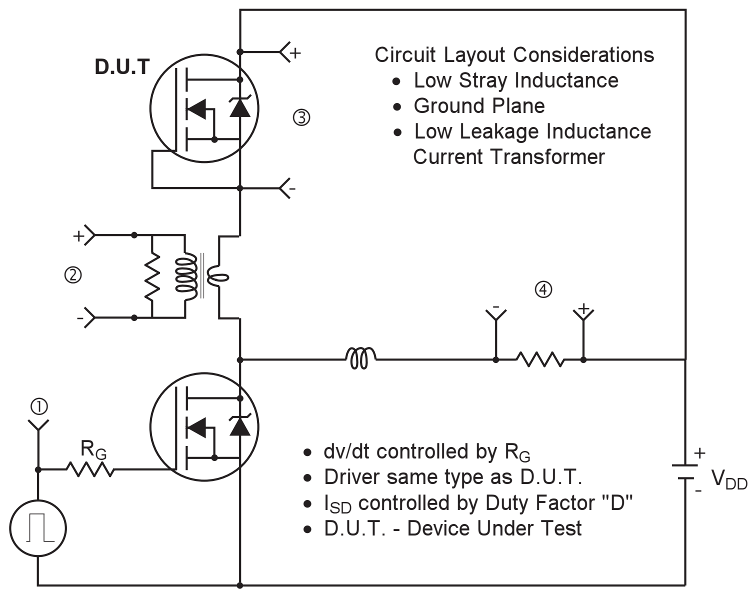
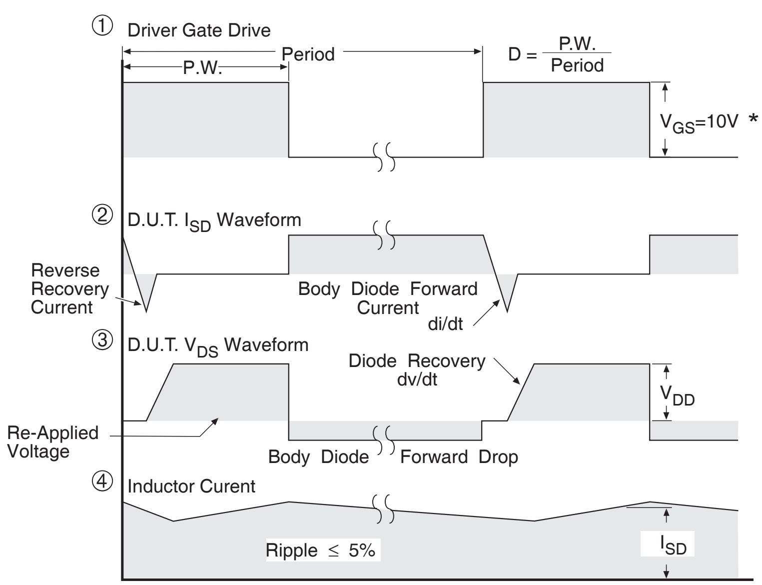


Fig 14b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



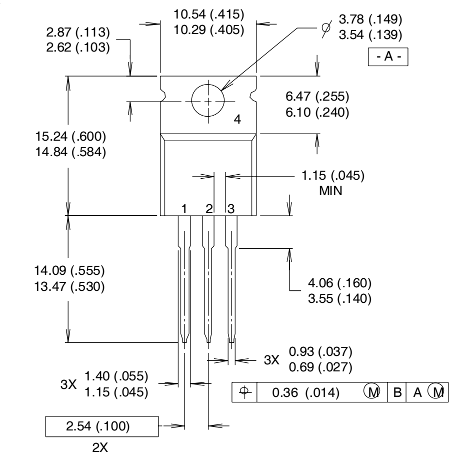


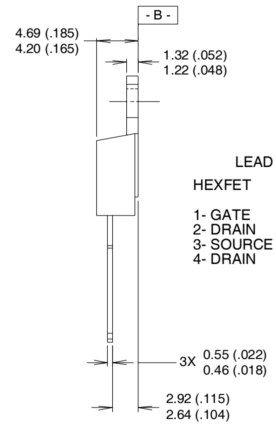
* V_{GS} = 5V for Logic Level Devices

Fig 15. For N-Channel HEXFET® Power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)





LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	4- COLLECTOR

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

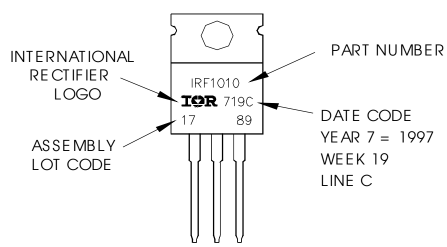
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
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08/04

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