NEW PRODUCT

400 mA LOAD SWITCH FEATURING PRE-BIASED PNP TRANSISTOR AND ESD PROTECTED N-MOSFET

General Description

- LMN400E01 is best suited for applications where the load needs to be turned on and off using control circuits like micro-controllers, comparators etc. particularly at a point of load. It features a discrete pass transistor with stable $V_{CE(SAT)}$ which does not depend on input voltage and can support continuous maximum current of 400 mA. It also contains an ESD protected discrete N-MOSFET that can be used as control. The component can be used as a part of a circuit or as a stand alone discrete device.

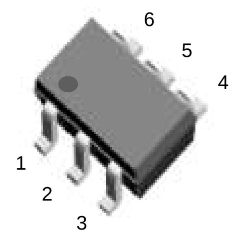

Fig. 1: SOT-363

Features

- Voltage Controlled Small Signal Switch
- N-MOSFET with ESD Gate Protection
- Surface Mount Package
- Ideally Suited for Automated Assembly Processes
- **Lead Free By Design/ROHS Compliant (Note 1)**
- **"Green" Device (Note 2)**

Mechanical Data

- Case: SOT-363
- Case Material: Molded Plastic. "Green Molding" Compound. UL Flammability Classification Rating 94V-0
- Moisture sensitivity: Level 1 per J-STD-020C
- Terminal Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL- STD -202, Method 208
- Marking & Type Code Information: See Last Page
- Ordering Information: See Last Page
- Weight: 0.016 grams (approximate)

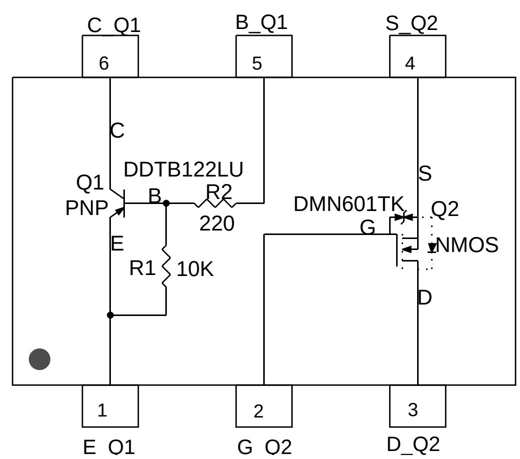

Fig 2 : Schematic and Pin Configuration

Sub-Component P/N	Reference	Device Type	R1(NOM)	R2(NOM)	Figure
DDTB122LU_DIE	Q1	PNP Transistor	10K	220	2
DMN601TK_DIE (ESD Protected)	Q2	N-MOSFET	¾	¾	2

Maximum Ratings, Total Device @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 3)	P_d	200	mW
Power Derating Factor above 37.5°C	P_{der}	1.6	mW/°C
Output Current	I_{out}	400	mA

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Junction Operation and Storage Temperature Range	T_j, T_{stg}	-55 to +150	°C
Thermal Resistance, Junction to Ambient Air (Note 3) (Equivalent to one heated junction of PNP transistor)	$R_{\theta JA}$	625	°C/W

Notes:
1. No purposefully added lead.
2. Diodes Inc.'s "Green" policy can be found on our website at http:/www.diodes.com/products/lead_free/index.php.
3. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

Maximum Ratings: @ T_A = 25°C unless otherwise specified
Sub-Component Device: Pre-Biased PNP Transistor (Q1)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	-50	V
Collector-Emitter Voltage	V_{CEO}	-50	V
Supply Voltage	V_{cc}	-50	V
Input Voltage	V_{in}	+5 to -6	V
Output Current	I_C	-400	mA

Sub-Component Device: @ T_A = 25°C unless otherwise specified
ESD Protected N-Channel MOSFET (Q2)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	60	V
Drain Gate Voltage (R_{GS} ≤1MOhm)		V_{DGR}	60	V
Gate-Source Voltage	Continuous	V_{GSS}	+/-20	V
	Pulsed (tp<50 uS)		+/-40	
Drain Current (Page 1: Note 3)	Continuous (V_{gs} = 10V)	I_D	300	mA
	Pulsed (tp <10 uS, Duty Cycle <1%)		800	
Continuous Source Current		I_S	300	mA

Electrical Characteristics: Pre-Biased PNP Transistor (Q1) @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Collector-Base Cut Off Current	I_{CBO}	¾	¾	-100	nA	V_{CB} = -50V, I_E = 0
Collector-Emitter Cut Off Current	I_{CEO}	¾	¾	-500	nA	V_{CE} = -50V, I_B = 0
Emitter-Base Cut Off Current	I_{EBO}	¾	¾	-1	mA	V_{EB} = -5V, I_C = 0
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	-50	¾	¾	V	I_C = -10 uA, I_E = 0
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	-50	¾	¾	V	I_C = -2 mA, I_B = 0
Input Off Voltage	$V_{I(OFF)}$	¾	−0.55	-0.3	V	V_{CE} = -5V, I_C = -100uA
Output Voltage	V_{OH}	-4.9	¾	¾	V	V_{CC} = -5V, V_B = -0.05V, R_L = 1K
Ouput Current (leakage current same as I_{CEO})	$I_{O(OFF)}$	¾	¾	-500	nA	V_{CC} = -50V, V_I = 0V
ON CHARACTERISTICS						
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	¾	¾	-0.15	V	I_C = -10 mA, I_B = -0.3 mA
		¾	¾	-0.15	V	I_C = -200mA, I_B = -20mA
		¾	¾	-0.3	V	I_C = -100mA, I_B = -1mA
		¾	¾	-0.2	V	I_C = -300mA, I_B= -30mA
		¾	¾	-0.25	V	I_C = -400mA, I_B= -40mA
		¾	¾	-0.3	V	I_C = -500mA, I_B = -50mA
Equivalent on-resistance*	$R_{CE(SAT)}$	¾	¾	1.125	Ω	I_C = -400mA, I_B = -20mA
DC Current Gain	h_{FE}	70	220	¾	¾	V_{CE} = -5V, I_C = -50 mA
		70	260	¾	¾	V_{CE} = -5V, I_C =- 100 mA
		70	265	¾	¾	V_{CE} = -5V, I_C = -200 mA
		70	225	¾	¾	V_{CE} = -5V, I_C = -400 mA
Input On Voltage	$V_{I(ON)}$	-2.45	-1.5	¾	V_{dc}	V_O = -0.3V, II_C = -2 mA
Output Voltage (equivalent to $V_{CE(SAT)}$)	$V_{O(on)}$ (V_{OL})	¾	-0.1	-0.3	V_{dc}	V_{CC} = -5V, V_B = -2.5V, $I_o/I_{I\ =}$ -50mA /-2.5mA
Input Current	I_i	¾	-18	-28	mA	V_I = -5V
Base-Emitter Turn-on Voltage	$V_{BE(ON)}$	¾	-1.2	-1.3	V	V_{CE} = -5V, I_C = -400mA
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	¾	-1.9	-2.2	V	I_C = -50mA, I_B = -5mA
		¾	-5.25	-5.5		I_C = -400mA, I_B = -20mA
Input Resistor (Base), +/- 30%	R2	0.154	0.22	0.286	KΩ	¾
Pull-up Resistor (Base to Vcc supply), +/- 30%	R1	¾	10	¾	KΩ	¾
Resistor Ratio (Input Resistor/Pullup resistor)	R1/R2	36	45	55	¾	¾
SMALL SIGNAL CHARACTERISTICS						
Transition Frequency (gain bandwidth product)	f_T	¾	200	¾	MHz	V_{CE} = -10V, I_E = -5mA, f = 100MHz
Collector capacitance, (Ccbo-Output Capacitance)	CC	¾	20	¾	pF	V_{CB} = -10V, I_E = 0A, f = 1MHz

* Pulse Test: Pulse width, tp <300 us, Duty Cycle, d ≤0.02

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Electrical Characteristics: ESD Protected N Channel MOSFET (Q2) @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 4)						
Drain-Source Breakdown Voltage, BVDSS	$V_{(BR)DSS}$	60	¾	¾	V	V_{GS} = 0V, I_D = 10uA
Zero Gate Voltage Drain Current (Drain Leakage Current)	I_{DSS}	¾	¾	1	µA	V_{GS} =0V, V_{DS} = 60V
Gate-Body Leakage Current, Forward	I_{GSSF}	¾	¾	10	µA	V_{GS} = 20V, V_{DS} = 0V
Gate-Body Leakage Current, Reverse	I_{GSSR}	¾	¾	-10	µA	V_{GS} = -20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 4)						
Gate Source Threshold Voltage (Control Supply Voltage)	$V_{GS(th)}$	1	1.6	2.5	V	V_{DS} = V_{GS}, I_D = 0.25mA
Static Drain-Source On-State Voltage	$V_{DS(on)}$	¾	0.09	1.5	V	V_{GS} = 5V, I_D = 50mA
		¾	0.6	3.75		V_{GS} = 10V, I_D = 500mA
On-State Drain Current	$I_{D(on)}$	500	¾	¾	mA	V_{GS} = 10V, V_{DS} ≥2*$V_{DS(ON)}$
Static Drain-Source On Resistance	$R_{DS(on)}$	¾	1.6	3	Ω	V_{GS} = 5V, ID = 50mA
		¾	1.2	2		V_{GS} = 10V, ID = 500mA
Forward Transconductance	g_{FS}	80	260	¾	mS	V_{DS} ≥2*$V_{DS(ON)}$, I_D = 200 mA
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	¾	¾	50	pF	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	¾	¾	25	pF	
Reverse Transfer Capacitance	C_{rss}	¾	¾	5	pF	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	$td_{(on)}$	¾	¾	20	ns	V_{DD} = 30V, V_{GS} =10V, I_D = 200mA, R_G = 25 Ohm, R_L = 150 Ohm
Turn-Off Delay Time	$td_{(off)}$	¾	¾	40	ns	
SOURCE-DRAIN (BODY) DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward On-Voltage	V_{SD}	¾	0.88	1.5	V	V_{GS} = 0V, I_S = 300 mA*
Maximum Continuous Drain-Source Diode Forward Current (Reverse Drain Current)	I_S	¾	¾	300	mA	
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}	¾	¾	800	mA	

* Pulse Test: Pulse width, tp <300 us, Duty Cycle, d ≤0.02

Notes: 4. Short duration test pulse used to minimize self-heating effect.

NEW PRODUCT

Typical Characteristics

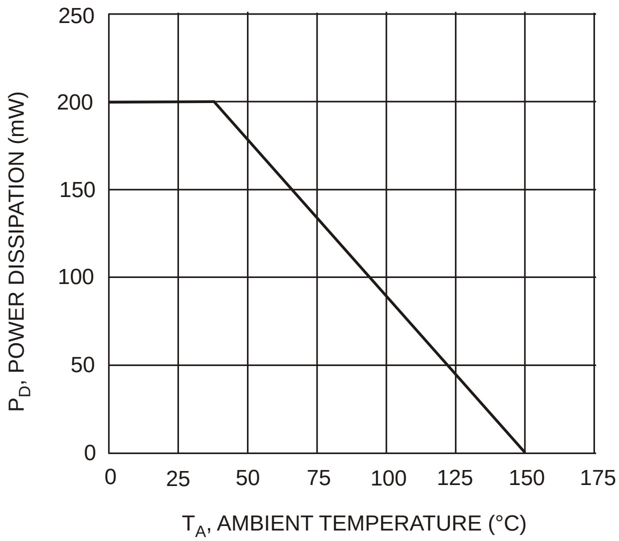

Fig. 3, Max Power Dissipation vs
Ambient Temperature

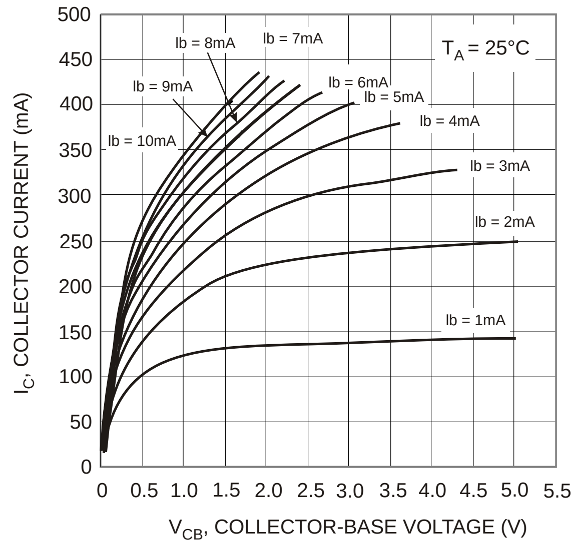

Fig. 4, Output Current vs.
Voltage Drop (Pass Element PNP)

Pre-Biased PNP Transistor Characteristics

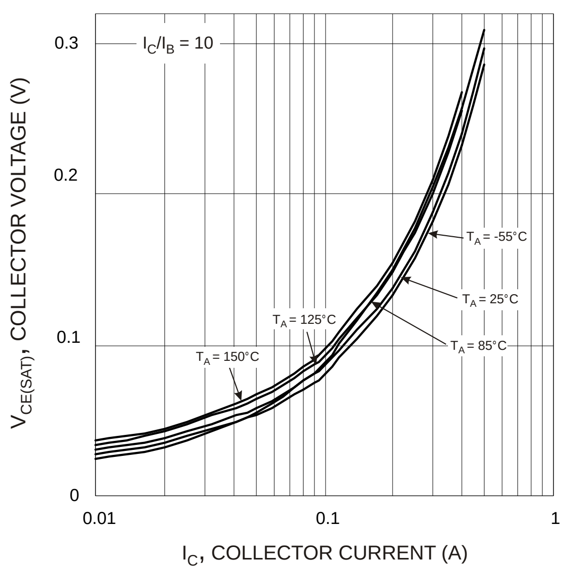

Fig. 5 $V_{CE(SAT)}$ vs. I_C @ I_C/I_B = 10

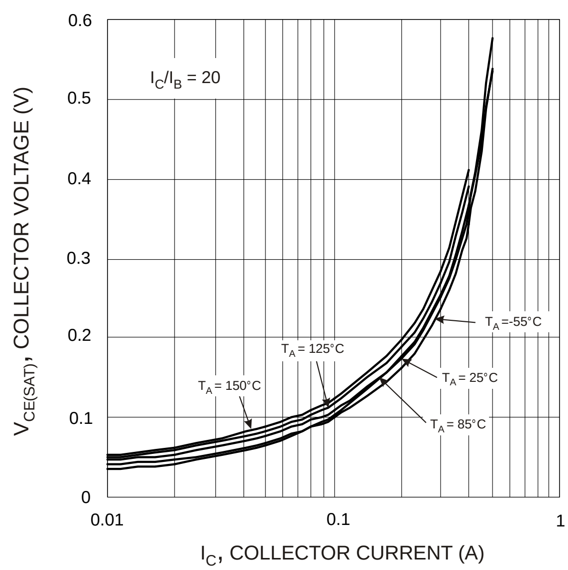

Fig. 6 $V_{CE(SAT)}$ vs. I_C @ I_C/I_B = 20

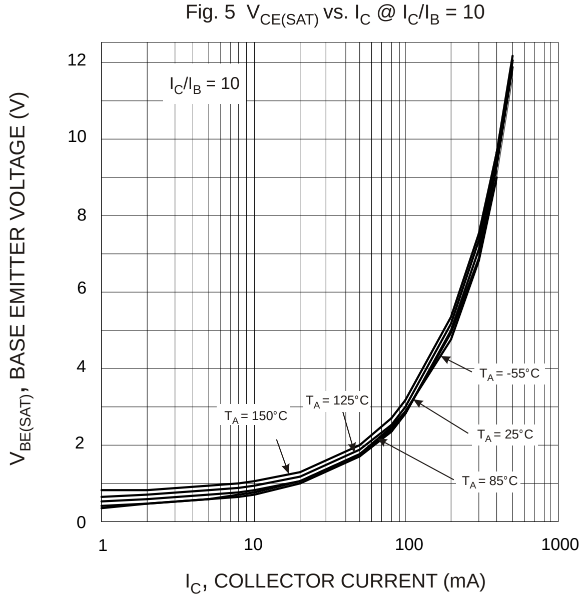

Fig. 7 $V_{BE(SAT)}$ vs. I_C @ I_C/I_B = 10

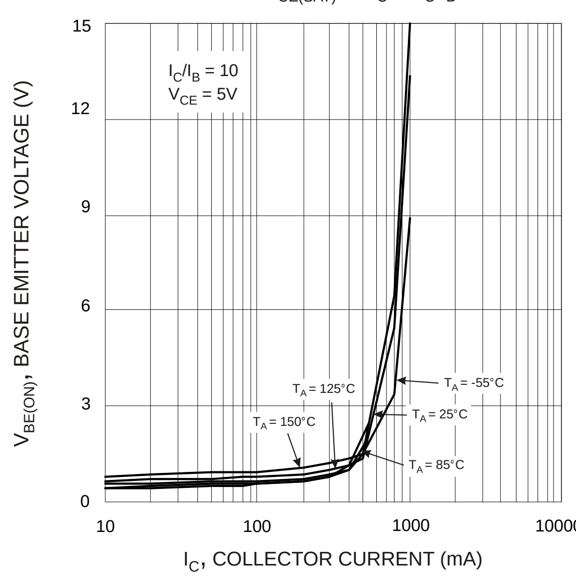

Fig. 8 $V_{BE(ON)}$ vs. I_C @ V_{CE} = 5V

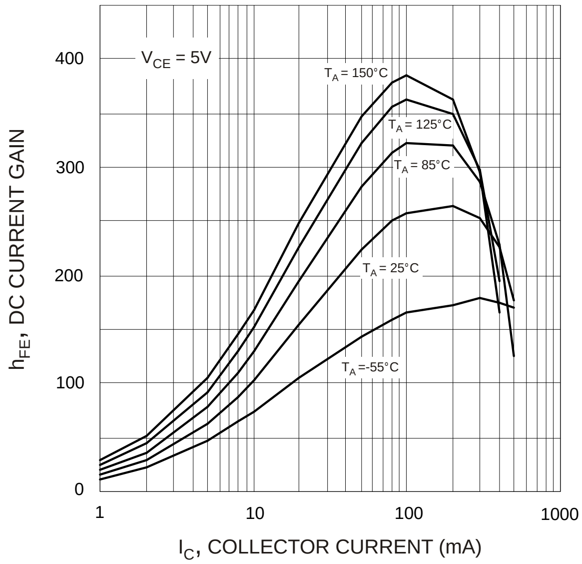

Fig. 9 h_{FE} vs. I_C @ V_{CE} = 5V

Typical N-Channel MOSFET (ESD Protected) Characteristics

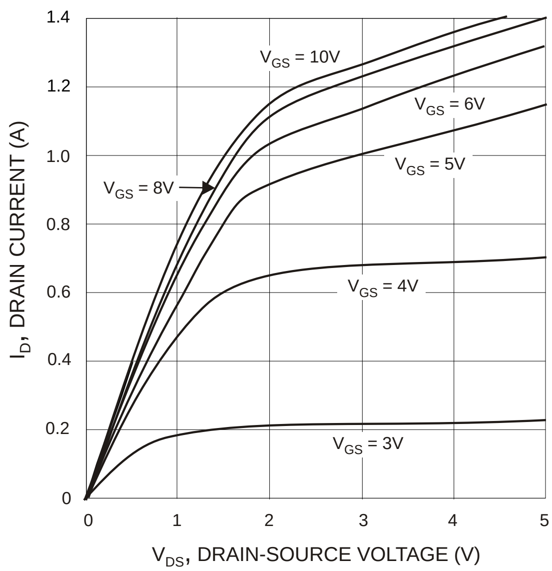

Fig. 10 Output Characteristics

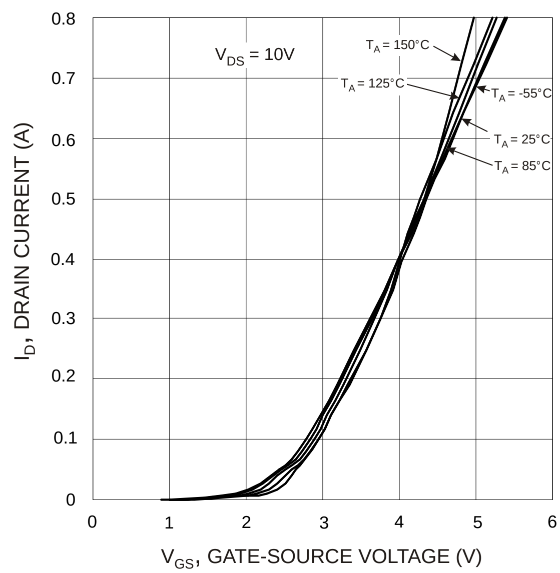

Fig. 11 Transfer Characteristics

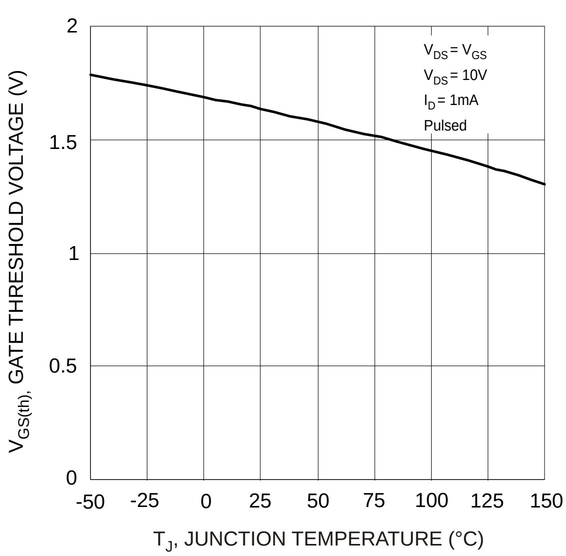

Fig. 12 Gate Threshold Voltage
vs. Junction Temperature

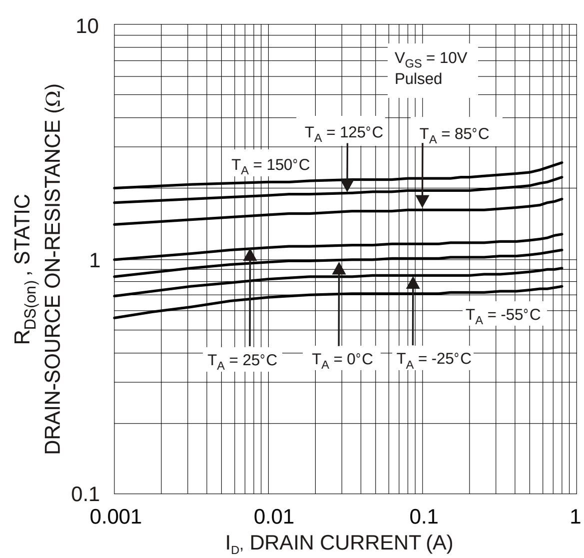

Fig. 13 Static Drain-Source On-Resistance
vs. Drain Current

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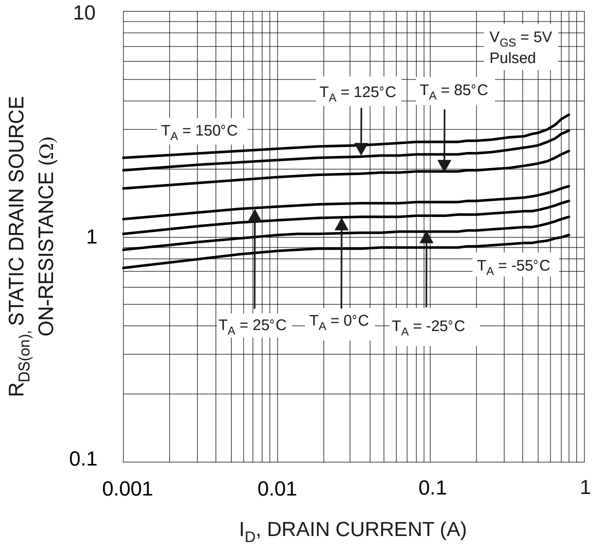

Fig. 14 Static Drain-Source On-Resistance vs. Drain Current

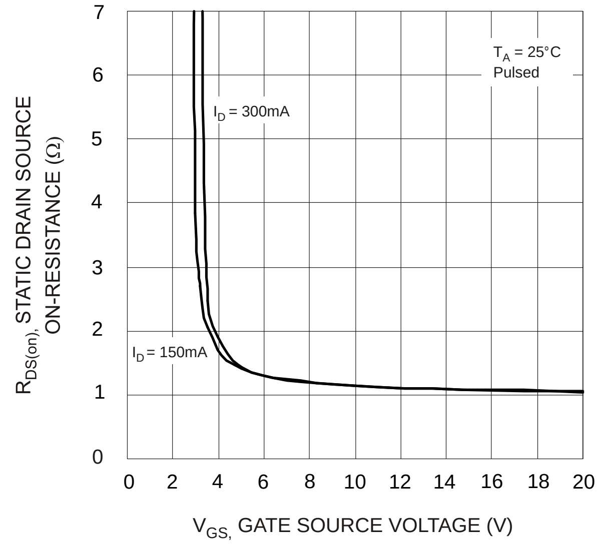

Fig. 15 Static Drain-Source On-Resistance vs. Gate-Source Voltage

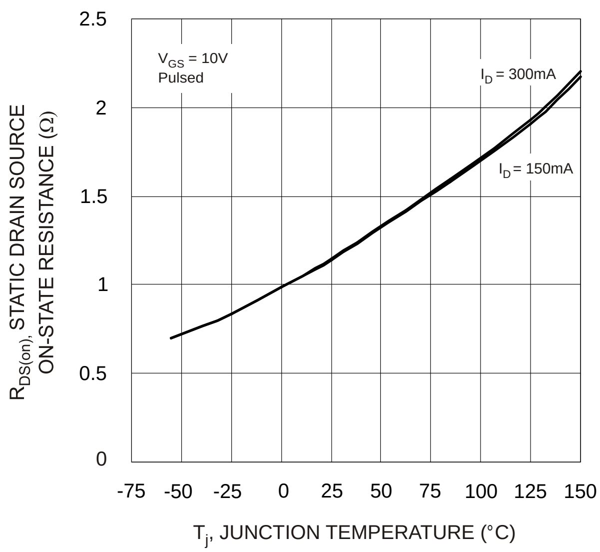

Fig. 16 Static Drain-Source On-State Resistance vs. Junction Temperature

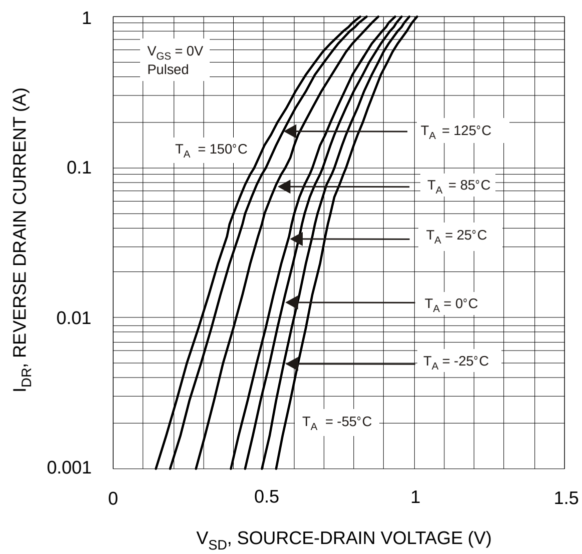

Fig. 17 Reverse Drain Current vs. Source-Drain Voltage

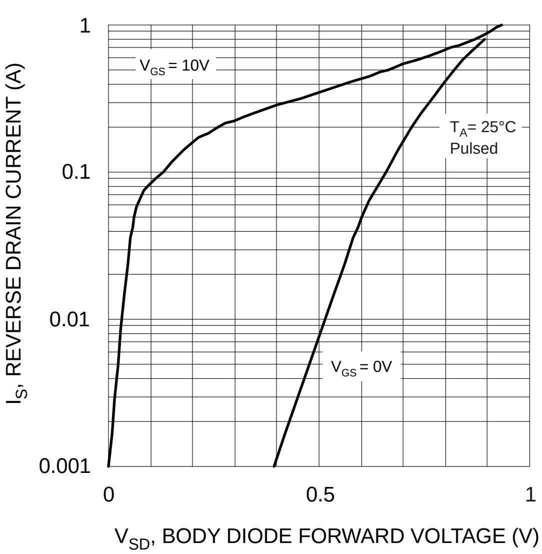

Fig. 18 Reverse Drain Current vs. Source-Drain Voltage

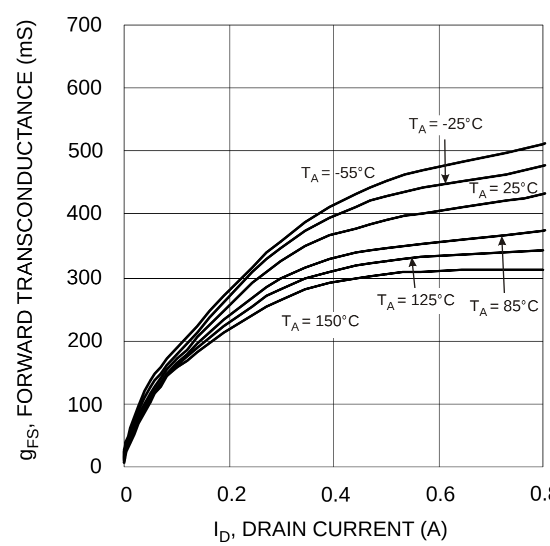

Fig. 19 Forward Transconductance vs. Drain Current ($V_{DS} > I_D * R_{DS(ON)}$)

Application Details

- PNP Transistor (DDTB122LU) and ESD Protected N-MOSFET (DMN601TK) integrated as one in LMN400E01 can be used as a discrete entity for general application or as an integrated circuit to function as a Load Switch. When it is used as the latter as shown in Fig. 20, various input voltage sources can be used as long as it does not exceed the maximum ratings of the device. These devices are designed to deliver continuous output load current up to a maximum of 400 mA. The MOSFET Switch draws no current, hence loading of control circuitry is prevented. Care must be taken for higher levels of dissipation while designing for higher load conditions. These devices provide high power and also consume less space. The product mainly helps in optimizing power usage, thereby conserving battery life in a controlled load system like portable battery powered applications. (Please see Fig. 21 for one example of a typical application circuit used in conjunction with a voltage regulator as a part of power management system).

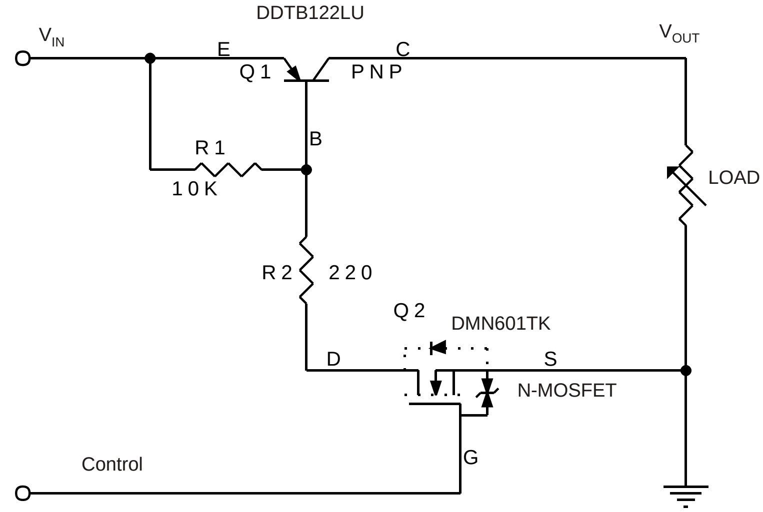

Fig 20 : Circuit Diagram

Typical Application Circuit

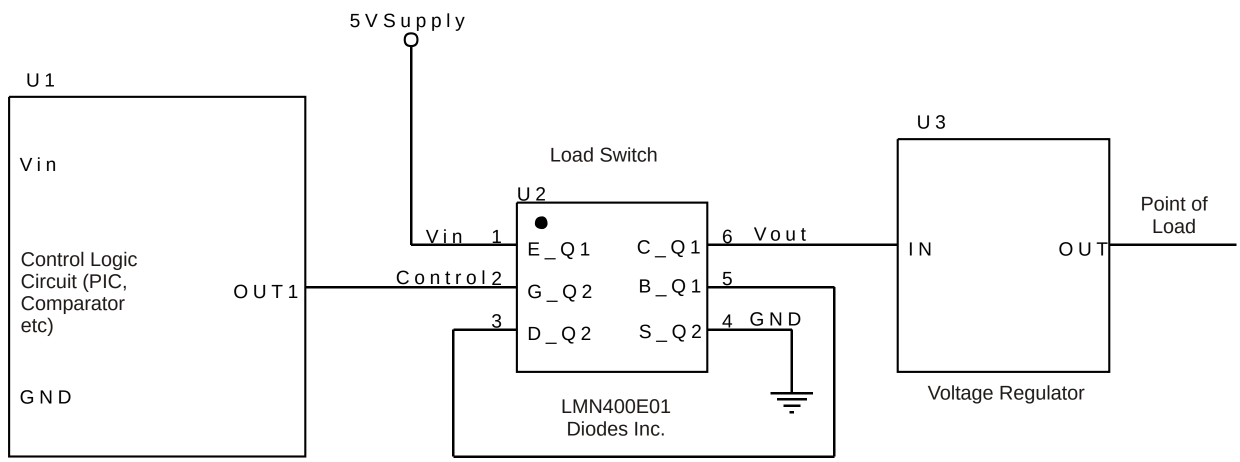

Fig 21

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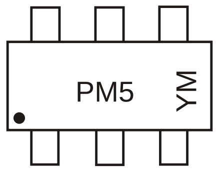
Ordering Information (Note 4)

Device	Marking Code	Packaging	Shipping
LMN400E01-7	PM5	SOT-363	3000/Tape & Reel

Notes: 4. For Packaging Details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information



PM5 = Product Type Marking Code,
YM = Date Code Marking
Y = Year, e.g., T = 2006
M = Month, e.g., 9 = September

Fig. 22

Date Code Key

Year	2006	2007	2008	2009
Code	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Package Details

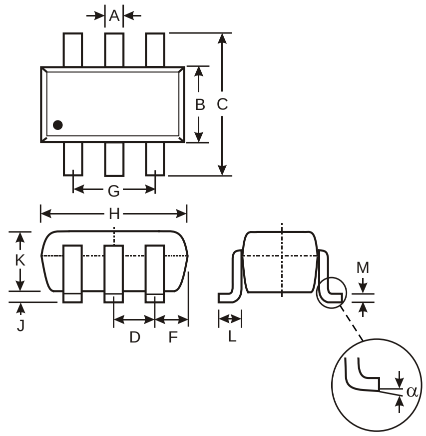


Fig. 23

SOT-363		
Dim	Min	Max
A	0.10	0.30
B	1.15	1.35
C	2.00	2.20
D	0.65 Nominal	
F	0.30	0.40
H	1.80	2.20
J	¾	0.10
K	0.90	1.00
L	0.25	0.40
M	0.10	0.25
α	0°	8°
All Dimensions in mm		

Suggested Pad Layout: (Based on IPC-SM-782)

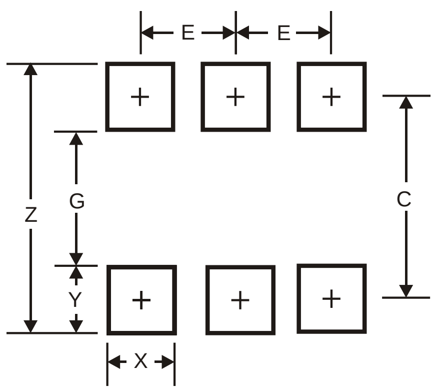


Fig. 24

Figure 14 Dimensions	SOT-363*
Z	2.5
G	1.3
X	0.42
Y	0.6
C	1.9
E	0.65

* Typical dimensions in mm