MK74CB218
Dual 1 to 8 Buffalo™ Clock Driver

Description

The MK74CB218 Buffalo™ is a monolithic CMOS high speed clock driver. It consists of two identical single input to eight low-skew output, non-inverting clock drivers. This eliminates concerns of part to part matching in many systems. The MK74CB218 is packaged in the tiny 28 pin SSOP, which uses the same board space as the narrow 16 pin SOIC. The inputs can be connected together for a 1 to 16 fanout buffer.

A quad 1 to 4, and PECL versions, are also available. Consult ICS for more details.

The MK74CB218 can also act as a voltage translator, since it is possible to run the inputs at 3.3 V and the outputs at 2.5 V.

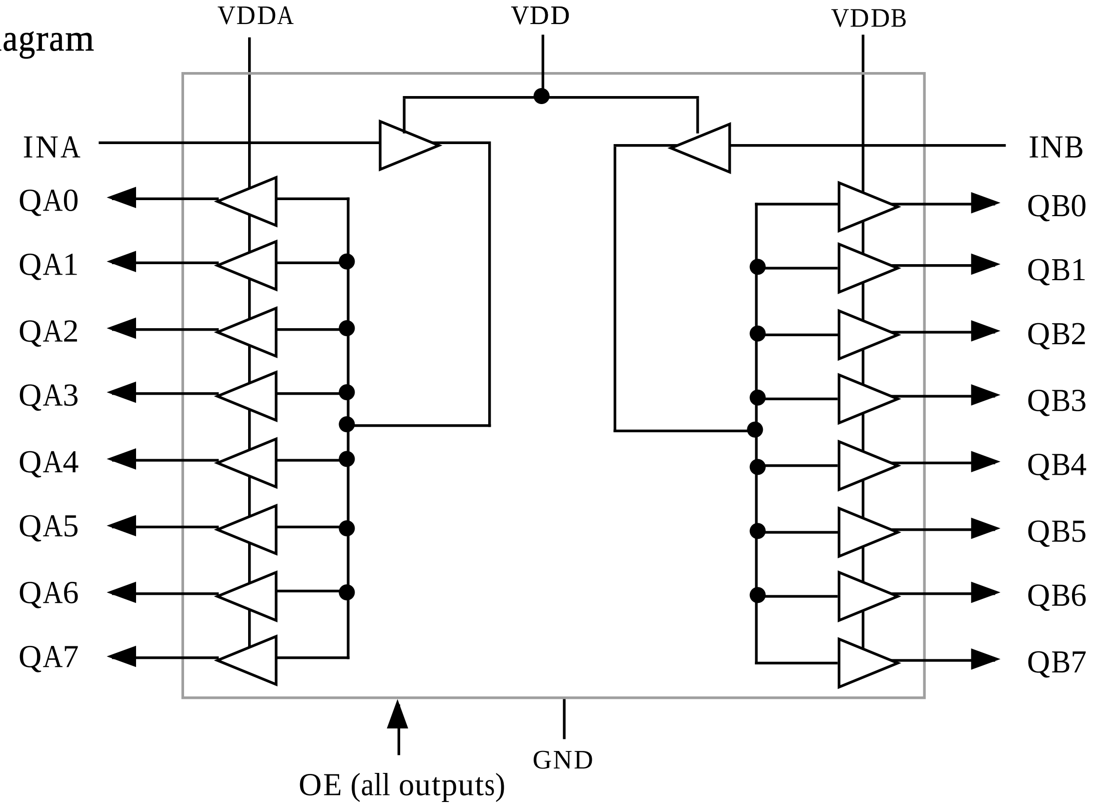
Features

- Tiny 28 pin SSOP (150 mil) package
- Dual one input to eight output clock drivers
- Outputs are skew matched to within 250 ps
- A outputs and B outputs matched to 250 ps
- 2.5 V, 3.3 V or 5 V supply voltages
- Output Enable tri-states each bank of eight
- Clock speeds up to 200 MHz

Family of ICS Parts

The MK74CB218 Buffalo™ is designed to be used with ICS's clock synthesizer devices. The inputs of the Buffalo are matched to the outputs of ICS clock synthesizers. Consult ICS for applications support.

Block Diagram



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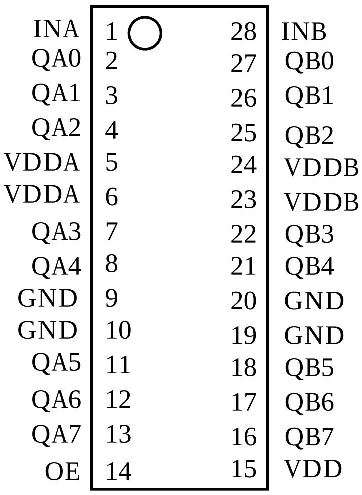
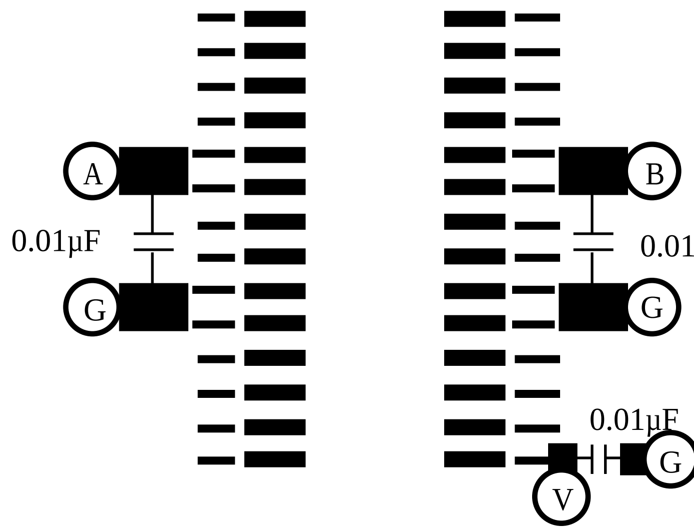
Pin Assignment



Suggested Layout



For simplicity, series terminating resistors are not shown for the outputs, but should be placed as close to the device as possible. It is most critical to have the 0.01µF decoupling capacitors closest.

(A) = connect to VDDA
(B) = connect to VDDB
(V) = connect to VDD
(G) = connect to low inductance ground plane

Pin Descriptions

Number	Name	Type	Description
1	INA	I	Clock input for eight A outputs.
2, 3, 4	QA0, QA1, QA2	O	Clock A outputs.
5, 6	VDDA	P	Power supply for QA outputs. Connect to a voltage from 2.5V to 5V. Cannot exceed VDD.
7, 8	QA3, QA4	O	Clock A outputs.
9, 10	GND	P	Connect to ground.
11, 12, 13	QA5, QA6, QA7	O	Clock A outputs.
14	OE	I	Output Enable. Tri-states all clock outputs when this input is low. Internal pull-up to VDD.
15	VDD	P	Power supply for inputs.
16, 17, 18	QB7, QB6, QB5	O	Clock B outputs.
19, 20	GND	P	Connect to ground.
21, 22	QB4, QB3	O	Clock B outputs.
23, 24	VDDB	P	Power supply for QB outputs. Connect to a voltage from 2.5V to 5V. Cannot exceed VDD.
25, 26, 27	QB2, QB1, QB0	O	Clock B outputs.
28	INB	I	Clock input for eight B outputs.

Type: I = Input, O = output, P = power supply connection

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Electrical Specifications

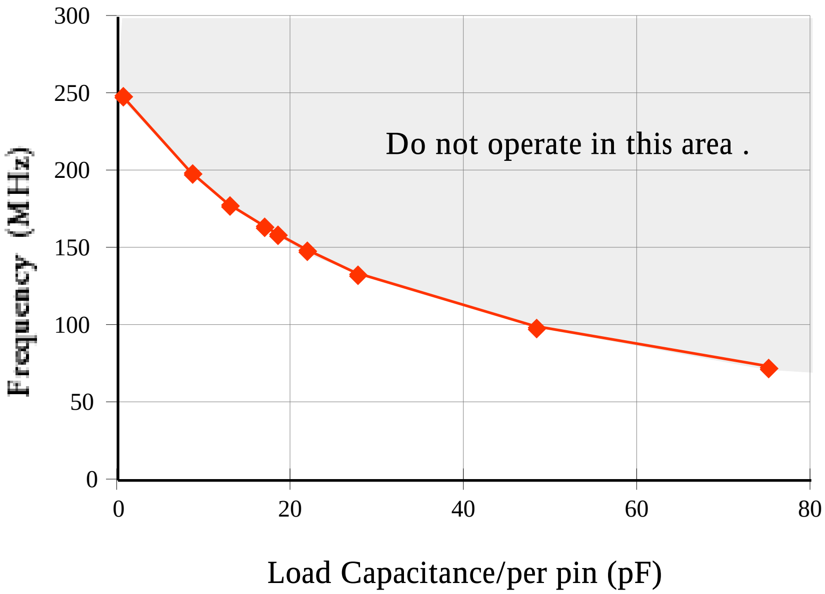
Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 20 seconds			260	°C
Storage Temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Operating Voltage, VDD		3.0	3.3	5.5	V
Operating Voltage, VDDA or VDDB		2.375		VDD	V
Input High Voltage, VIH (INA, INB pins)		VDD-1.0	VDD/2		V
Input Low Voltage, VIL (INA, INB pins)			VDD/2	1.0	V
Input High Voltage, VIH (OE pin)		2.0			V
Input Low Voltage, VIL (OE pin)				0.8	V
Output High Voltage, 3.3V and 5V	IOH=-12mA	VDD-0.4			V
Output High Voltage, 3.3V and 5V	IOH=-25mA	2.4			V
Output Low Voltage, 3.3V and 5V	IOL=25mA			0.8	V
Output High Voltage, 2.5V	IOH=-16mA	2			V
Output Low Voltage, 2.5V	IOL=16mA			0.5	V
Operating Supply Current, IDD, at 100 MHz	No Load		55		mA
Output Impedance			14		Ω
Short Circuit Current	Each output		100		mA
On-Chip Pull-up Resistor	OE		250		kΩ
Input Capacitance			7		pF
AC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Input Clock Frequency	Note 4	0		200	MHz
Propagation Delay with load=15pF			1.4	3	ns
Output Clock Rise Time	0.8 to 2.0V			2	ns
Output Clock Fall Time	2.0 to 0.8V			2	ns
Output Clock Rising Edge Skew	At VDD/2. Note 2		100	250	ps
Output Clock A to B Skew	At VDD/2. Note 3		100	250	ps
Output Enable Time, OE high to output on				20	ns
Output Disable Time, OE low to tri-state				20	ns

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Between any two A outputs, or any two B outputs, with equal loading.
3. Between any clock A output and any clock B output with INA connected to INB, and equal loading.
4. See discussion and graph of speed versus load.

Maximum Speed

The maximum speed at which the chip can operate is limited by power dissipation in the package. Graph 1 shows the operating frequency plotted against load capacitance per pin for a die temperature of 125°C. This is at VDD = VDDA = VDDB = 3.3 V, 70°C and with 33 Ω series termination resistors. The termination resistors are essential because they allow a large proportion of the total power to be dissipated outside the package. Reducing or eliminating the series termination will cause an increase in die temperature. It is not recommended to operate the chip at die temperatures greater than 125°C. Also note that the load capacitance per pin must include PC board parasitics such as trace capacitance.

If not all outputs of the chip are used, it is possible to operate the chip faster with larger loads. Consult ICS for your specific requirement.



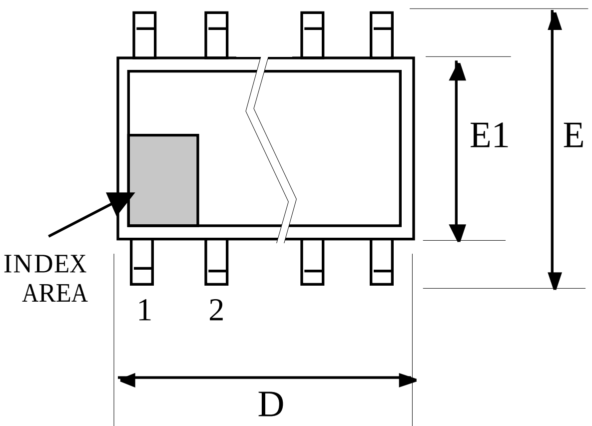
Graph 1
MK74CB218
Maximum Speed with all VDDs at 3.3V

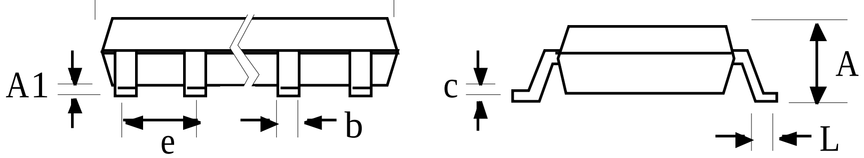
Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)

28 pin SSOP

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
D	0.337	0.344	8.55	8.75
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.80	6.20
E1	0.150	0.157	3.80	4.00
L	0.016	0.050	0.40	1.27





Ordering Information

Part/Order Number	Marking	Package	Temperature
MK74CB218R	MK74CB218R	28 pin SSOP	0-70 °C
MK74CB218RTR	MK74CB218R	Add Tape & Reel	0-70 °C