# **Power MOSFET**

# 20 V, 7.2 A, N-Channel ChipFET™

#### **Features**

- Low R<sub>DS(on)</sub> for Higher Efficiency
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package Saves Board Space
- Pb-Free Package is Available

## **Applications**

Power Management in Portable and Battery-Powered Products; i.e.,
 Cellular and Cordless Telephones and PCMCIA Cards

# **MAXIMUM RATINGS** ( $T_A = 25^{\circ}C$ unless otherwise noted)

( <del>//</del>					
Rating	Symbol	5 Secs	Steady State	Unit	
Drain-Source Voltage	V <sub>DS</sub>	20		V	
Gate-Source Voltage	$V_{GS}$	±12		V	
Continuous Drain Current $(T_J = 150^{\circ}C)$ (Note 1) $T_A = 25^{\circ}C$ $T_A = 85^{\circ}C$	l <sub>D</sub>	7.2 5.2	5.2 3.8	А	
Pulsed Drain Current	I <sub>DM</sub>	±20		Α	
Continuous Source Current (Diode Conduction) (Note 1)	I <sub>S</sub>	7.2	5.2	Α	
Maximum Power Dissipation (Note 1)  T <sub>A</sub> = 25°C  T <sub>A</sub> = 85°C	P <sub>D</sub>	2.5 1.3	1.3 0.7	W	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150		°C	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

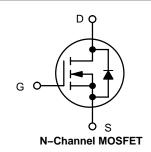
 Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

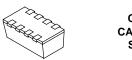


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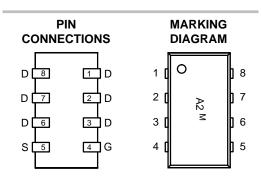
#### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX	
20 V	25 mΩ @ 4.5 V	7.2 A	





ChipFET CASE 1206A STYLE 1



A2 = Specific Device Code M = Month Code

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTHS5404T1	ChipFET	3000/Tape & Reel
NTHS5404T1G	ChipFET (Pb-Free)	3000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Тур	Max	Unit
Maximum Junction–to–Ambient (Note 2) t ≤ 5 sec Steady State	$R_{ hetaJA}$	40 80	50 95	°C/W
Maximum Junction-to-Foot (Drain) Steady State	$R_{ hetaJF}$	15	20	°C/W

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Тур	Max	Unit
Static				•		
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.6	-	_	V
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$	-	-	±100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$ $V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$		-	-	1.0	μΑ
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V},$ $T_{J} = 85^{\circ}\text{C}$	-	_	5.0	
On-State Drain Current (Note 3)	I <sub>D(on)</sub>	$V_{DS} \ge 5.0 \text{ V}, V_{GS} = 4.5 \text{ V}$	20	-	-	Α
Drain-Source On-State Resistance (Note 3)	r <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 5.2 \text{ A}$	-	0.025	0.030	Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 4.3 \text{ A}$	-	0.038	0.045	1
Forward Transconductance (Note 3)	9fs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.2 A	-	20	_	S
Diode Forward Voltage (Note 3)	$V_{SD}$	I <sub>S</sub> = 5.2 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V
Dynamic (Note 4)						
Total Gate Charge	$Q_{G}$		-	12	18	nC
Gate-Source Charge	$Q_{GS}$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_{D} = 5.2 \text{ A}$	-	2.4	_	
Gate-Drain Charge	$Q_{GD}$		-	3.2	_	
Turn-On Delay Time	t <sub>d(on)</sub>		-	20	30	ns
Rise Time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_L = 10 \Omega$	-	40	60	]
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 1.0 \text{ A}, V_{GEN} = 4.5 \text{ V},$ $R_G = 6 \Omega$	-	40	60	1
Fall Time	t <sub>f</sub>	1	-	15	23	1
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1.1 A, di/dt = 100 A/μs	_	30	60	1

Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
 Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Guaranteed by design, not subject to production testing.

#### TYPICAL ELECTRICAL CHARACTERISTICS

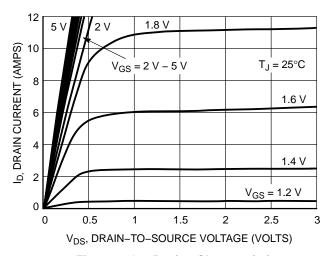


Figure 1. On-Region Characteristics

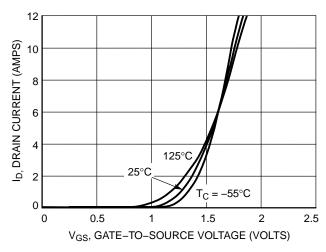


Figure 2. Transfer Characteristics

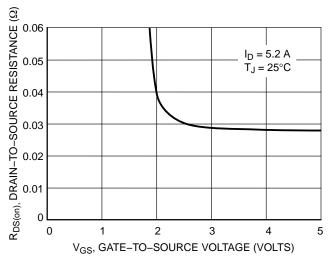


Figure 3. On–Resistance versus Gate–to–Source Voltage

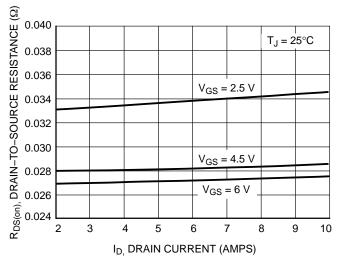


Figure 4. On-Resistance versus Drain Current and Gate Voltage

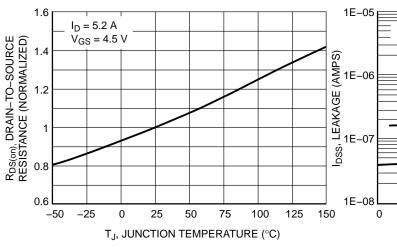


Figure 5. On–Resistance Variation with Temperature

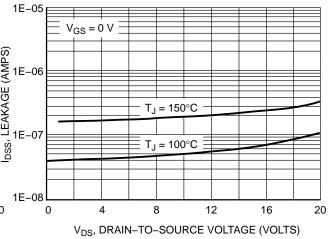
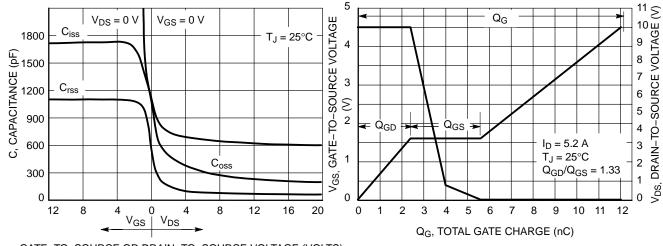


Figure 6. Drain-to-Source Leakage Current versus Voltage

#### TYPICAL ELECTRICAL CHARACTERISTICS



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

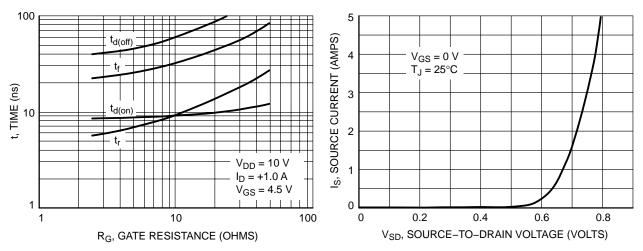


Figure 9. Resistive Switching Time Variation versus Gate Resistance

Figure 10. Diode Forward Voltage versus Current

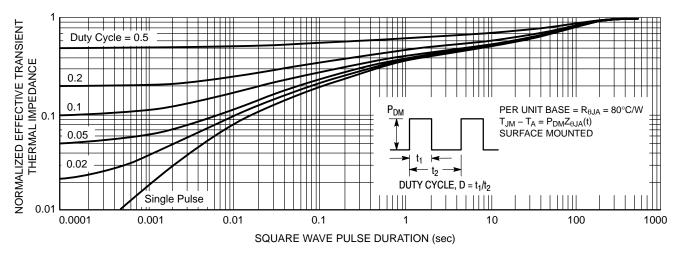


Figure 11. Normalized Thermal Transient Impedance, Junction-to-Ambient

# **SOLDERING FOOTPRINT\***

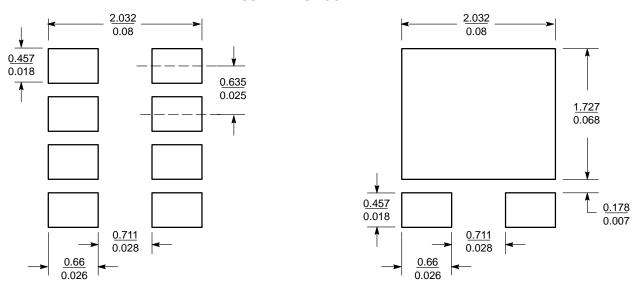


Figure 12. Basic

Figure 13. Style 1

#### **BASIC PAD PATTERNS**

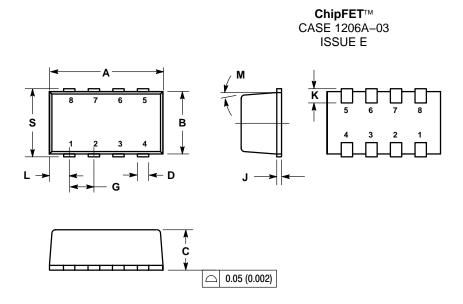
The basic pad layout with dimensions is shown in Figure 12. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 13 improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the

confines of the basic footprint. The drain copper area is 0.0054 sq. in. (or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper lead–frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
- LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM
- DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE
- 6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
- 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

	MILLIMETERS		INC	INCHES	
DIM	MIN	MAX	MIN	MAX	
Α	2.95	3.10	0.116	0.122	
В	1.55	1.70	0.061	0.067	
С	1.00	1.10	0.039	0.043	
D	0.25	0.35	0.010	0.014	
G	0.65 BSC		0.02	0.025 BSC	
J	0.10	0.20	0.004	0.008	
K	0.28	0.42	0.011	0.017	
L	0.55 BSC		0.02	2 BSC	
M	5 °	5° NOM		NOM	
S	1.80	2.00	0.072	0.080	

STYLE 1: PIN 1. DRAIN

- 2. DRAIN
  3. DRAIN
  4. GATE
  5. SOURCE
  6. DRAIN
  7. DRAIN

- 8. DRAIN

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