MC74VHCT126A

Quad Bus Buffer
with 3–State Control Inputs

The MC74VHCT126A is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves noninverting high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT126A requires the 3–state control input (OE) to be set Low to place the output into high impedance.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

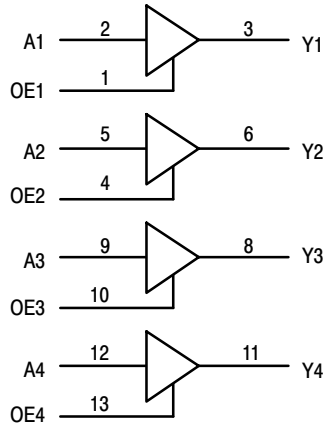
The VHCT126A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 3.8ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8V; V_{IH} = 2.0V
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 72 FETs or 18 Equivalent Gates

LOGIC DIAGRAM

Active–High Output Enables

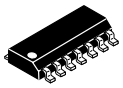


FUNCTION TABLE

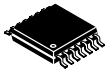
VHCT126A		
Inputs		Output
A	OE	Y
H	H	H
L	H	L
X	L	Z

ON Semiconductor

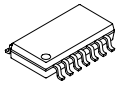
http://onsemi.com



14–LEAD SOIC
D SUFFIX
CASE 751A

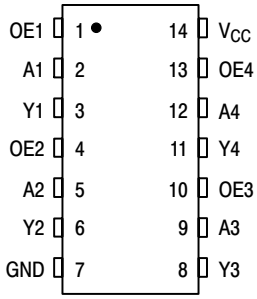


14–LEAD TSSOP
DT SUFFIX
CASE 948G



14–LEAD SOIC EIAJ
M SUFFIX
CASE 965

PIN CONNECTION AND MARKING DIAGRAM (Top View)



For detailed package marking information, see the Marking Diagram section on page 4 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT126AD	SOIC	55 Units/Rail
MC74VHCT126ADT	TSSOP	96 Units/Rail
MC74VHCT126AM	SOIC EIAJ	50 Units/Rail

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} =5.0V ±0.5V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			T_A ≤ 85°C		T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = – 50μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Maximum Low–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4V	5.5			1.35		1.50		1.65	mA
I_{OZ}	Maximum 3–State Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	5.5			±0.25		±2.5		±2.5	μA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \leq 85°C$ Min	$T_A \leq 85°C$ Max	$T_A \leq 125°C$ Min	$T_A \leq 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 3.3 \pm 0.3V$ $C_L = 15pF$		5.6	8.0	1.0	9.5		12.0	ns
		$C_L = 50pF$		8.1	11.5	1.0	13.0		16.0	
		$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$		3.8	5.5	1.0	6.5		8.5	
		$C_L = 50pF$		5.3	7.5	1.0	8.5		10.5	
t_{PZL}, t_{PZH}	Maximum Output Enable TIme, $\overline{OE}$ to Y	$V_{CC} = 3.3 \pm 0.3V$ $C_L = 15pF$ $R_L = 1k\Omega$		5.4	8.0	1.0	9.5		11.5	ns
		$C_L = 50pF$		7.9	11.5	1.0	13.0		15.0	
		$V_{CC} = 5.0 \pm 0.5V$ $C_L = 15pF$ $R_L = 1k\Omega$		3.6	5.1	1.0	6.0		7.5	
		$C_L = 50pF$		5.1	7.1	1.0	8.0		9.5	
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time, $\overline{OE}$ to Y	$V_{CC} = 3.3 \pm 0.3V$ $C_L = 50pF$ $R_L = 1k\Omega$		9.5	13.2	1.0	15.0		18.0	ns
		$V_{CC} = 5.0 \pm 0.5V$ $C_L = 50pF$ $R_L = 1k\Omega$		6.1	8.8	1.0	10.0		12.0	
t_{OSLH}, t_{OSHL}	Output–to–Output Skew	$V_{CC} = 3.3 \pm 0.3V$ $C_L = 50pF$ (Note 1.)			1.5		1.5		2.0	ns
		$V_{CC} = 5.0 \pm 0.5V$ $C_L = 50pF$ (Note 1.)			1.0		1.0		1.5	
C_{in}	Maximum Input Capacitance			4	10		10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High Impedance State)			6						pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 2.)	15	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per buffer). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50pF$, $V_{CC} = 5.0V$)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.3	– 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

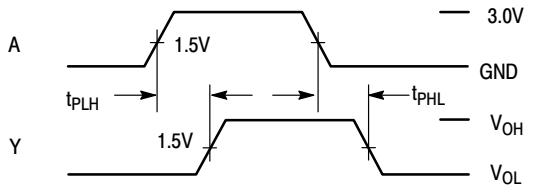


Figure 1.

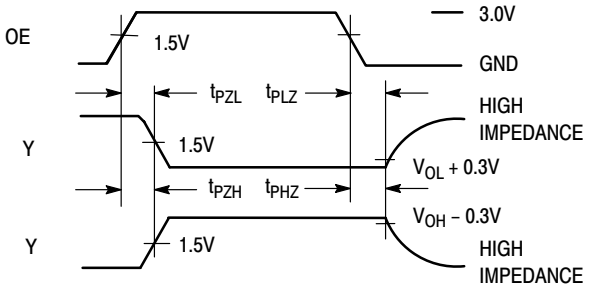
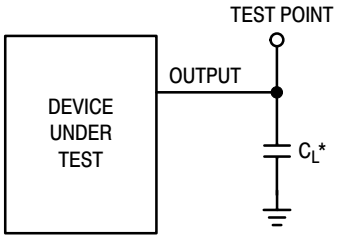
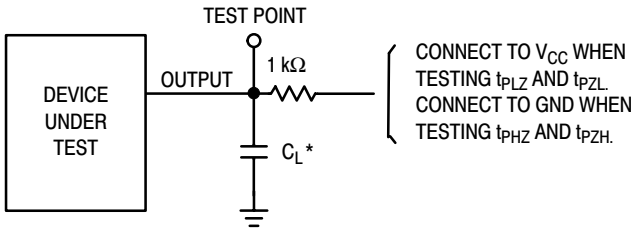


Figure 2.



*Includes all probe and jig capacitance

Figure 3. Test Circuit

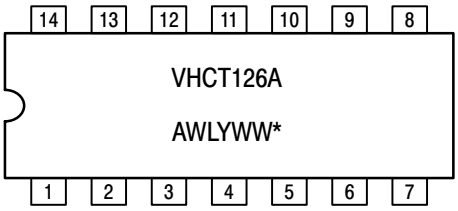


*Includes all probe and jig capacitance

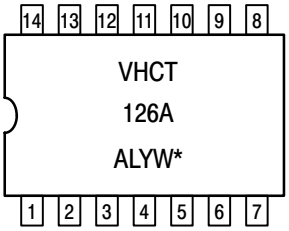
Figure 4. Test Circuit

MARKING DIAGRAMS

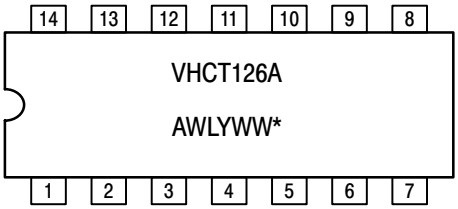
(Top View)



14–LEAD SOIC
D SUFFIX
CASE 751A



14–LEAD TSSOP
DT SUFFIX
CASE 948G

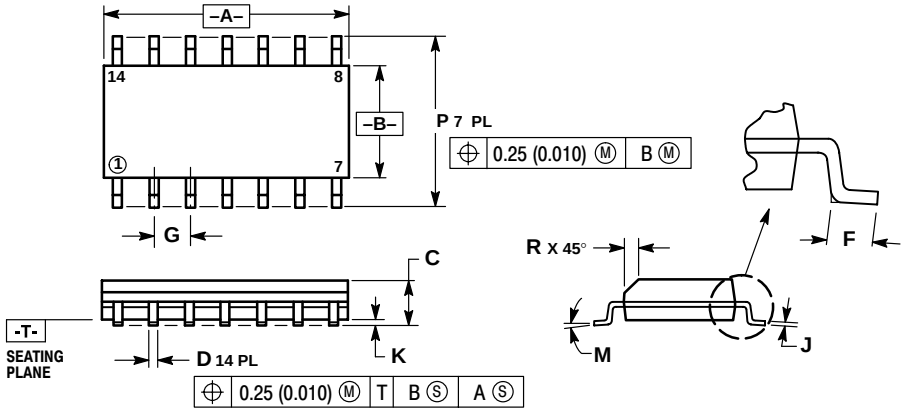


14–LEAD SOIC EIAJ
M SUFFIX
CASE 965

*See Applications Note #AND8004/D for date code and traceability information.

PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F

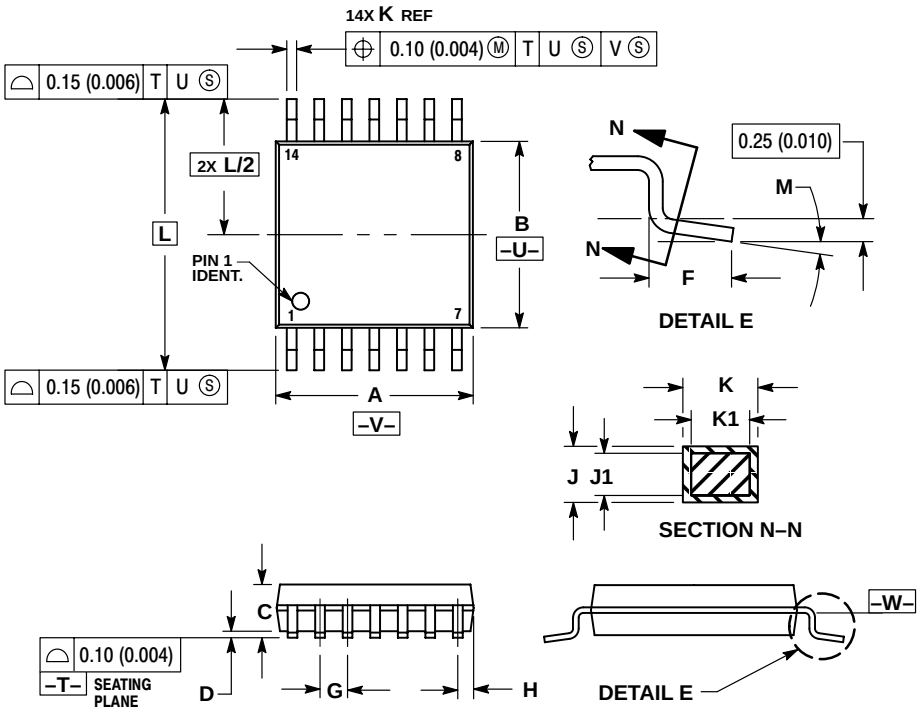


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948G–01
ISSUE O

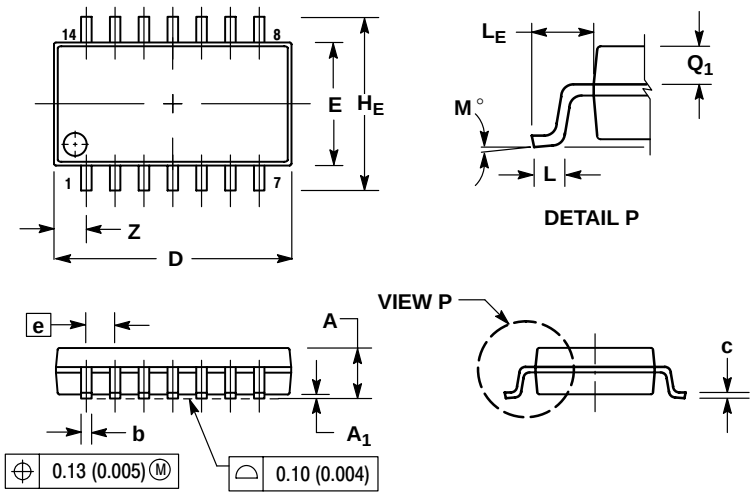


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 965–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303–675–2167 or 800–344–3810 Toll Free USA/Canada

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support
German Phone: (+1) 303–308–7140 (M–F 1:00pm to 5:00pm Munich Time)
Email: ONlit–german@hibbertco.com
French Phone: (+1) 303–308–7141 (M–F 1:00pm to 5:00pm Toulouse Time)
Email: ONlit–french@hibbertco.com
English Phone: (+1) 303–308–7142 (M–F 12:00pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

EUROPEAN TOLL–FREE ACCESS*: 00–800–4422–3781
*Available from Germany, France, Italy, England, Ireland

CENTRAL/SOUTH AMERICA:
Spanish Phone: 303–308–7143 (Mon–Fri 8:00am to 5:00pm MST)
Email: ONlit–spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001–800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–8549
Phone: 81–3–5740–2745
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.