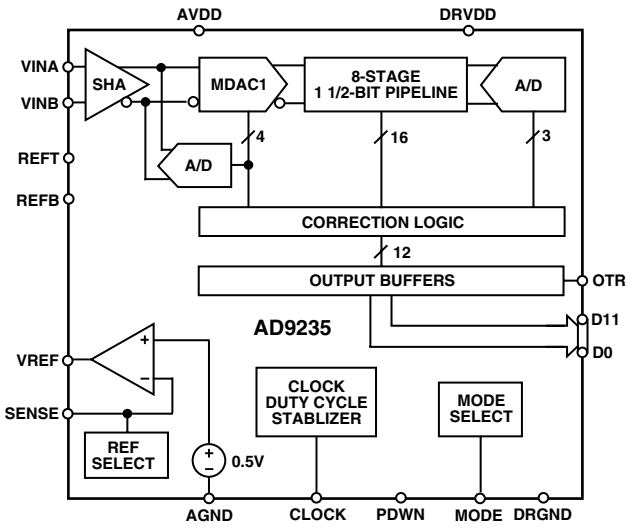
12-Bit, 20/40/65 MSPS 3 V A/D Converter

AD9235

FEATURES
Single 3 V Supply Operation (2.7 V to 3.6 V)
SNR = 70 dBc (to Nyquist)
SFDR = 90 dBc (to Nyquist)
Low Power: 300 mW at 65 MSPS
Differential Input with 500 MHz Bandwidth
On-Chip Reference and SHA
DNL = ±0.4 LSB
Flexible Analog Input: 1 V p-p to 2 V p-p Range
Offset Binary or Two's Complement Data Format
Clock Duty Cycle Stabilizer

APPLICATIONS
Ultrasound Equipment
IF Sampling in Communications Receivers:
IS-95, CDMA-One, IMT-2000
Battery-Powered Instruments
Hand-Held Scopemeters
Low Cost Digital Oscilloscopes

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9235 is a family of monolithic, single 3 V supply, 12-bit, 20/40/65 MSPS analog-to-digital converters. This family features a high performance sample-and-hold amplifier and voltage reference. The AD9235 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 65 MSPS data rates and guarantee no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows for a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available analog-to-digital converters, the AD9235 is suitable for applications in communications, imaging and medical ultrasound.

A single-ended clock input is used to control all internal conversion cycles. A duty cycle stabilizer compensates for wide variations in the cock duty cycle while maintaining excellent performance. The digital output data is presented in straight binary or two's complement formats. An out-of-range signal indicates an overflow condition, which can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9235 is available in a 28-lead surface mount plastic package and is specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

1. The AD9235 operates from a single 3 V power supply, and features a separate digital output driver supply to accommodate 2.5 V and 3.3 V logic families.
2. Operating at 65 MSPS, the AD9235 consumes a low 300 mW.
3. The patented SHA input maintains excellent performance for input frequencies up to 200 MHz, and can be configured for single-ended or differential operation.
4. The AD9235 pinout is similar to the AD9214-65, a 10-bit, 65 MSPS A/D converter. This allows a simplified upgrade path from 10- to 12-bits for 65 MSPS systems.
5. The clock duty cycle stabilizer maintains performance over a wide range of clock pulsewidths.
6. The OTR output bit indicates when the signal is beyond the selected input range.

REV. 0

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AD9235–SPECIFICATIONS

DC SPECIFICATIONS (AVDD = 3 V, DRVDD = 2.5 V, Maximum Sample Rate, 2 V p-p Differential Input, 1.0 V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Temp	Test Level	AD9235BRU-20 Min	AD9235BRU-20 Typ	AD9235BRU-20 Max	AD9235BRU-40 Min	AD9235BRU-40 Typ	AD9235BRU-40 Max	AD9235BRU-65 Min	AD9235BRU-65 Typ	AD9235BRU-65 Max	Unit
RESOLUTION	Full	VI	12			12			12			Bits
ACCURACY												
No Missing Codes Guaranteed	Full	VI	12			12			12			Bits
Offset Error	Full	VI		±0.30	±1.20		±0.50	±1.20		±0.50	±1.20	% FSR
Gain Error[1]	Full	VI		±0.30	±2.40		±0.50	±2.50		±0.50	±2.60	% FSR
Differential Nonlinearity (DNL)[2]	Full	IV		±0.35	±0.65		±0.35	±0.75		±0.40	±0.80	LSB
	25°C	I		±0.35			±0.35			±0.35		LSB
Integral Nonlinearity (INL)[2]	Full	IV		±0.45	±0.80		±0.50	±0.90		±0.70	±1.30	LSB
	25°C	I		±0.40			±0.40			±0.45		LSB
TEMPERATURE DRIFT												
Offset Error	Full	V		±2			±2			±3		ppm/°C
Gain Error[1]	Full	V		±12			±12			±12		ppm/°C
INTERNAL VOLTAGE REFERENCE												
Output Voltage Error (1 V Mode)	Full	VI		±5	±35		±5	±35		±5	±35	mV
Load Regulation @ 1.0 mA	Full	V		0.8			0.8			0.8		mV
Output Voltage Error (0.5 V Mode)	Full	V		±2.5			±2.5			±2.5		mV
Load Regulation @ 0.5 mA	Full	V		0.1			0.1			0.1		mV
INPUT REFERRED NOISE												
VREF = 0.5 V	25°C	V		0.54			0.54			0.54		LSB rms
VREF = 1.0 V	25°C	V		0.27			0.27			0.27		LSB rms
ANALOG INPUT												
Input Span, VREF = 0.5 V	Full	IV		1			1			1		V p-p
Input Span, VREF = 1.0 V	Full	IV		2			2			2		V p-p
Input Capacitance[3]	Full	V		7			7			7		pF
REFERENCE INPUT RESISTANCE	Full	V		7			7			7		kΩ
POWER SUPPLIES												
Supply Voltages												
AVDD	Full	IV	2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	Full	IV	2.25	3.0	3.6	2.25	3.0	3.6	2.25	3.0	3.6	V
Supply Current												
IAVDD[2]	Full	V		30			55			100		mA
IDRVDD[2]	Full	V		2			5			7		mA
PSRR	Full	V		±0.01			±0.01			±0.01		% FSR
POWER CONSUMPTION												
DC Input[4]	Full	V		90			165			300		mW
Sine Wave Input[2]	Full	VI		95	110		180	205		320	350	mW
Standby Power[5]	Full	V		1.0			1.0			1.0		mW

NOTES

[1]Gain error and gain temperature coefficient are based on the A/D converter only (with a fixed 1.0 V external reference).

[2]Measured at maximum clock rate, f_{IN} = 2.4 MHz, full-scale sine wave, with approximately 5 pF loading on each output bit.

[3]Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 2 for the equivalent analog input structure.

[4]Measured with dc input at maximum clock rate.

[5]Standby power is measured with a dc input, the CLOCK pin inactive (i.e., set to AVDD or AGND).

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

Parameter	Temp	Test Level	AD9235BRU-20 Min	AD9235BRU-20 Typ	AD9235BRU-20 Max	AD9235BRU-40 Min	AD9235BRU-40 Typ	AD9235BRU-40 Max	AD9235BRU-65 Min	AD9235BRU-65 Typ	AD9235BRU-65 Max	Unit
LOGIC INPUTS												
High-Level Input Voltage	Full	IV	2.0			2.0			2.0			V
Low-Level Input Voltage	Full	IV			0.8			0.8			0.8	V
High-Level Input Current	Full	IV	–10		+10	–10		+10	–10		+10	µA
Low-Level Input Current	Full	IV	–10		+10	–10		+10	–10		+10	µA
Input Capacitance	Full	V		2			2			2		pF
LOGIC OUTPUTS[1]												
DRVDD = 3.3 V												
High-Level Output Voltage (IOH = 50 mA)	Full	IV	3.29			3.29			3.29			V
High-Level Output Voltage (IOH = 0.5 mA)	Full	IV	3.25			3.25			3.25			V
Low-Level Output Voltage (IOL = 1.6 mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL = 50 mA)	Full	IV			0.05			0.05			0.05	V
DRVDD = 2.5 V												
High-Level Output Voltage (IOH = 50 mA)	Full	IV	2.49			2.49			2.49			V
High-Level Output Voltage (IOH = 0.5 mA)	Full	IV	2.45			2.45			2.45			V
Low-Level Output Voltage (IOL = 1.6 mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL = 50 mA)	Full	IV			0.05			0.05			0.05	V

NOTES
[1]Output Voltage Levels measured with 5 pF load on each output.
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

Parameter	Temp	Test Level	AD9235BRU-20 Min	AD9235BRU-20 Typ	AD9235BRU-20 Max	AD9235BRU-40 Min	AD9235BRU-40 Typ	AD9235BRU-40 Max	AD9235BRU-65 Min	AD9235BRU-65 Typ	AD9235BRU-65 Max	Unit
CLOCK INPUT PARAMETERS												
Max Conversion Rate	Full	VI	20			40			65			MSPS
Min Conversion Rate	Full	V			1			1			1	MSPS
CLOCK Period	Full	V	50.0			25.0			15.4			ns
CLOCK Pulsewidth High[1]	Full	V	15.0			8.8			6.2			ns
CLOCK Pulsewidth Low[1]	Full	V	15.0			8.8			6.2			ns
DATA OUTPUT PARAMETERS												
Output Delay[2] (t_{OD})	Full	V		3.5			3.5			3.5		ns
Pipeline Delay (Latency)	Full	V		7			7			7		Cycles
Aperture Delay	Full	V		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter)	Full	V		0.5			0.5			0.5		ps rms
Wake-Up Time[3]	Full	V		2.5			2.5			2.5		ms
OUT-OF-RANGE RECOVERY TIME	Full	V		1			1			2		Cycles

NOTES
[1]For the AD9235-65 model only, with duty cycle stabilizer enabled. DCS function not applicable for -20 and -40 models.
[2]Output delay is measured from CLOCK 50% transition to DATA 50% transition, with 5 pF load on each output.
[3]Wake-up time is dependant on value of decoupling capacitors, typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.
Specifications subject to change without notice.

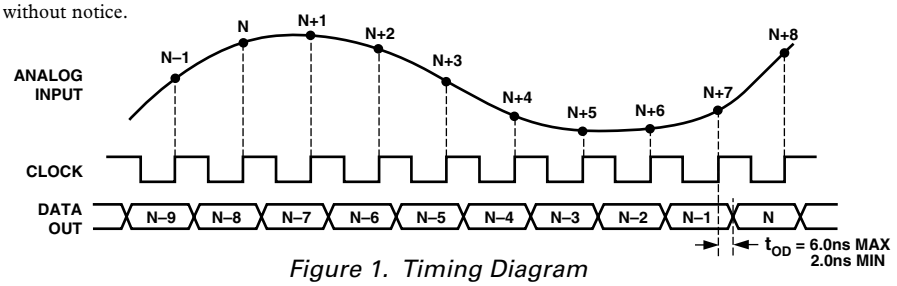


Figure 1. Timing Diagram

AD9235–SPECIFICATIONS

AC SPECIFICATIONS (AVDD = 3 V, DRVDD = 2.5 V, Maximum Sample Rate, 2 V p-p Differential Input, 1.0 V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Temp	Test Level	AD9235BRU-20 Min	AD9235BRU-20 Typ	AD9235BRU-20 Max	AD9235BRU-40 Min	AD9235BRU-40 Typ	AD9235BRU-40 Max	AD9235BRU-65 Min	AD9235BRU-65 Typ	AD9235BRU-65 Max	Unit
SIGNAL-TO-NOISE RATIO												
f_{INPUT} = 2.4 MHz	25°C	V		70.8			70.6			70.5		dBc
f_{INPUT} = 9.7 MHz	Full	IV	70.0	70.4								dBc
	25°C	I		70.6								dBc
f_{INPUT} = 19.6 MHz	Full	IV				69.9	70.3					dBc
	25°C	I					70.4					dBc
f_{INPUT} = 32.5 MHz	Full	IV							68.7	69.7		dBc
	25°C	I								70.1		dBc
f_{INPUT} = 100 MHz	25°C	V		68.7			68.5			68.3		dBc
SIGNAL-TO-NOISE RATIO AND DISTORTION												
f_{INPUT} = 2.4 MHz	25°C	V		70.6			70.5			70.4		dBc
f_{INPUT} = 9.7 MHz	Full	IV	69.9	70.3								dBc
	25°C	I		70.5								dBc
f_{INPUT} = 19.6 MHz	Full	IV				69.7	70.2					dBc
	25°C	I					70.3					dBc
f_{INPUT} = 32.5 MHz	Full	IV							68.3	69.5		dBc
	25°C	I								69.9		dBc
f_{INPUT} = 100 MHz	25°C	V		68.6			68.3			67.8		dBc
TOTAL HARMONIC DISTORTION												
f_{INPUT} = 2.4 MHz	25°C	V		–88.0			–89.0			–87.5		dBc
f_{INPUT} = 9.7 MHz	Full	IV		–86.0	–79.0							dBc
	25°C	I		–87.4								dBc
f_{INPUT} = 19.6 MHz	Full	IV					–85.5	–79.0				dBc
	25°C	I					–86.0					dBc
f_{INPUT} = 32.5 MHz	Full	IV								–81.8	–74.0	dBc
	25°C	I								–82.0		dBc
f_{INPUT} = 100 MHz	25°C	V		–84.0			–82.5			–78.0		dBc
WORST HARMONIC (Second or Third)												
f_{INPUT} = 9.7 MHz	Full	IV		–90.0	–80.0							dBc
f_{INPUT} = 19.6 MHz	Full	IV					–90.0	–80.0				dBc
f_{INPUT} = 32.5 MHz	Full	IV								–83.5	–74.0	dBc
SPURIOUS FREE DYNAMIC RANGE												
f_{INPUT} = 2.4 MHz	25°C	V		92.0			92.0			92.0		dBc
f_{INPUT} = 9.7 MHz	Full	IV	80.0	88.5								dBc
	25°C	I		91.0								dBc
f_{INPUT} = 19.6 MHz	Full	IV				80.0	89.0					dBc
	25°C	I					90.0					dBc
f_{INPUT} = 32.5 MHz	Full	IV							74.0	83.0		dBc
	25°C	I								85.0		dBc
f_{INPUT} = 100 MHz	25°C	V		84.0			85.0			80.5		dBc

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Pin Name	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	–0.3	+3.9	V
DRVDD	DRGND	–0.3	+3.9	V
AGND	DRGND	–0.3	+0.3	V
AVDD	DRVDD	–3.9	+3.9	V
Digital Outputs	DRGND	–0.3	DRVDD + 0.3	V
CLOCK, MODE	AGND	–0.3	AVDD + 0.3	V
VINA, VINB	AGND	–0.3	AVDD + 0.3	V
VREF	AGND	–0.3	AVDD + 0.3	V
SENSE	AGND	–0.3	AVDD + 0.3	V
REFB, REFT	AGND	–0.3	AVDD + 0.3	V
PDWN	AGND	–0.3	AVDD + 0.3	V
ENVIRONMENTAL[2]				
Operating Temperature		–40	+85	°C
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C
Storage Temperature		–65	+150	°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances (28-lead TSSOP); θ_{JA} = 97.9°C/W; θ_{JC} = 14°C/W. These measurements were taken on a 2-layer board in still air, in accordance with EIA/JESD51-3.

EXPLANATION OF TEST LEVELS

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

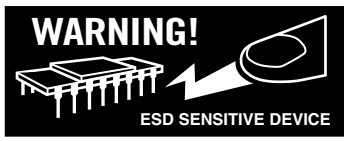
VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9235BRU-20	–40°C to +85°C	28-Lead Thin Shrink Small Outline (TSSOP)	RU-28
AD9235BRU-40	–40°C to +85°C	28-Lead Thin Shrink Small Outline (TSSOP)	RU-28
AD9235BRU-65	–40°C to +85°C	28-Lead Thin Shrink Small Outline (TSSOP)	RU-28
AD9235-20PCB		Evaluation Board	
AD9235-40PCB		Evaluation Board	
AD9235-65PCB		Evaluation Board	

CAUTION

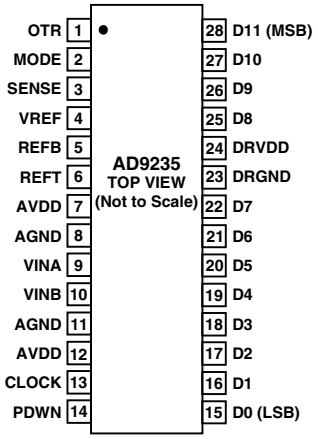
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9235 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	OTR	Out-of-Range Indicator.
2	MODE	Data Format and Clock Duty Cycle Stabilizer (DCS) Mode selection.
3	SENSE	Reference Mode Selection.
4	VREF	Voltage Reference Input/Output.
5	REFB	Differential Reference (Negative).
6	REFT	Differential Reference (Positive).
7, 12	AVDD	Analog Power Supply.
8, 11	AGND	Analog Ground.
9	VINA	Analog Input Pin (+).
10	VINB	Analog Input Pin (–).
13	CLOCK	Clock Input Pin.
14	PDWN	Power-Down Function Selection (Active High).
15–22, 25–28	D0 (LSB)–D11 (MSB)	Data Output Bits.
23	DRGND	Digital Output Ground.
24	DRVDD	Digital Output Driver Supply. Must be decoupled to DRGND with a minimum 0.1 µF capacitor. Recommended decoupling is 0.1 µF in parallel with 10 µF.

PIN CONFIGURATION



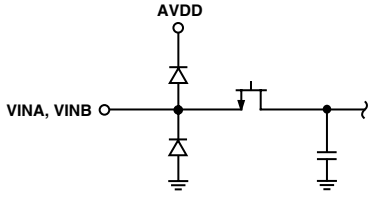


Figure 2. Equivalent Analog Input Circuit

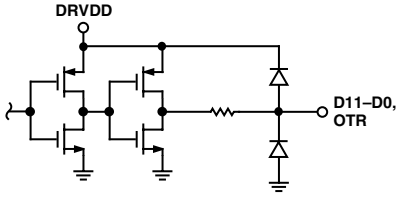


Figure 4. Equivalent Digital Output Circuit

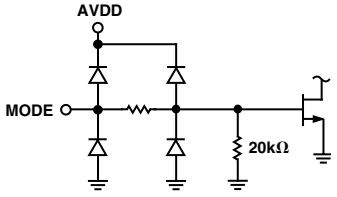


Figure 3. Equivalent MODE Input Circuit

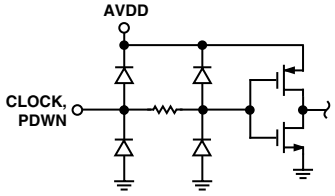


Figure 5. Equivalent Digital Input Circuit

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal A/D converter exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

OFFSET ERROR

The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and can be manifested as noise on the input to the A/D converter.

APERTURE DELAY

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to obtain a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

CLOCK PULSEWIDTH AND DUTY CYCLE

Pulsewidth high is the minimum amount of time that the clock pulse should be left in the logic "1" state to achieve rated performance: pulsewidth low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

MINIMUM CONVERSION RATE

The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

MAXIMUM CONVERSION RATE

The clock rate at which parametric testing is performed.

OUTPUT PROPAGATION DELAY

The delay between the clock logic threshold and the time when all bits are within valid logic levels.

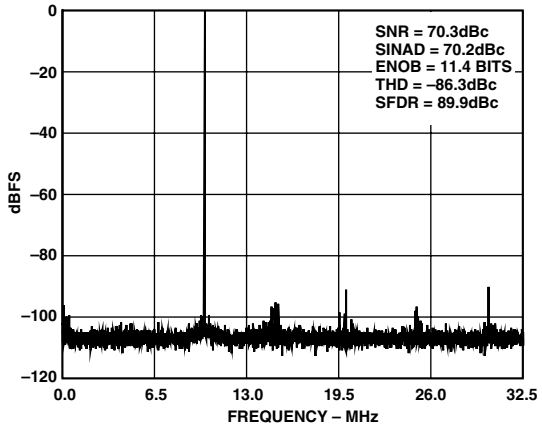
TWO-TONE SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

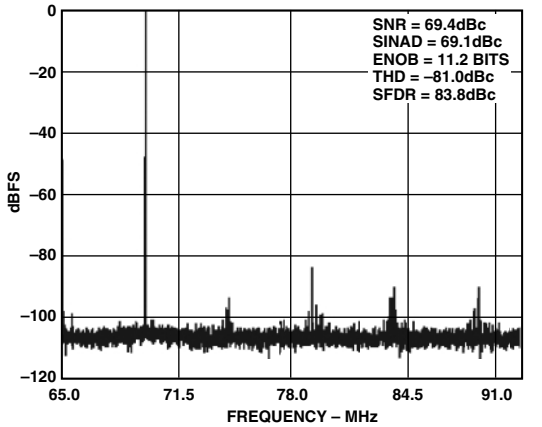
OUT-OF-RANGE RECOVERY TIME

Out-of-range recovery time is the time it takes for the A/D converter to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

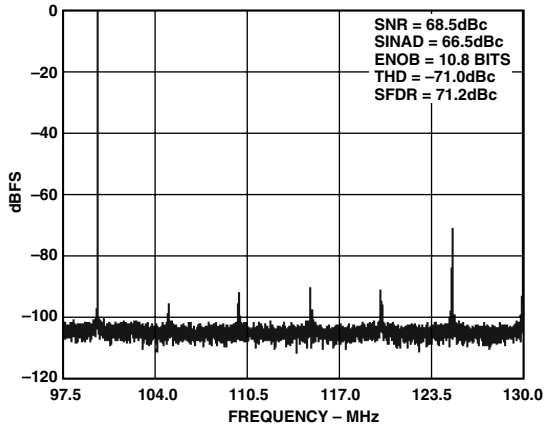
AD9235–Typical Performance Characteristics (AVDD = 3.0 V, DRVDD = 2.5 V, f_{SAMPLE} = 65 MSPS with DCS Enabled, T_A = 25°C, 2 V Differential Input, A_{IN} = –0.5 dBFS, VREF = 1.0 V unless otherwise noted.)



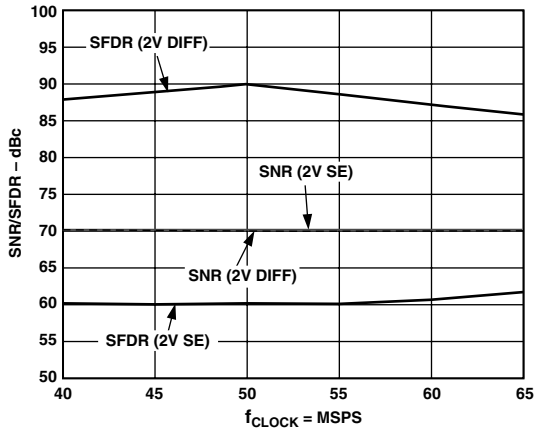
TPC 1. Single Tone 8K FFT with f_{IN} = 10 MHz



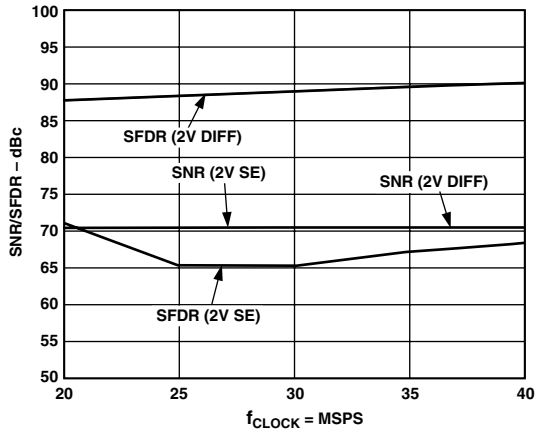
TPC 2. Single Tone 8K FFT with f_{IN} = 70 MHz



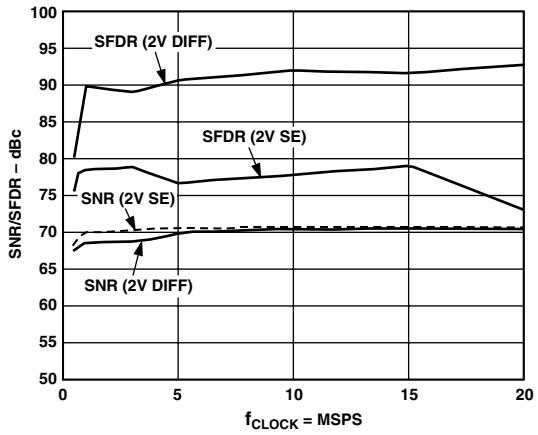
TPC 3. Single Tone 8K FFT with f_{IN} = 100 MHz



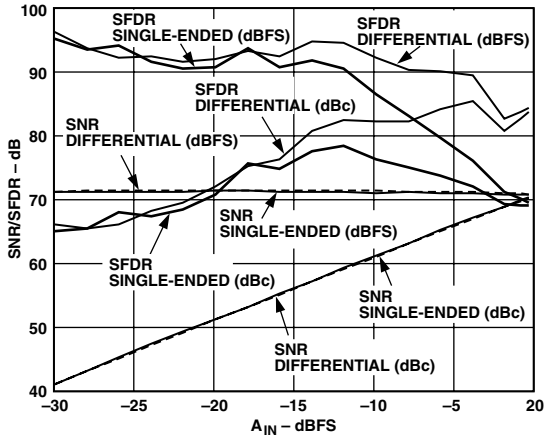
TPC 4. AD9235-65: Single Tone SNR/SFDR vs. f_{CLOCK} with f_{IN} = Nyquist (32.5 MHz)



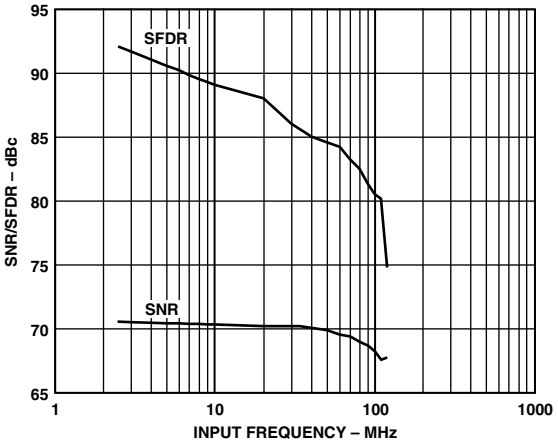
TPC 5. AD9235-40: Single Tone SNR/SFDR vs. f_{CLOCK} with f_{IN} = Nyquist (20 MHz)



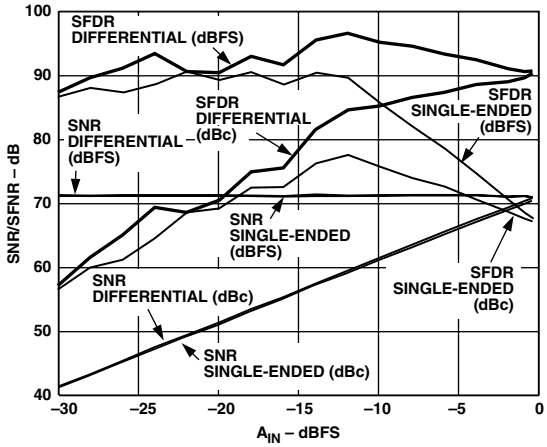
TPC 6. AD9235-20: Single Tone SNR/SFDR vs. f_{CLOCK} with f_{IN} = Nyquist (10 MHz)



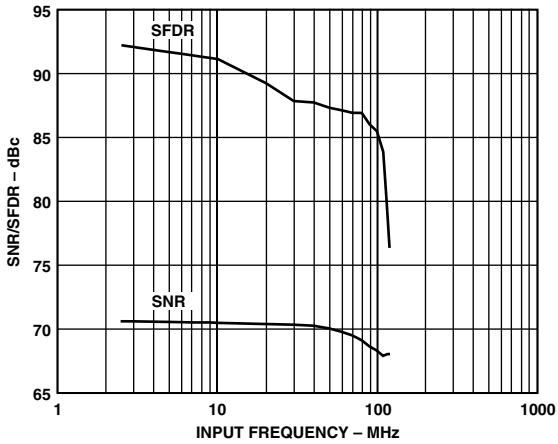
TPC 7. AD9235-65: Single Tone SNR/SFDR vs. A_{IN} with f_{IN} = Nyquist (32.5 MHz)



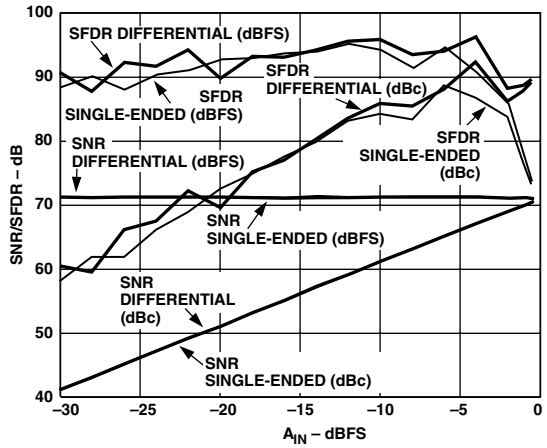
TPC 10. AD9235-65: SNR/SFDR vs. Frequency



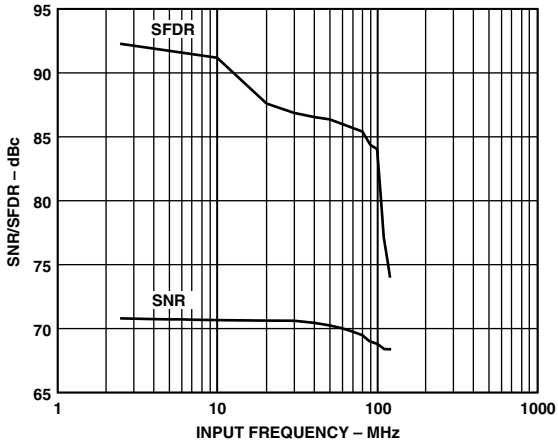
TPC 8. AD9235-40: Single Tone SNR/SFDR vs. A_{IN} with f_{IN} = Nyquist (20 MHz)



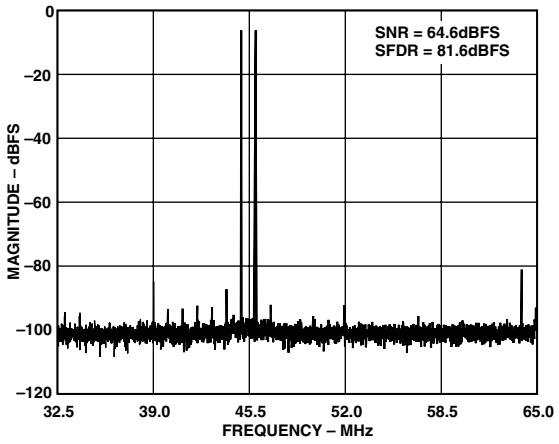
TPC 11. AD9235-40: SNR/SFDR vs. Frequency



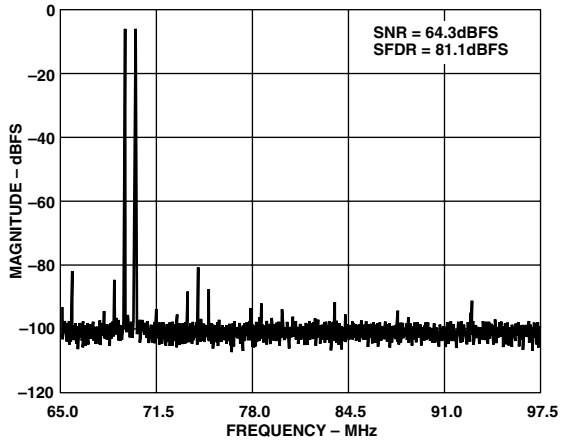
TPC 9. AD9235-20: Single Tone SNR/SFDR vs. A_{IN} with f_{IN} = Nyquist (10 MHz)



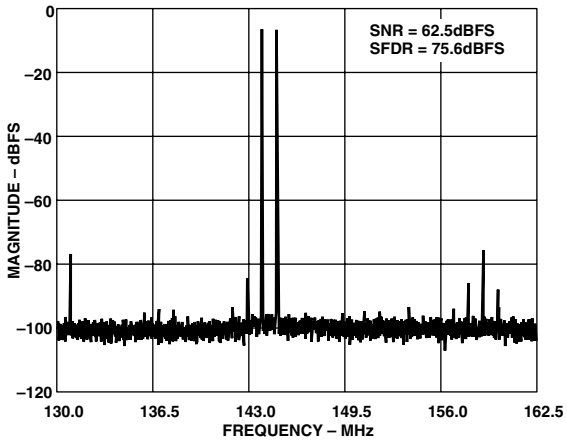
TPC 12. AD9235-20: SNR/SFDR vs. Frequency



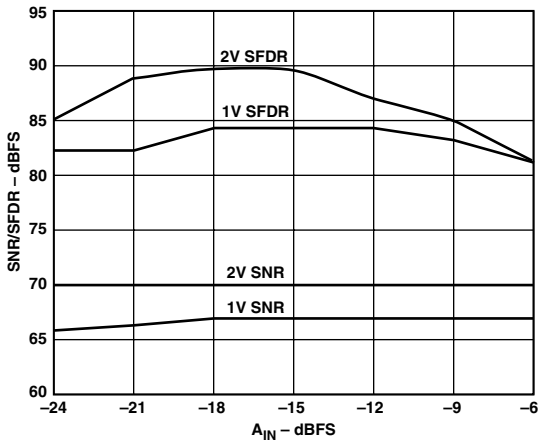
TPC 13. Dual Tone 8K FFT with f_{IN1} = 45 MHz and f_{IN2} = 46 MHz



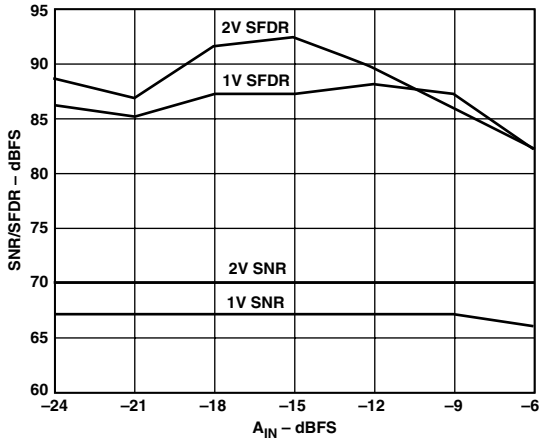
TPC 14. Dual Tone 8K FFT with f_{IN1} = 69 MHz and f_{IN2} = 70 MHz



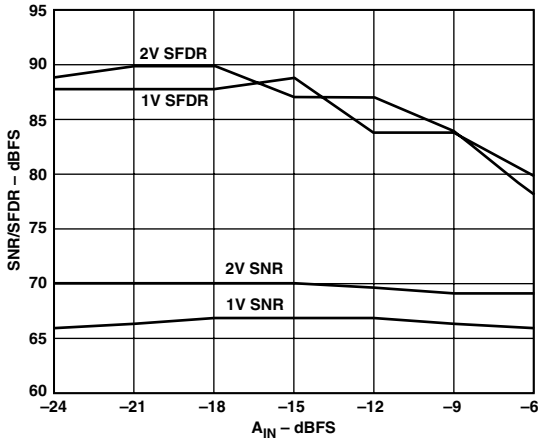
TPC 15. Dual Tone 8K FFT with f_{IN1} = 144 MHz and f_{IN2} = 145 MHz



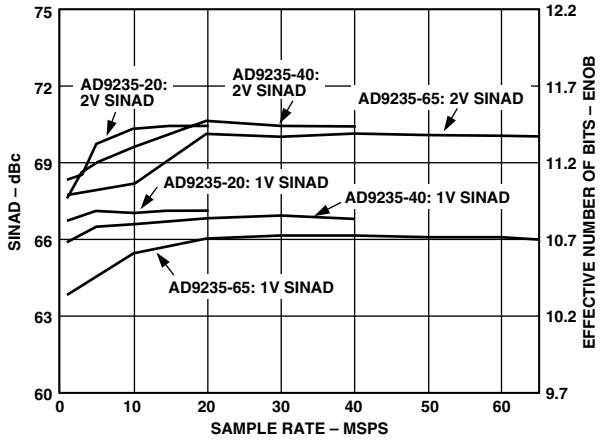
TPC 16. Dual Tone SNR/SFDR vs. A_{IN} with f_{IN1} = 45 MHz and f_{IN2} = 46 MHz



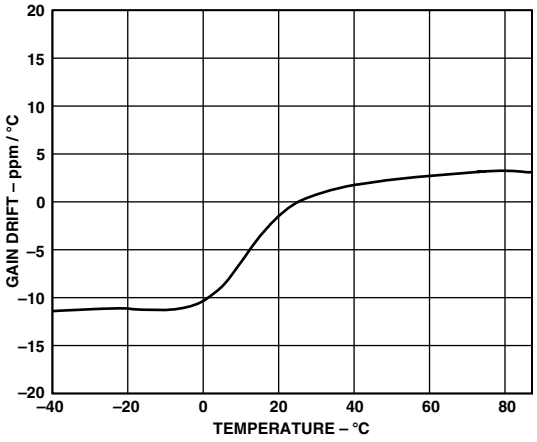
TPC 17. Dual Tone SNR/SFDR vs. A_{IN} with f_{IN1} = 69 MHz and f_{IN2} = 70 MHz



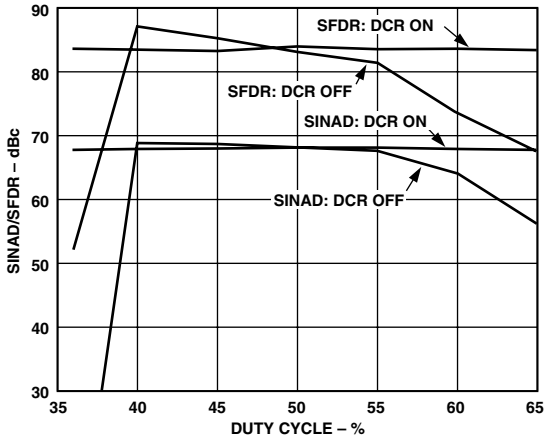
TPC 18. Dual Tone SNR/SFDR vs. A_{IN} with f_{IN1} = 144 MHz and f_{IN2} = 145 MHz



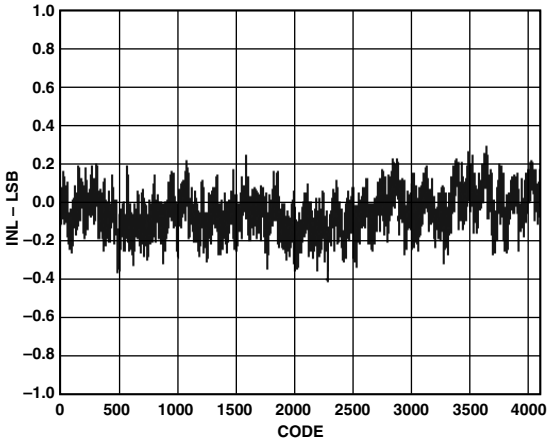
TPC 19. SINAD vs. f_{CLOCK} with f_{IN} = Nyquist



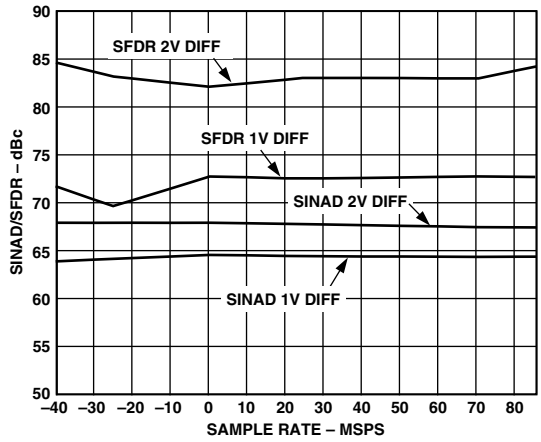
TPC 22. A/D Gain vs. Temperature using an External Reference



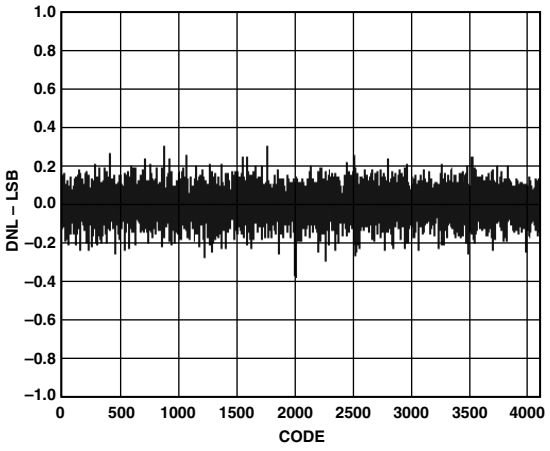
TPC 20. SINAD/SFDR vs. Clock Duty Cycle



TPC 23. Typical INL



TPC 21. SINAD/SFDR vs. Temperature with f_{IN} = 32.5 MHz



TPC 24. Typical DNL

APPLYING THE AD9235

THEORY OF OPERATION

The AD9235 architecture consists of a front-end Sample and Hold Amplifier (SHA) followed by a pipelined switched capacitor A/D converter. The pipelined A/D converter is divided into three sections, consisting of a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash A/D connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D.

The input stage contains a differential SHA that can be configured as ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction and passes the data to the output buffers. The output buffers are powered from a separate supply allowing adjustment of the output voltage swing. During power-down the output buffers go into a high impedance state.

ANALOG INPUT

The analog input to the AD9235 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal. The SHA input can support a wide common-mode range and maintain excellent performance, as shown in Figure 7. An input common-mode voltage of midsupply will minimize signal-dependant errors and provide optimum performance.

Referring to Figure 6, the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network will create a low-pass filter at the A/D's input; therefore, the precise values are dependant upon the application. In IF undersampling applications, any shunt capacitors should be removed. In combination with the driving source impedance they would limit the input bandwidth.

For best dynamic performance, the source impedances driving VINA and VINB should be matched such that common-mode settling errors are symmetrical. These errors will be reduced by the common-mode rejection of the A/D.

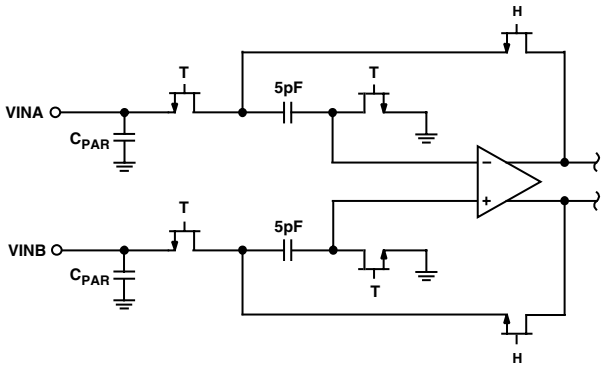


Figure 6. Switched-Capacitor SHA Input

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, respectively, that define the span of the A/D core. The output common mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as follows:

$$REFT = 1/2\ (AVDD + VREF),$$
$$REFB = 1/2\ (AVDD - VREF),$$
$$Span = 2 \times (REFT - REFB) = 2 \times VREF.$$

It can be seen from the equations above that the *REFT* and *REFB* voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

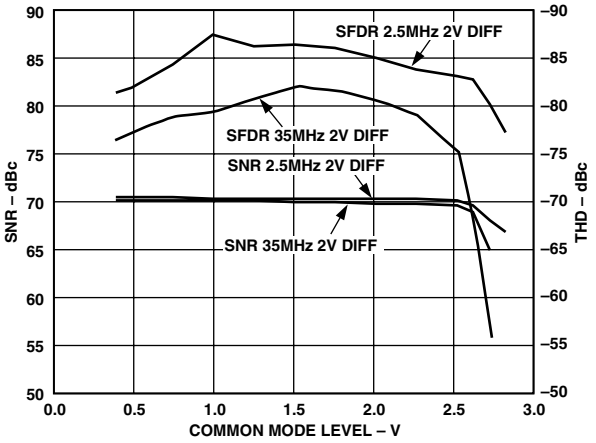


Figure 7. AD9235-65: SNR, THD vs. Common-Mode Level

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V, or adjusted within the same range as discussed in the Internal Reference Connection section. Maximum SNR performance will be achieved with the AD9235 set to the largest input span of 2 V p-p. The relative SNR degradation will be 3 dB when changing from 2 V p-p mode to 1 V p-p mode.

The SHA may be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as follows:

$$VCM_{MIN} = VREF/2,$$

$$VCM_{MAX} = (AVDD + VREF)/2.$$

The minimum common-mode input level allows the AD9235 to accommodate ground-referenced inputs.

Although optimum performance is achieved with a differential input, a single-ended source may be driven into VINA or VINB. In this configuration, one input will accept the signal, while the opposite input should be set to midscale by connecting it to an appropriate reference. For example, a 2 V p-p signal may be applied to VINA while a 1 V reference is applied to VINB. The AD9235 will then accept a signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance may degrade significantly as compared to the differential case. However, the effect will be less noticeable at lower input frequencies and in the lower speed grade models (AD9235-40 and AD9235-20).

DIFFERENTIAL INPUT CONFIGURATIONS

As previously detailed, optimum performance will be achieved while driving the AD9235 in a differential input configuration. For baseband applications, the AD8138 Differential Driver provides excellent performance and a flexible interface to the A/D converter. The output common-mode voltage of the AD8138 is easily set to AVDD/2, and the driver can be configured in a Sallen Key filter topology to provide band limiting of the input signal.

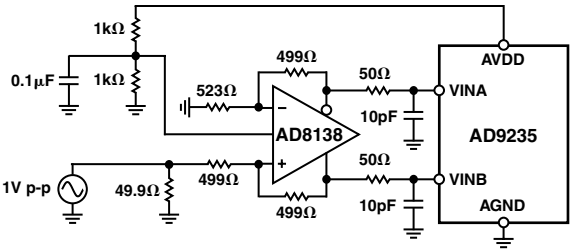


Figure 8. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers will not be adequate to achieve the true performance of the AD9235. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 200 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration, as shown in Figure 9.

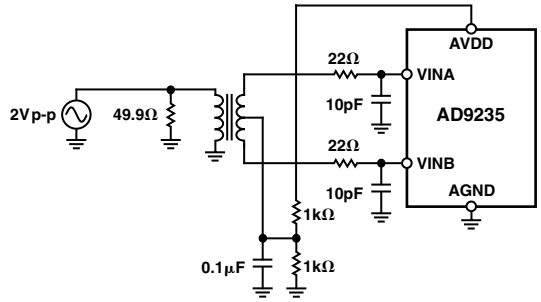


Figure 9. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers will saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

SINGLE-ENDED INPUT CONFIGURATION

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration there will be a degradation in SFDR and distortion performance due to the large input common-mode swing. However, if the source impedances on each input are kept matched, there should be little effect on SNR performance. Figure 10 details a typical single-ended input configuration.

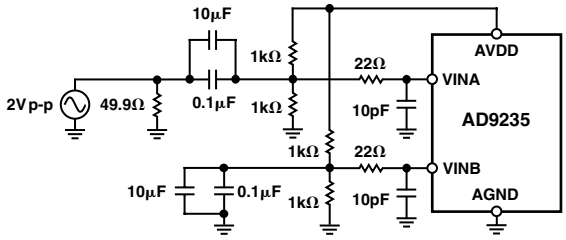


Figure 10. Single-Ended Input Configuration

CLOCK INPUT AND CONSIDERATIONS

Typical high-speed A/D converters use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Commonly a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9235 contains a clock duty cycle stabilizer that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9235. As shown in TPC 20, noise and distortion performance are nearly flat over a 30% range of duty cycle.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency will require approximately 100 clock cycles to allow the DLL to acquire and lock to the new rate.

High-speed, high-resolution A/Ds are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_A) can be calculated with the following equation:

$$SNR\ degradation = 20 \times \log10\ [1/2 \times \pi \times f_{INPUT} \times t_A]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum square of all jitter sources, which include the clock input, analog input signal, and A/D aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9235. Power supplies for clock drivers should be separated from the A/D output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Table I. Reference SENSE Operation

SENSE Voltage	Internal Switch Position	Selected Mode	Resulting VREF (V)	Resulting Differential Span (V p-p)
AVDD	N/A	External Reference	N/A	2 × External Reference
VREF	SENSE	Internal Fixed Reference	0.5	1.0
0.2 V to VREF	SENSE	Programmable Reference	0.5 × (1 + R2/R1)	2 × VREF (See Figure 13)
AGND to 0.2 V	Internal Divider	Internal Fixed Reference	1.0	2.0

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 11, the power dissipated by the AD9235 is proportional to its sample rate. The digital power dissipation does not vary substantially between the three speed grades, because it is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLOCK} \times N$$

where N is the number of output bits, 12 in the case of the AD9235. This maximum current is for the condition of every output bit switching on every clock cycle, which can only occur for a full scale square wave at the Nyquist frequency, f_{CLOCK} /2. In practice, the DRVDD current will be established by the average number of output bits switching, which will be determined by the encode rate and the characteristics of the analog input signal.

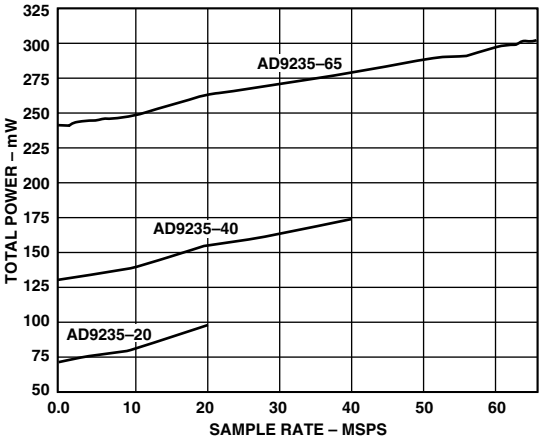


Figure 11. Total Power vs. Sample Rate with f_{IN} = 10 MHz

For the AD9235-20 speed grade, the digital power consumption can represent as much as 10% of the total dissipation. Digital power consumption can be minimized by reducing the capacitive load presented to the output drivers. The data in Figure 11 was taken with a 5 pF load on each output driver.

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increases linearly with the clock frequency.

By asserting the PDWN pin high, the AD9235 is placed in standby mode. In this state the A/D will typically dissipate 1 mW if the CLOCK and analog inputs are static. During standby the output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9235 into its normal operational mode.

Low power dissipation in standby mode is achieved by shutting down the reference, reference buffer and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering standby mode, and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in standby mode, and shorter standby cycles will result in proportionally shorter wake-up times. With the recommended 0.1 µF and 10 µF decoupling capacitors on REFT and REFB, it takes approximately one second to fully discharge the reference buffer decoupling capacitors, and 5 ms to restore full operation.

DIGITAL OUTPUTS

The AD9235 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

As detailed in Table II, the data format can be selected for either offset binary or two's complement.

TIMING

The AD9235 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{OD}) after the rising edge of the clock signal. Refer to Figure 1 for a detailed timing diagram.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9235; these transients can detract from the converter's dynamic performance.

The lowest typical conversion rate of the AD9235 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance may degrade.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9235. The input range can be adjusted by varying the reference voltage applied to the AD9235, using either the internal reference or an externally applied reference voltage. The input span of the A/D tracks reference voltage changes linearly.

If the A/D is being driven differentially through a transformer, the reference voltage can be used to bias the center tap (common-mode voltage).

INTERNAL REFERENCE CONNECTION

A comparator within the AD9235 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table I. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 12), setting VREF to 1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected as shown in Figure 13, the switch will again be set to the SENSE pin. This will put the reference amplifier in a noninverting mode with the VREF output defined as follows:

$$VREF = 0.5 \times (1 + R2/R1)$$

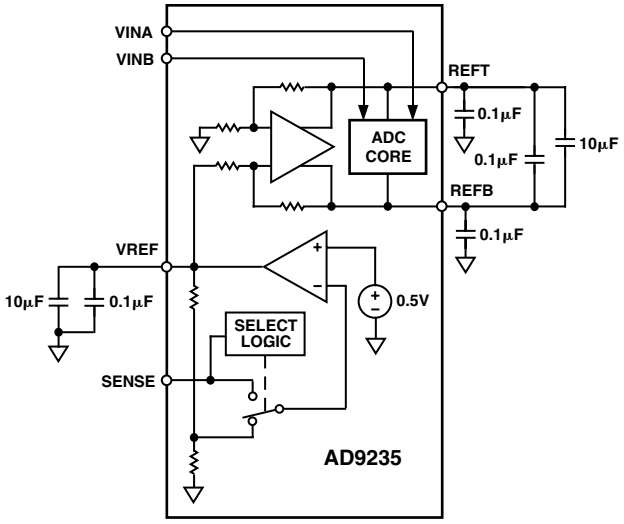


Figure 12. Internal Reference Configuration

In all reference configurations, REFT and REFB drive the A/D conversion core and establish its input span. The input range of the A/D always equals twice the voltage at the reference pin for either an internal or an external reference.

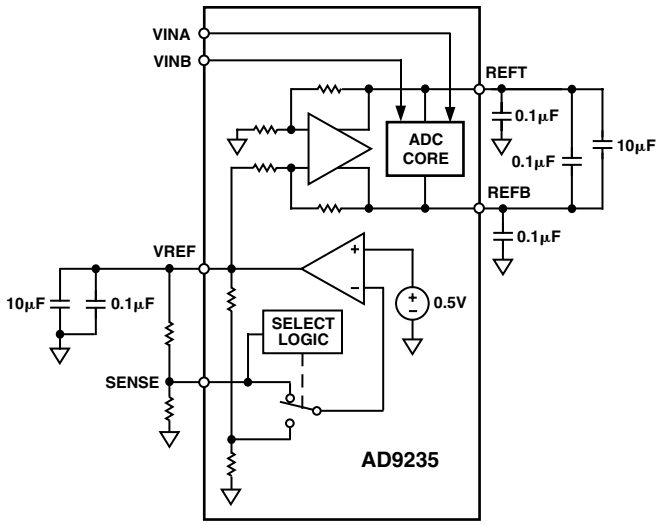


Figure 13. Programmable Reference Configuration

EXTERNAL REFERENCE OPERATION

The use of an external reference may be necessary to enhance the gain accuracy of the A/D or improve thermal drift characteristics. When multiple A/Ds track one another, a single reference (internal or external) may be necessary to reduce gain matching errors to an acceptable level. A high precision external reference may also be selected to provide lower gain and offset temperature drift. Figure 14 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes.

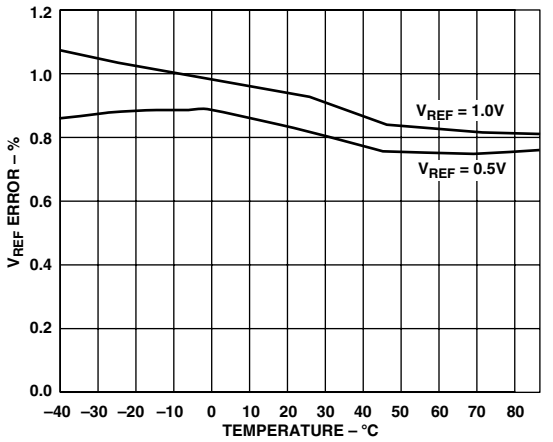


Figure 14. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference will be disabled, allowing the use of an external reference. An internal reference buffer will load the external reference with an equivalent 7 kΩ load. The internal buffer will still generate the positive and negative full-scale references, REFT and REFB, for the A/D core. The input span will always be twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V.

If the internal reference of the AD9235 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 15 depicts how the internal reference voltage is affected by loading.

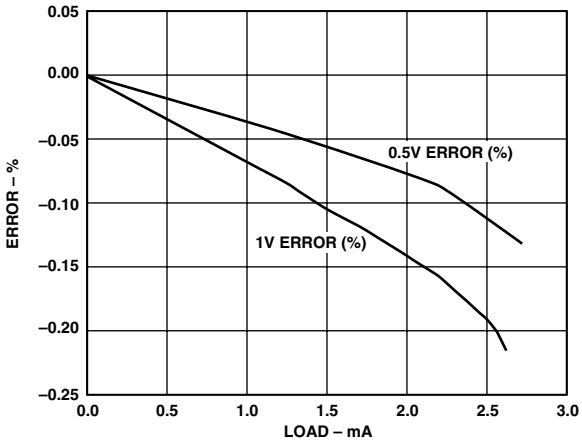


Figure 15. VREF Accuracy vs. Load

OPERATIONAL MODE SELECTION

As discussed earlier, the AD9235 can output data in either offset binary or two's complement format. There is also a provision for enabling or disabling the Clock Duty Cycle Stabilizer (DCS). The MODE pin is a multilevel input that controls the data format and DCS state. The input threshold values and corresponding mode selections are outlined below.

Table II. Mode Selection

MODE Voltage	Data Format	Duty Cycle Stabilizer
AVDD	Two's Complement	Disabled
2/3 AVDD	Two's Complement	Enabled
1/3 AVDD	Offset Binary	Enabled
AGND (Default)	Offset Binary	Disabled

The MODE pin is internally pulled down to AGND by a 20 kΩ resistor.

EVALUATION BOARD

The AD9235 evaluation board provides all of the support circuitry required to operate the A/D in its various modes and configurations. The converter can be driven differentially, through an AD8138 driver or a transformer, or single-ended. Separate power pins are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (refer to the schematics). Figure 16 shows the typical bench characterization setup used to evaluate the ac performance of the AD9235. It is critical that signal sources with very low phase noise (< 1 picosecond rms jitter) be used to realize the ultimate performance of the converter. Proper filtering of the input signal, to remove harmonics and lower the integrated noise at the input, is also necessary to achieve the specified noise performance.

The AUXCLK input should be selected in applications requiring the lowest jitter and SNR performance (i.e., IF undersampling characterization). It allows the user to apply a clock input signal that is 4× the target sample rate of the AD9235. A low-jitter, differential divide-by-4 counter, the MC100LVEL33D, provides a 1× clock output that is subsequently returned back to the CLOCK input via JP9. For example, a 260 MHz signal (sinusoid) will be divided down to a 65 MHz signal for clocking the A/D. Note, R1 must be removed with the AUXCLK interface. Lower jitter is often achieved with this interface since many RF signal generators display improved phase noise at higher output frequencies and the slew rate of the sinusoidal output signal is 4× that of a 1× signal of equal amplitude.

Complete schematics and layout plots follow, which demonstrate the proper routing and grounding techniques that should be applied at the system level.

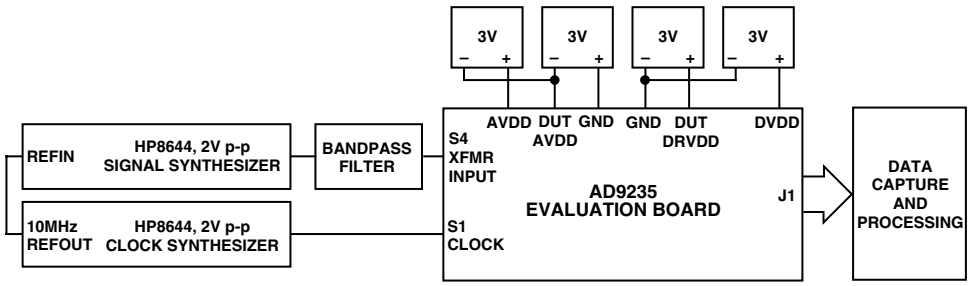


Figure 16. Evaluation Board Connections

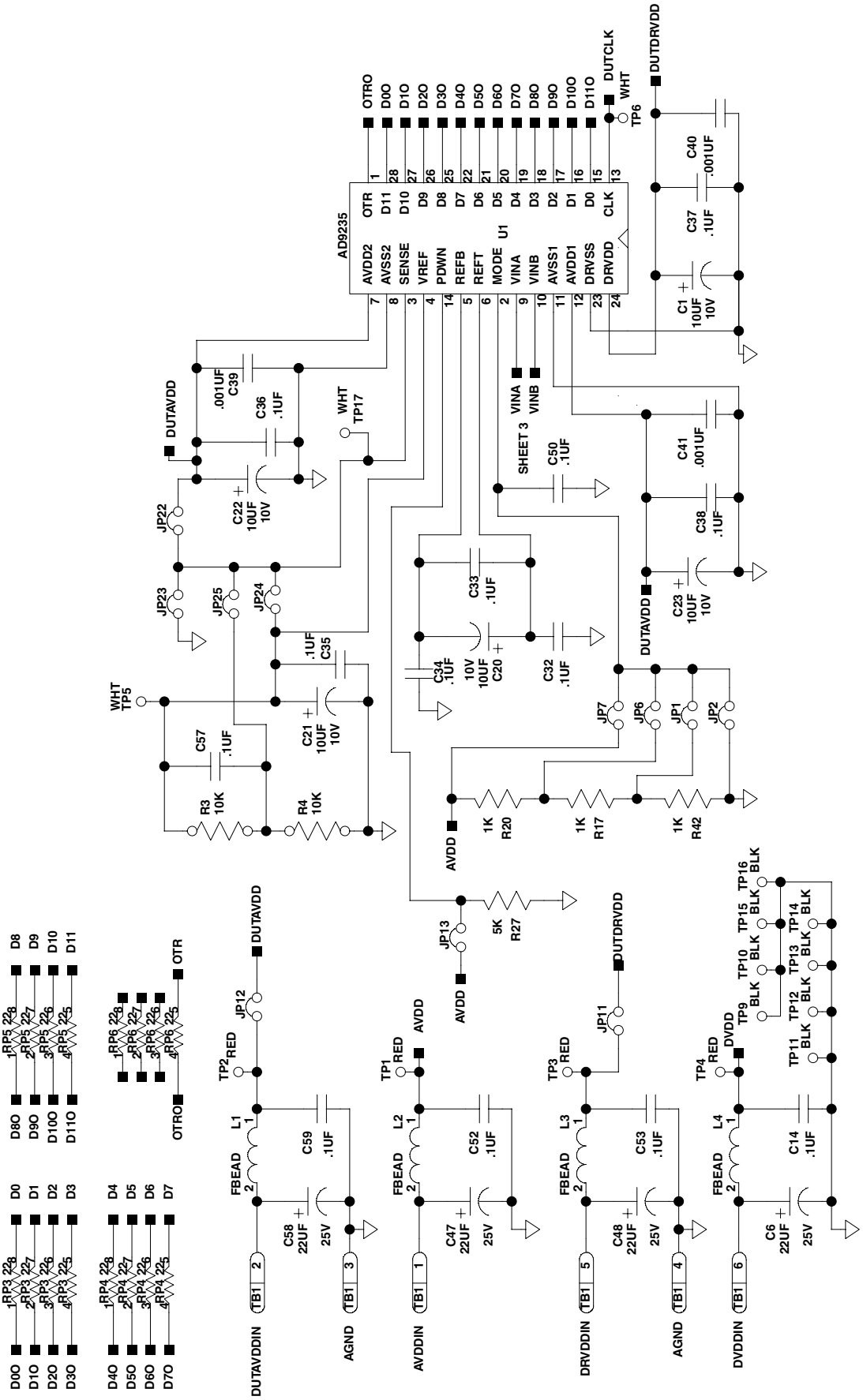


Figure 17. Evaluation Board Schematic, DUT

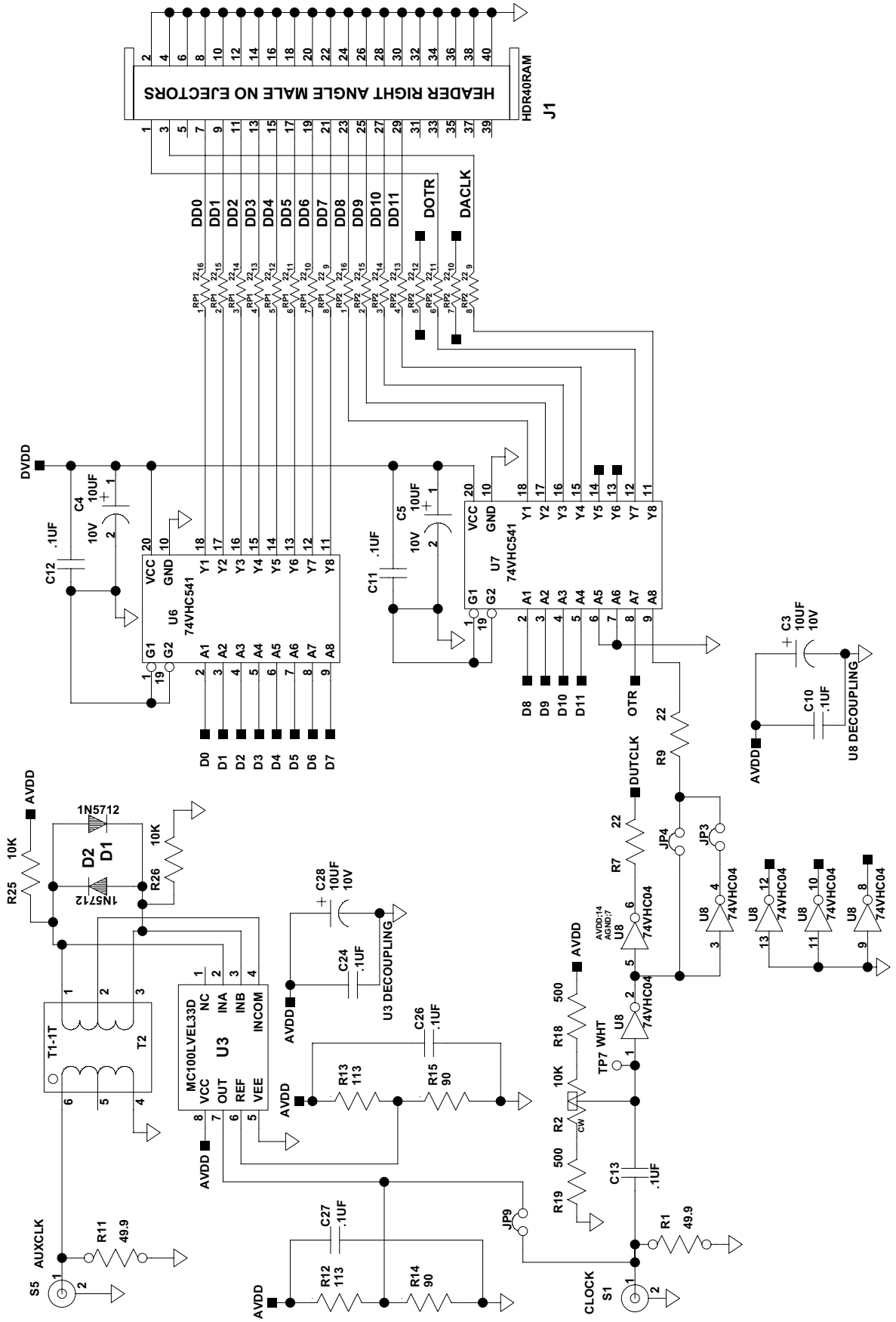


Figure 18. Evaluation Board Schematic, Clock Inputs and Output Buffering

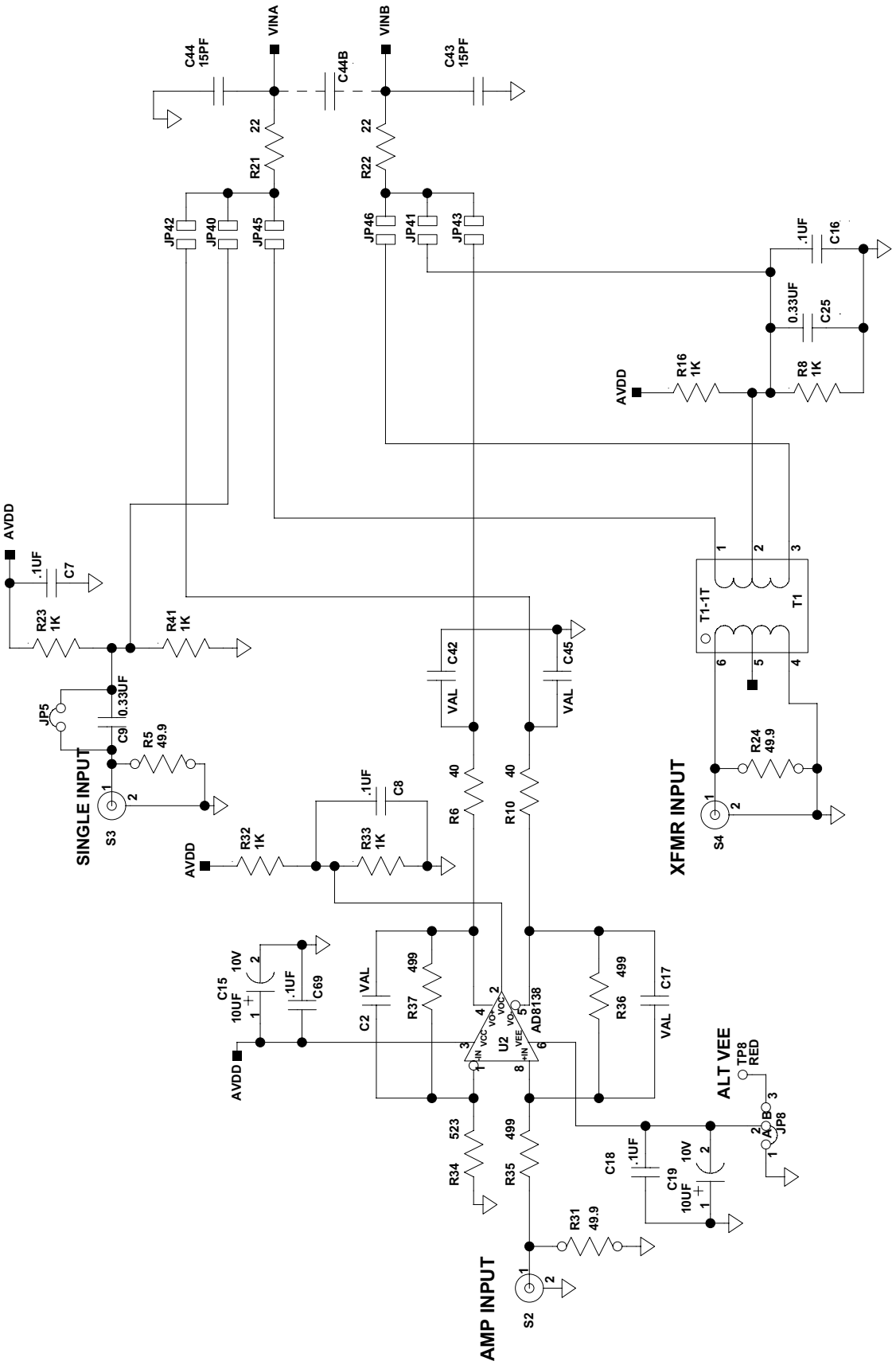


Figure 19. Evaluation Board Schematic, Analog Inputs

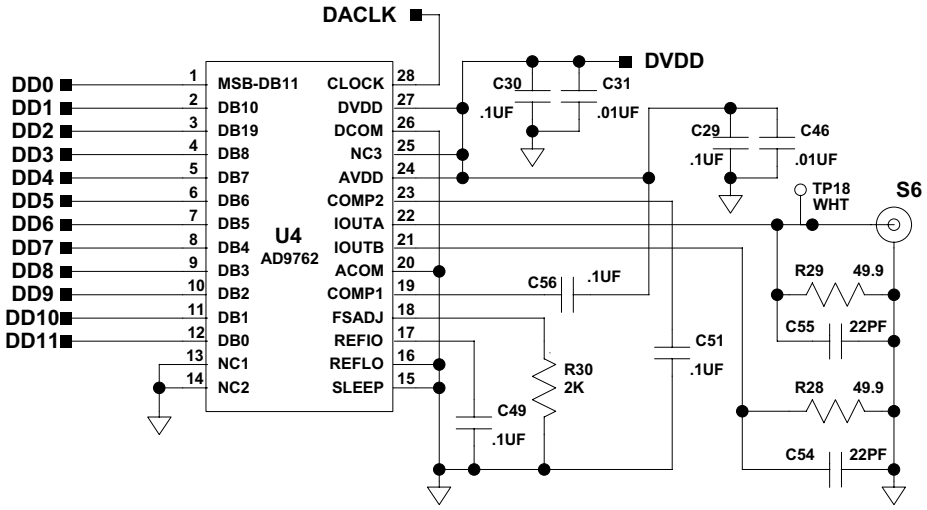


Figure 20. Evaluation Board Schematic, Optional D/A Converter

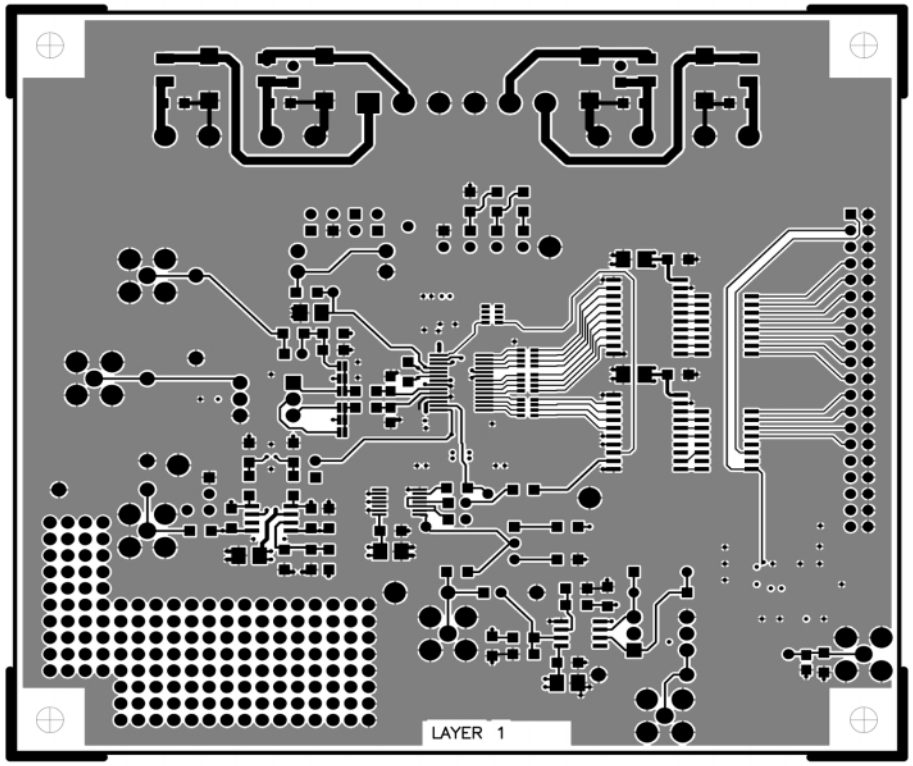


Figure 21. Evaluation Board Layout, Primary Side

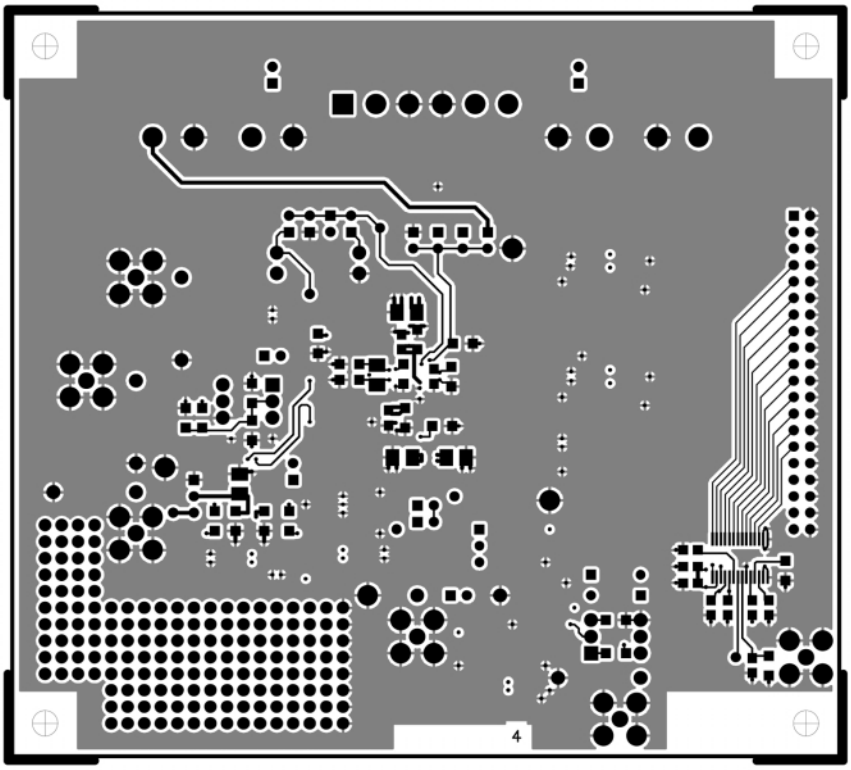


Figure 22. Evaluation Board Layout, Secondary Side

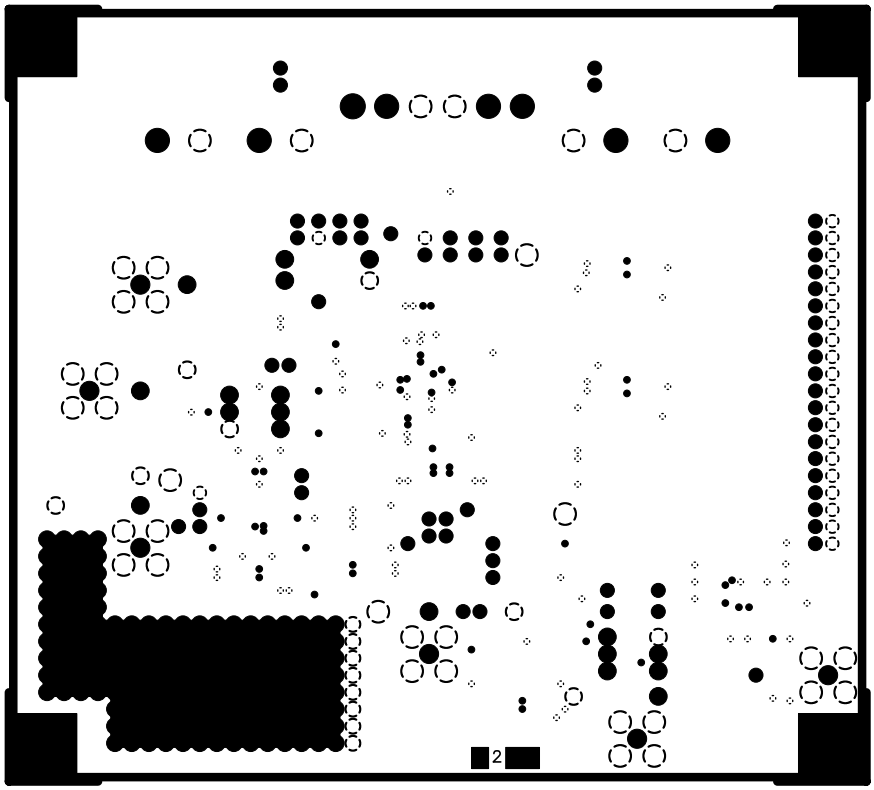


Figure 23. Evaluation Board Layout, Ground Plane

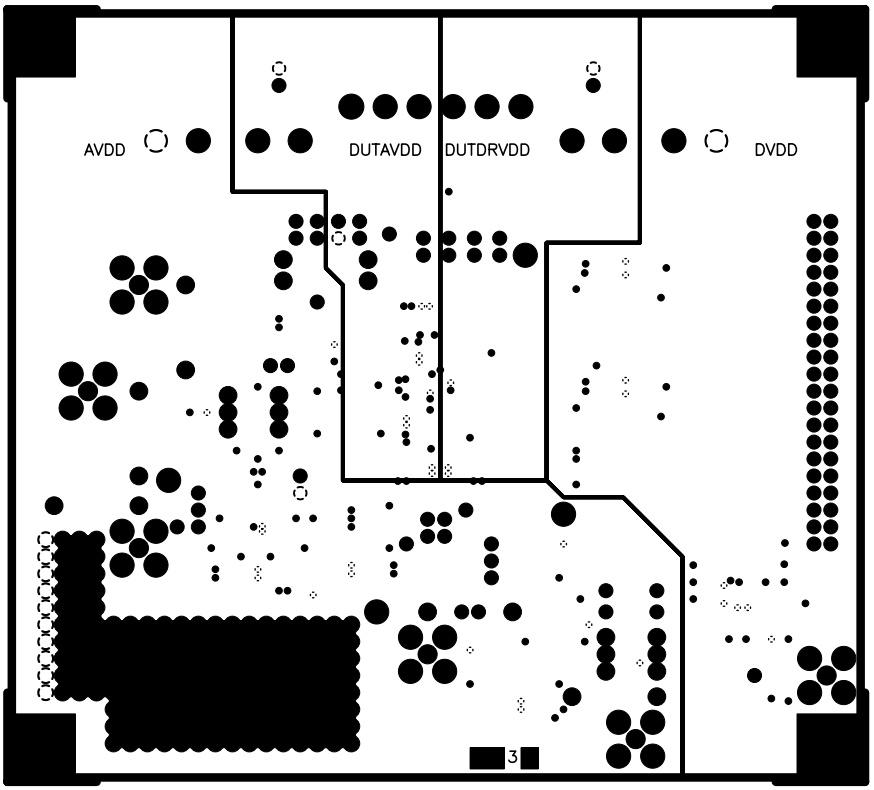


Figure 24. Evaluation Board Power Plane

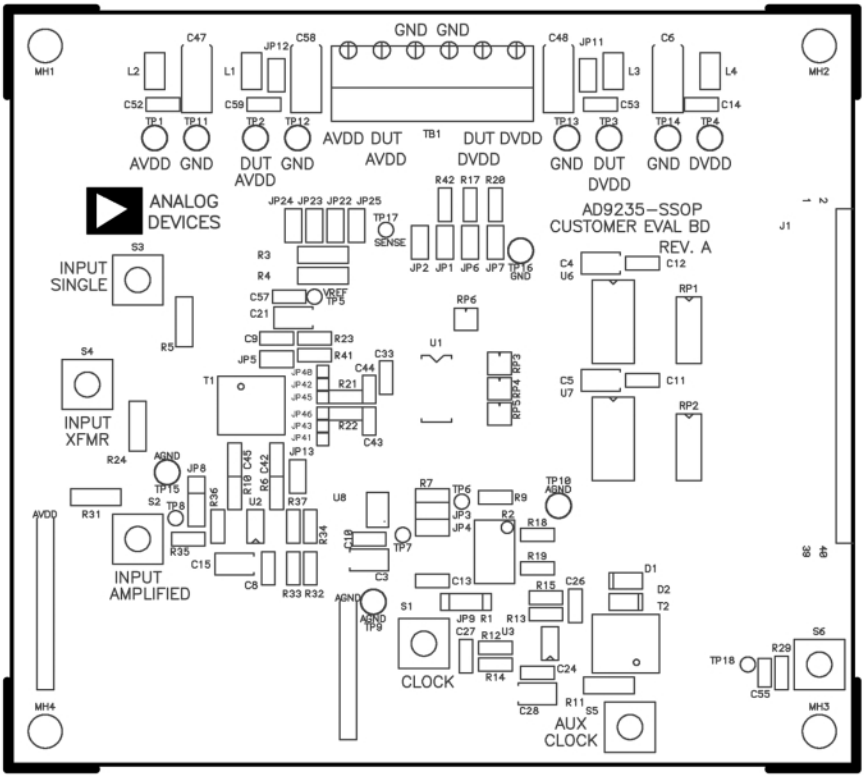


Figure 25. Evaluation Board Layout, Primary Silkscreen

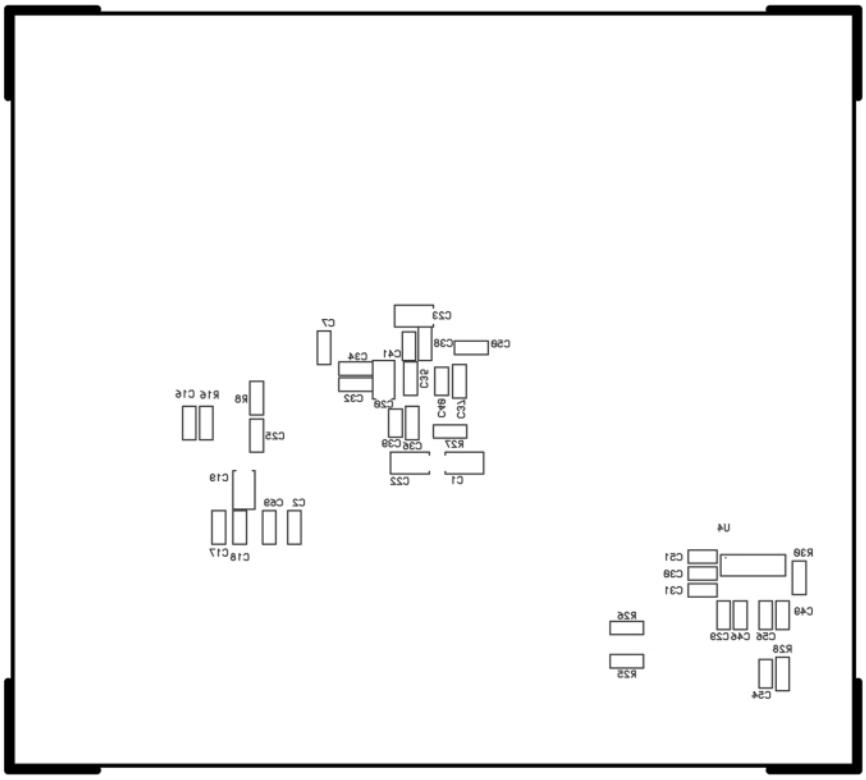
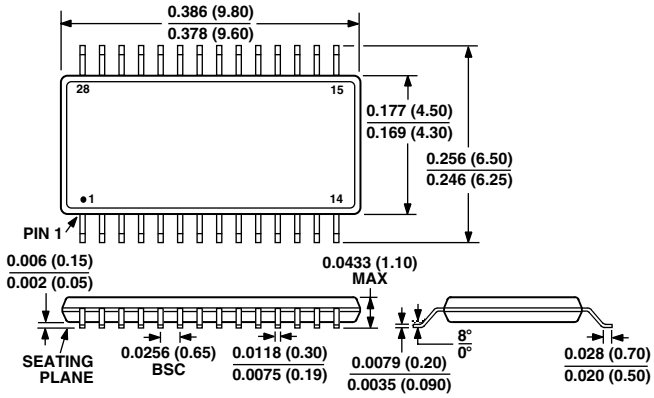


Figure 26. Evaluation Board Layout, Secondary Silkscreen

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead TSSOP
(RU-28)



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