

# Darlington Complementary Silicon Power Transistors

... designed for general-purpose amplifier and low-speed switching motor control applications.

- Similar to the Popular NPN 2N6284 and the PNP 2N6287
- Rugged RBSOA Characteristics
- Monolithic Construction with Built-in Collector-Emitter Diode

## MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	100	Vdc
Collector-Base Voltage	$V_{CB}$	100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous Peak	$I_C$	20 40	Adc
Base Current	$I_B$	0.5	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	160 1.28	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.78	$^\circ\text{C/W}$

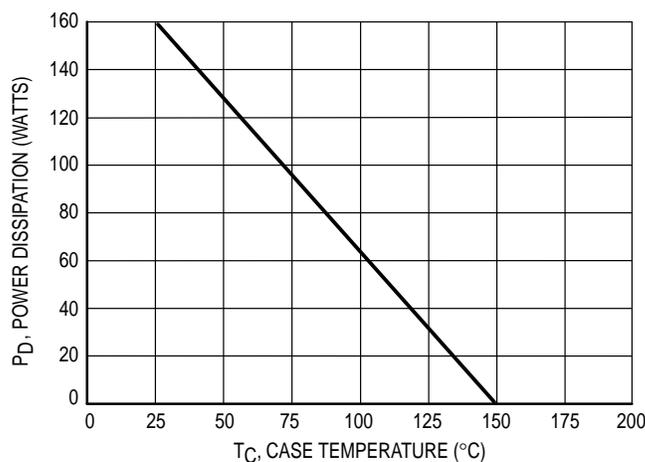


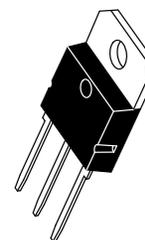
Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

**NPN**  
**MJH6284**  
**PNP**  
**MJH6287**

Motorola Preferred Devices

**DARLINGTON**  
**20 AMPERE**  
**COMPLEMENTARY SILICON**  
**POWER TRANSISTORS**  
**100 VOLTS**  
**160 WATTS**



CASE 340D-02

# MJH6284 MJH6287

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 0.1 Adc, I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	100	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 50 Vdc, I <sub>B</sub> = 0)	I <sub>CEO</sub>	—	1.0	mAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CE</sub> = Rated V <sub>CB</sub> , V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C)	I <sub>CEx</sub>	—	0.5 5.0	mAdc
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	2.0	mAdc

## ON CHARACTERISTICS (1)

DC Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc) (I <sub>C</sub> = 20 Adc, V <sub>CE</sub> = 3.0 Vdc)	h <sub>FE</sub>	750 100	18,000 —	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 10 Adc, I <sub>B</sub> = 40 mAdc) (I <sub>C</sub> = 20 Adc, I <sub>B</sub> = 200 mAdc)	V <sub>CE(sat)</sub>	—	2.0 3.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc)	V <sub>BE(on)</sub>	—	2.8	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 20 Adc, I <sub>B</sub> = 200 mAdc)	V <sub>BE(sat)</sub>	—	4.0	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain Bandwidth Product (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 MHz)	f <sub>T</sub>	4.0	—	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	C <sub>ob</sub>	—	400 600	pF
				MJH6284 MJH6287
Small–Signal Current Gain (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 3.0 Vdc, f = 1.0 kHz)	h <sub>fe</sub>	300	—	—

## SWITCHING CHARACTERISTICS

Resistive Load		Symbol	Typical		Unit
			NPN	PNP	
Delay Time	V <sub>CC</sub> = 30 Vdc, I <sub>C</sub> = 10 Adc I <sub>B1</sub> = I <sub>B2</sub> = 100 mA Duty Cycle = 1.0%	t <sub>d</sub>	0.1	0.1	μs
Rise Time		t <sub>r</sub>	0.3	0.3	
Storage Time		t <sub>s</sub>	1.0	1.0	
Fall Time		t <sub>f</sub>	3.5	2.0	

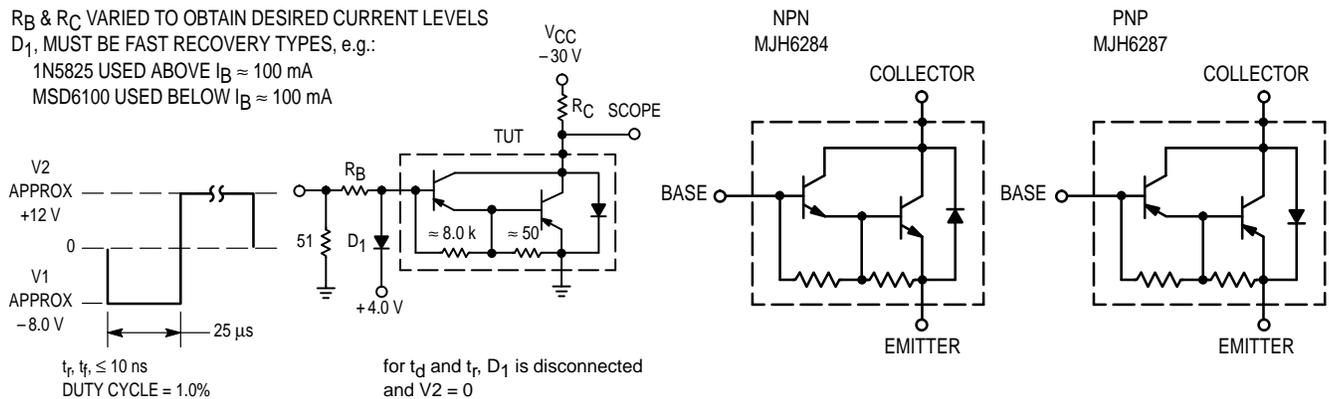
(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

R<sub>B</sub> & R<sub>C</sub> VARIED TO OBTAIN DESIRED CURRENT LEVELS

D<sub>1</sub>, MUST BE FAST RECOVERY TYPES, e.g.:

1N5825 USED ABOVE I<sub>B</sub> ≈ 100 mA

MSD6100 USED BELOW I<sub>B</sub> ≈ 100 mA



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

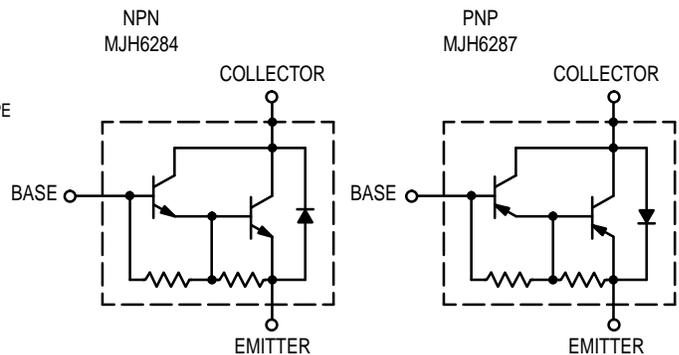


Figure 3. Darlington Schematic

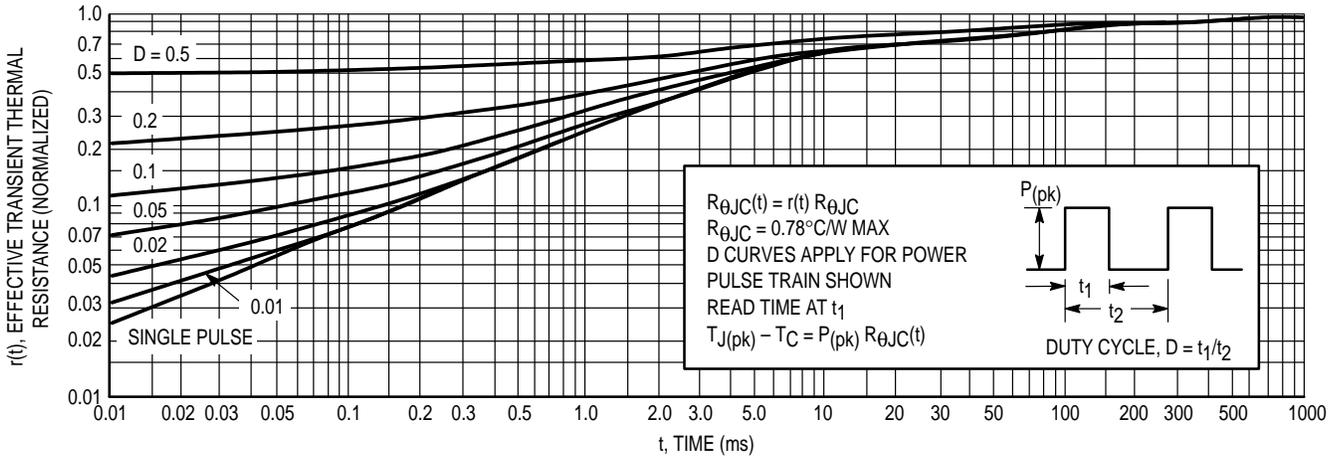


Figure 4. Thermal Response

**FBSOA, FORWARD BIAS SAFE OPERATING AREA**

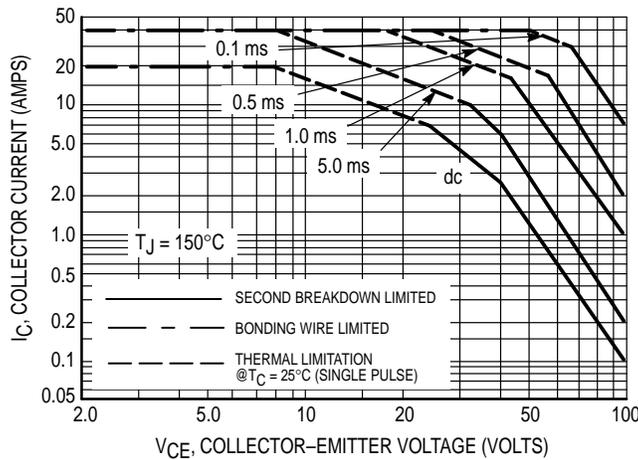


Figure 5. MJH6284, MJH6287

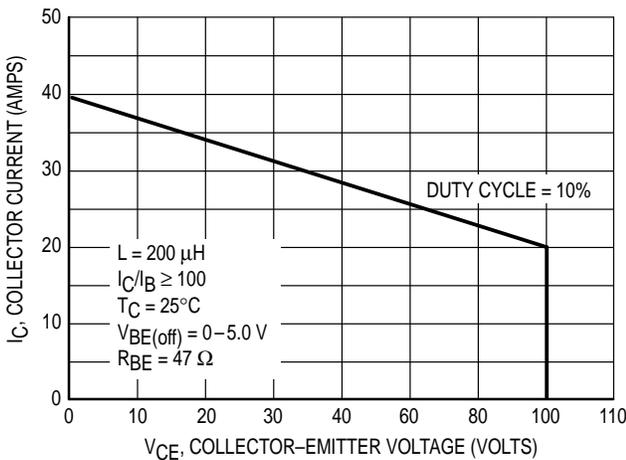


Figure 6. Maximum RBSOA, Reverse Bias Safe Operating Area

**FORWARD BIAS**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_J(pk) = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_J(pk) \leq 150^{\circ}\text{C}$ .  $T_J(pk)$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

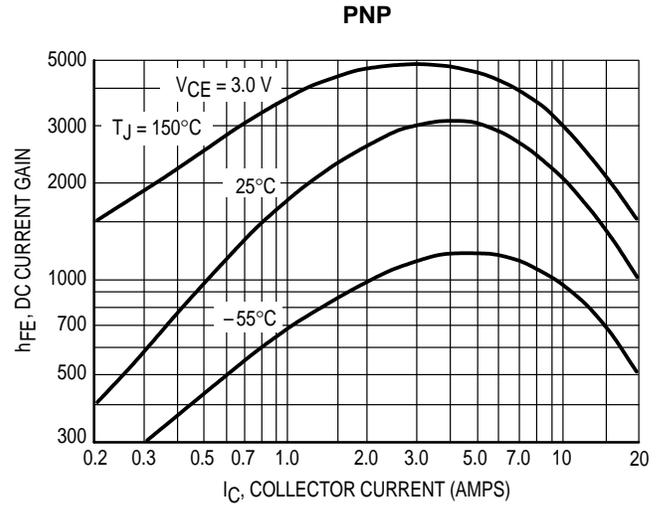
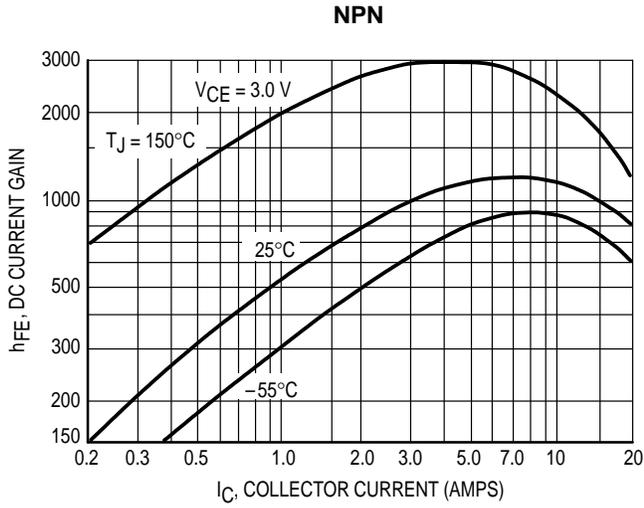


Figure 7. DC Current Gain

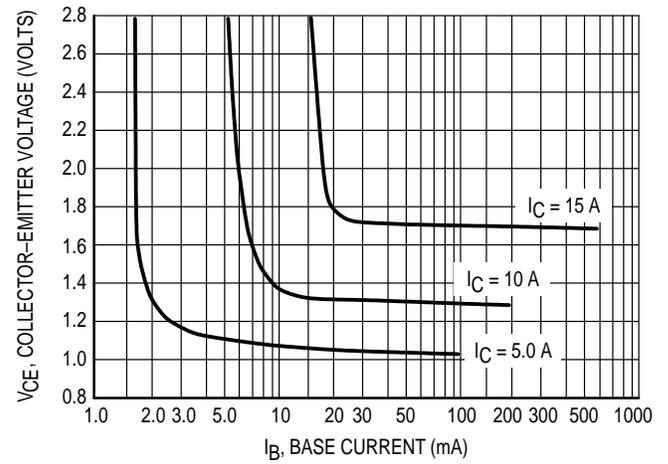
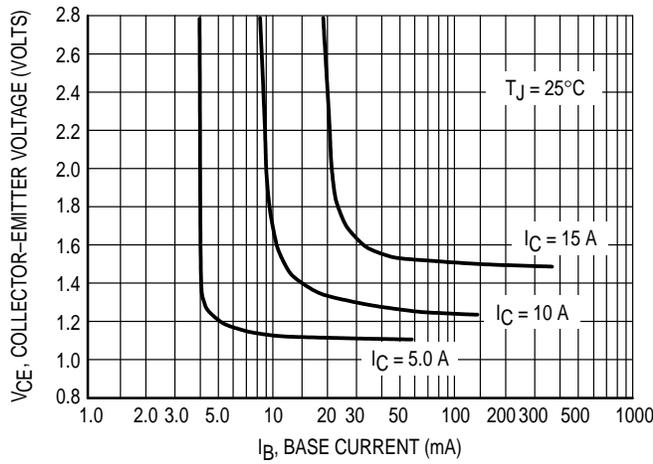


Figure 8. Collector Saturation Region

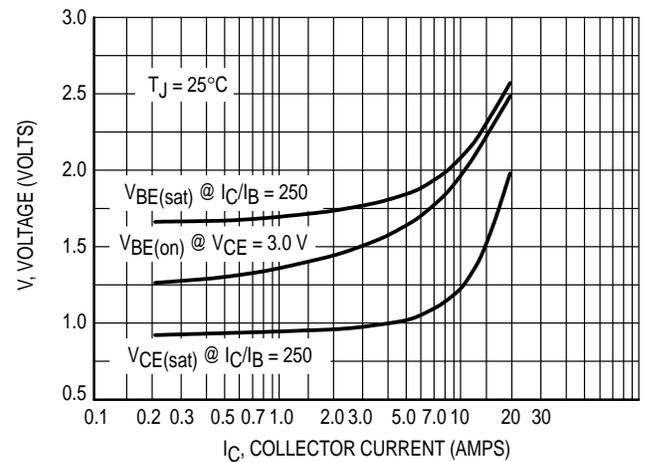
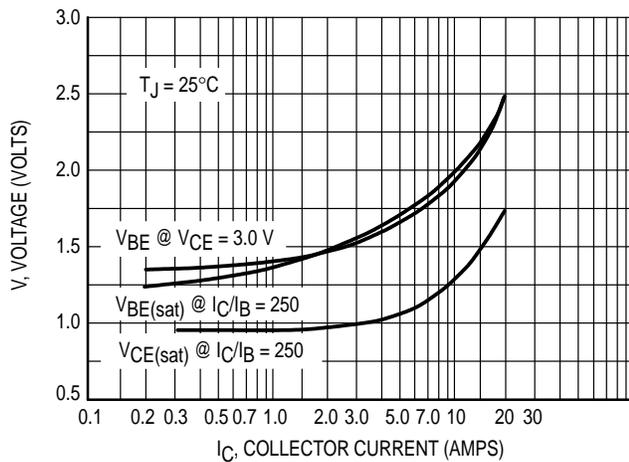
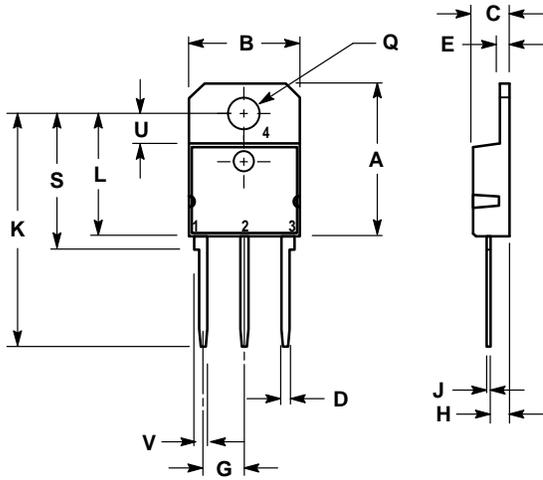


Figure 9. "On" Voltages

PACKAGE DIMENSIONS



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	20.35	—	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	—	16.20	—	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

- STYLE 1:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR

CASE 340D-02  
 ISSUE B

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