

SN5404, SN54LS04, SN54S04, SN7404, SN74LS04, SN74S04 HEX INVERTERS

SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

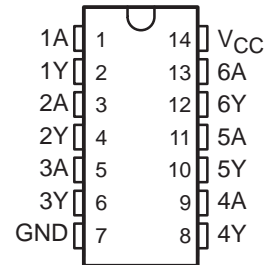
- Dependable Texas Instruments Quality and Reliability

description/ordering information

These devices contain six independent inverters.

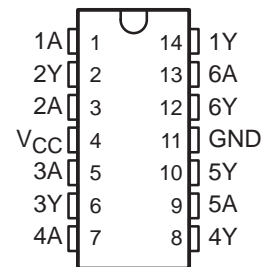
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE

(TOP VIEW)



SN5404 . . . W PACKAGE

(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS**

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ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------------|-----------------|---------------|------------------------------|-------------------------|
| 0°C to 70°C | PDIP – N | Tube | SN7404N | SN7404N |
| | | Tube | SN74LS04N | SN74LS04N |
| | | Tube | SN74S04N | SN74S04N |
| | SOIC – D | Tube | SN7404D | 7404 |
| | | Tape and reel | SN7404DR | |
| | | Tube | SN74LS04D | LS04 |
| | | Tape and reel | SN74LS04DR | |
| | | Tube | SN74S04D | S04 |
| | | Tape and reel | SN74S04DR | |
| | SOP – NS | Tape and reel | SN7404NSR | SN7404 |
| | | Tape and reel | SN74LS04NSR | 74LS04 |
| | | Tape and reel | SN74S04NSR | 74S04 |
| | SSOP – DB | Tape and reel | SN74LS04DBR | LS04 |
| | –55°C to 125°C | CDIP – J | Tube | SN5404J |
| Tube | | | SNJ5404J | SNJ5404J |
| Tube | | | SN54LS04J | SN54LS04J |
| Tube | | | SN54S04J | SN54S04J |
| Tube | | | SNJ54LS04J | SNJ54LS04J |
| Tube | | | SNJ54S04J | SNJ54S04J |
| CFP – W | | Tube | SNJ5404W | SNJ5404W |
| | | Tube | SNJ54LS04W | SNJ54LS04W |
| | | Tube | SNJ54S04W | SNJ54S04W |
| LCCC – FK | | Tube | SNJ54LS04FK | SNJ54LS04FK |
| | | Tube | SNJ54S04FK | SNJ54S04FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE
(each inverter)**

| INPUT A | OUTPUT Y |
|--------------------|---------------------|
| H | L |
| L | H |



**SN5404, SN54LS04, SN54S04,
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logic diagram (positive logic)

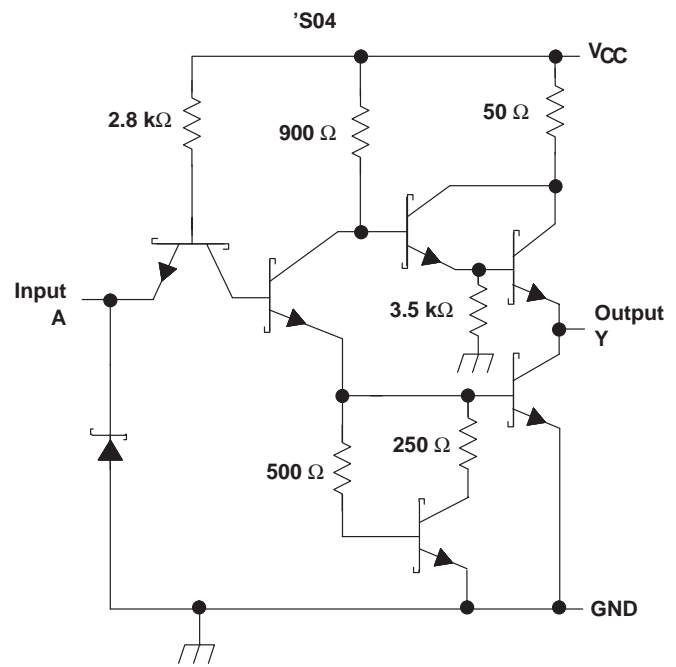
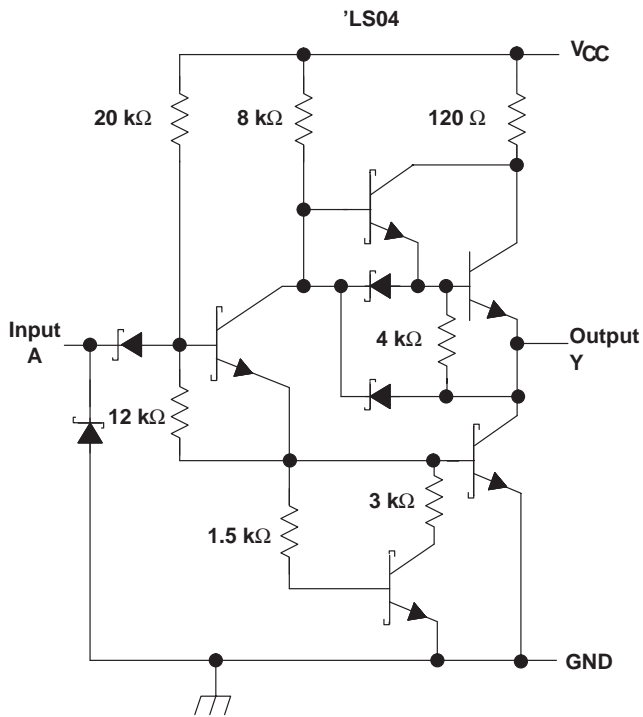
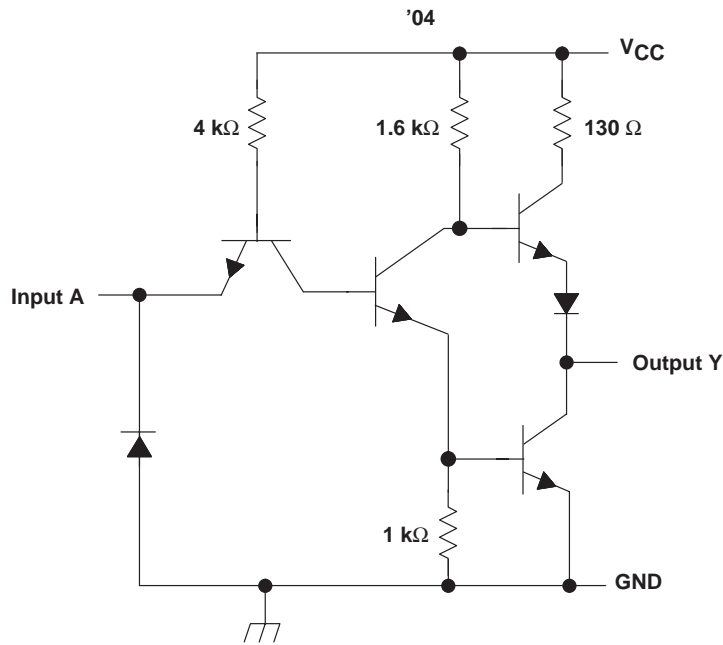


$$Y = \bar{A}$$

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schematics (each gate)



Resistor values shown are nominal.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I : '04, 'S04 | 5.5 V |
| 'LS04 | 7 V |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| DB package | 96°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | SN5404 | | | SN7404 | | | UNIT |
|----------|--------------------------------|--------|-----|-----|--------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | 0.8 | | | 0.8 | | | V |
| I_{OH} | High-level output current | -0.4 | | | -0.4 | | | mA |
| I_{OL} | Low-level output current | 16 | | | 16 | | | mA |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | SN5404 | | | SN7404 | | | UNIT |
|-----------|---|--------|------|------|--------|------|------|------|
| | | MIN | TYP§ | MAX | MIN | TYP§ | MAX | |
| V_{IK} | $V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} | $V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$ | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| V_{OL} | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 16 \text{ mA}$ | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| I_I | $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | | 1 | | | 1 | mA |
| I_{IH} | $V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$ | | | 40 | | | 40 | µA |
| I_{IL} | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | | | -1.6 | | | -1.6 | mA |
| $I_{OS}¶$ | $V_{CC} = \text{MAX}$ | -20 | | -55 | -18 | | -55 | mA |
| I_{CCH} | $V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$ | | 6 | 12 | | 6 | 12 | mA |
| I_{CCL} | $V_{CC} = \text{MAX}$, $V_I = 4.5 \text{ V}$ | | 18 | 33 | | 18 | 33 | mA |

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

¶ Not more than one output should be shorted at a time.



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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN5404 SN7404 | | | UNIT |
|-----------|--------------|-------------|---|------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | |
| t_{PLH} | A | Y | $R_L = 400\ \Omega$, $C_L = 15\text{ pF}$ | 12 | | 22 | ns |
| t_{PHL} | | | | 8 | | 15 | |

recommended operating conditions (see Note 3)

| | | SN54LS04 | | | SN74LS04 | | | UNIT |
|----------|--------------------------------|----------|-----|-----|----------|-----|------|------------------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | 0.7 | | | 0.8 | | | V |
| I_{OH} | High-level output current | -0.4 | | | -0.4 | | | mA |
| I_{OL} | Low-level output current | 4 | | | 8 | | | mA |
| T_A | Operating free-air temperature | -55 | | | 125 | | | $^\circ\text{C}$ |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54LS04 | | | SN74LS04 | | | UNIT |
|-----------|---|------------------------|------|------|----------|------|------|---------------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | $V_{CC} = \text{MIN}$, $I_I = -18\text{ mA}$ | -1.5 | | | -1.5 | | | V |
| V_{OH} | $V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $I_{OH} = -0.4\text{ mA}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V_{OL} | $V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$ | $I_{OL} = 4\text{ mA}$ | | 0.4 | | 0.4 | | V |
| | | $I_{OL} = 8\text{ mA}$ | | | | 0.25 | | |
| I_I | $V_{CC} = \text{MAX}$, $V_I = 7\text{ V}$ | 0.1 | | | 0.1 | | | mA |
| I_{IH} | $V_{CC} = \text{MAX}$, $V_I = 2.7\text{ V}$ | 20 | | | 20 | | | μA |
| I_{IL} | $V_{CC} = \text{MAX}$, $V_I = 0.4\text{ V}$ | -0.4 | | | -0.4 | | | mA |
| $I_{OS}§$ | $V_{CC} = \text{MAX}$ | -20 | | -100 | -20 | | -100 | mA |
| I_{CCH} | $V_{CC} = \text{MAX}$, $V_I = 0\text{ V}$ | 1.2 | | 2.4 | 1.2 | | 2.4 | mA |
| I_{CCL} | $V_{CC} = \text{MAX}$, $V_I = 4.5\text{ V}$ | 3.6 | | 6.6 | 3.6 | | 6.6 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN54LS04 SN74LS04 | | | UNIT |
|-----------|--------------|-------------|--|----------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | |
| t_{PLH} | A | Y | $R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$ | 9 | | 15 | ns |
| t_{PHL} | | | | 10 | | 15 | |



**SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS**

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recommended operating conditions (see Note 3)

| | | SN54S04 | | | SN74S04 | | | UNIT |
|----------|--------------------------------|---------|-----|-----|---------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} | High-level output current | | | -1 | | | -1 | mA |
| I_{OL} | Low-level output current | | | 20 | | | 20 | mA |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54S04 | | | SN74S04 | | | UNIT |
|-----------|---|---------|------|------|---------|------|------|------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | $V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$ | | | -1.2 | | | -1.2 | V |
| V_{OH} | $V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -1 \text{ mA}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V_{OL} | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 20 \text{ mA}$ | | | 0.5 | | | 0.5 | V |
| I_I | $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | | 1 | | | 1 | mA |
| I_{IH} | $V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$ | | | 50 | | | 50 | µA |
| I_{IL} | $V_{CC} = \text{MAX}$, $V_I = 0.5 \text{ V}$ | | | -2 | | | -2 | mA |
| $I_{OS}§$ | $V_{CC} = \text{MAX}$ | -40 | | -100 | -40 | | -100 | mA |
| I_{CCH} | $V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$ | | 15 | 24 | | 15 | 24 | mA |
| I_{CCL} | $V_{CC} = \text{MAX}$, $V_I = 4.5 \text{ V}$ | | 30 | 54 | | 30 | 54 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

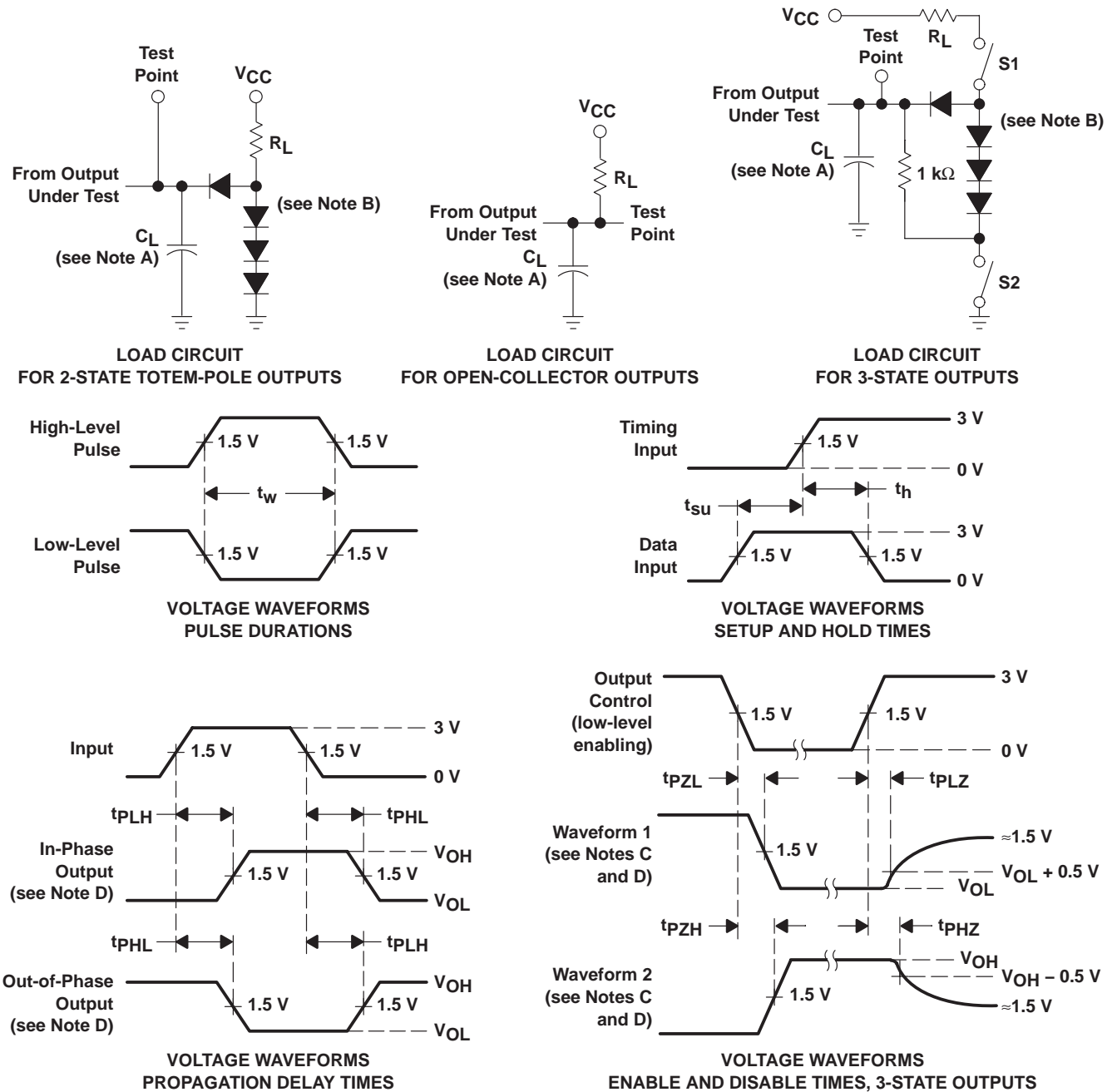
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | SN54S04 SN74S04 | | | UNIT |
|-----------|--------------|-------------|--|--------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | |
| t_{PLH} | A | Y | $R_L = 280 \Omega$, $C_L = 15 \text{ pF}$ | 3 4.5 | | | ns |
| t_{PHL} | | | | 3 5 | | | |
| t_{PLH} | A | Y | $R_L = 280 \Omega$, $C_L = 50 \text{ pF}$ | 4.5 | | | ns |
| t_{PHL} | | | | 5 | | | |



SN5404, SN54LS04, SN54S04, SN7404, SN74LS04, SN74S04 HEX INVERTERS

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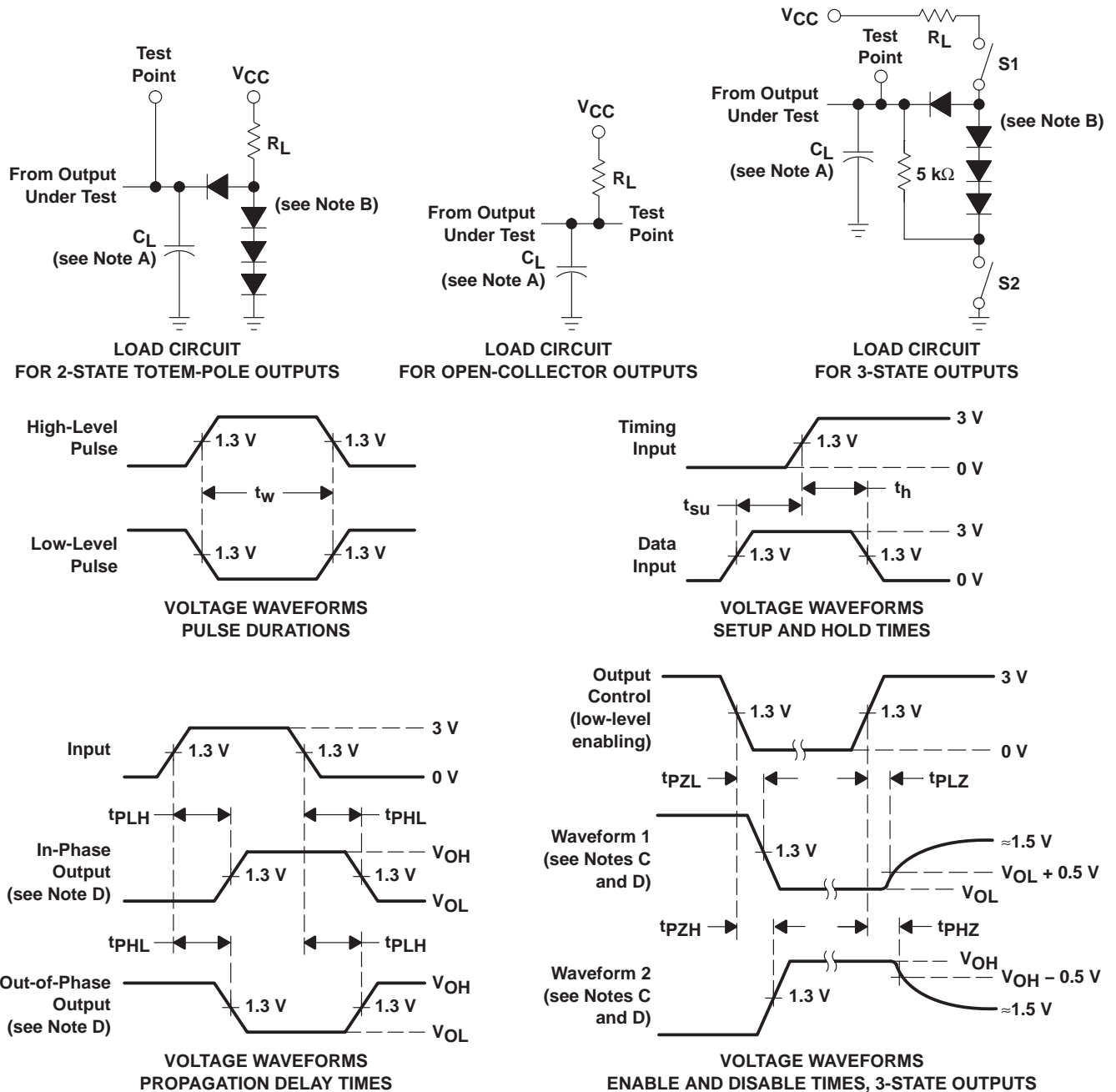
PARAMETER MEASUREMENT INFORMATION SERIES 54/74 AND 54S/74S DEVICES



- NOTES:
- C_L includes probe and jig capacitance.
 - All diodes are 1N3064 or equivalent.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PZL} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 - The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O \approx 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
 G. The outputs are measured one at a time, with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| JM38510/00105BCA | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/00105BDA | ACTIVE | CFP | W | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/07003BCA | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/30003B2A | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/30003BCA | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/30003BDA | ACTIVE | CFP | W | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/30003SCA | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/30003SDA | ACTIVE | CFP | W | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SN5404J | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SN54LS04J | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SN54S04J | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SN7404D | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN7404DR | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN7404N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN7404N3 | OBSOLETE | PDIP | N | 14 | | None | Call TI | Call TI |
| SN7404NSR | ACTIVE | SO | NS | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LS04D | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LS04DR | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LS04J | OBSOLETE | CDIP | J | 14 | | None | Call TI | Call TI |
| SN74LS04N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74LS04N3 | OBSOLETE | PDIP | N | 14 | | None | Call TI | Call TI |
| SN74LS04NSR | ACTIVE | SO | NS | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74S04D | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74S04DR | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74S04N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74S04N3 | OBSOLETE | PDIP | N | 14 | | None | Call TI | Call TI |
| SN74S04NSR | ACTIVE | SO | NS | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SNJ5404J | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ5404W | ACTIVE | CFP | W | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54LS04FK | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54LS04J | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54LS04W | ACTIVE | CFP | W | 14 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54S04FK | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54S04J | ACTIVE | CDIP | J | 14 | 1 | None | Call TI | Level-NC-NC-NC |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SNJ54S04W | ACTIVE | CFP | W | 14 | 1 | None | Call TI | Level-NC-NC-NC |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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