



# CSD19531KCS 100 V N-Channel NexFET™ Power MOSFET

## 1 Features

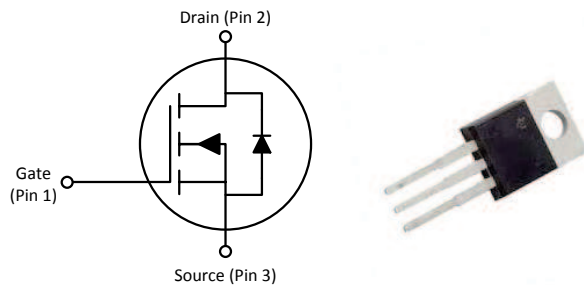
- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

## 2 Applications

- Secondary Side Synchronous Rectifier
- Hot Swap Telecom
- Motor Control

## 3 Description

This 100 V, 6.4 m $\Omega$ , TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	100		V
$Q_g$	Gate Charge Total (10 V)	37		nC
$Q_{gd}$	Gate Charge Gate to Drain	7.5		nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 6\text{ V}$	7.3	m $\Omega$
		$V_{GS} = 10\text{ V}$	6.4	m $\Omega$
$V_{GS(th)}$	Threshold Voltage	2.7		V

### Ordering Information<sup>(1)</sup>

Device	Package	Media	Qty	Ship
CSD19531KCS	TO-220 Plastic Package	Tube	50	Tube

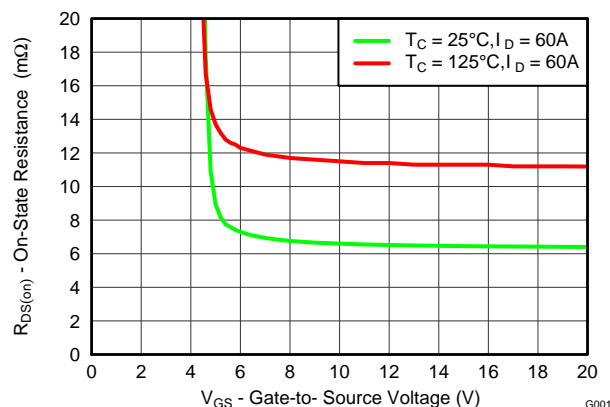
(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

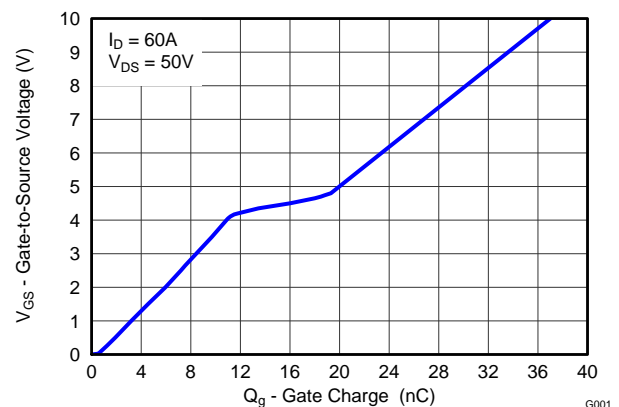
$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	110	
	Continuous Drain Current (Silicon limited), $T_C = 100^\circ\text{C}$	78	
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	285	A
$P_D$	Power Dissipation	214	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 60\text{ A}, L = 0.1\text{ mH}, R_G = 25\text{ }\Omega$	180	mJ

(1) Max  $R_{\theta JC} = 0.7^\circ\text{C/W}$ , Pulse duration  $\leq 100\text{ }\mu\text{s}$ , Duty cycle  $\leq 1\%$

**$R_{DS(on)}$  vs  $V_{GS}$**



**Gate Charge**



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## 4 Revision History

<b>Changes from Original (September 2013) to Revision A</b>	<b>Page</b>
• Added part number to title .....	<b>1</b>
• Updated the silicon limited currents to reflect increase in device operating temperature range .....	<b>1</b>
• Increased pulsed current to reflect new conditions .....	<b>1</b>
• Increased max power dissipation to reflect new conditions .....	<b>1</b>
• Increased operating and junction temperature range to 175°C .....	<b>1</b>
• Updated the pulsed drain current conditions .....	<b>1</b>
• Changed <a href="#">Figure 1</a> from a normalized $R_{\theta JA}$ curve to a normalized $R_{\theta JC}$ curve .....	<b>4</b>
• Updated <a href="#">Figure 6</a> to reflect increase in device operating temperature range .....	<b>5</b>
• Updated <a href="#">Figure 8</a> to reflect increase in device operating temperature range .....	<b>5</b>
• Updated <a href="#">Figure 10</a> to reflect measured SOA data .....	<b>6</b>
• Updated <a href="#">Figure 12</a> to reflect increase in device operating temperature range .....	<b>6</b>

## 5 Specifications

### 5.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV <sub>DSS</sub>	Drain-to-Source Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 80 V			1	μA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA
V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.2	2.7	3.3	V
R <sub>DS(on)</sub>	Drain-to-Source On Resistance	V <sub>GS</sub> = 6 V, I <sub>D</sub> = 60 A	7.3		8.8	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 60 A	6.4		7.7	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 60 A	137			S
DYNAMIC CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V, f = 1 MHz		2980	3870	pF
C <sub>oss</sub>	Output Capacitance			560	728	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			13	17	pF
R <sub>G</sub>	Series Gate Resistance		1.3	2.6		Ω
Q <sub>g</sub>	Gate Charge Total (10 V)	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 60 A		38		nC
Q <sub>gd</sub>	Gate Charge Gate to Drain			7.5		nC
Q <sub>gs</sub>	Gate Charge Gate to Source			11.9		nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			7.3		nC
Q <sub>oss</sub>	Output Charge	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		98		nC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>DS</sub> = 60 A, R <sub>G</sub> = 0 Ω		8.4		ns
t <sub>r</sub>	Rise Time			7.2		ns
t <sub>d(off)</sub>	Turn Off Delay Time			16		ns
t <sub>f</sub>	Fall Time			4.1		ns
DIODE CHARACTERISTICS						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>SD</sub> = 60 A, V <sub>GS</sub> = 0 V		0.9	1	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DS</sub> = 50 V, I <sub>F</sub> = 60 A, di/dt = 300 A/μs		270		nC
t <sub>rr</sub>	Reverse Recovery Time			83		ns

### 5.2 Thermal Information

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			0.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	

## 5.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

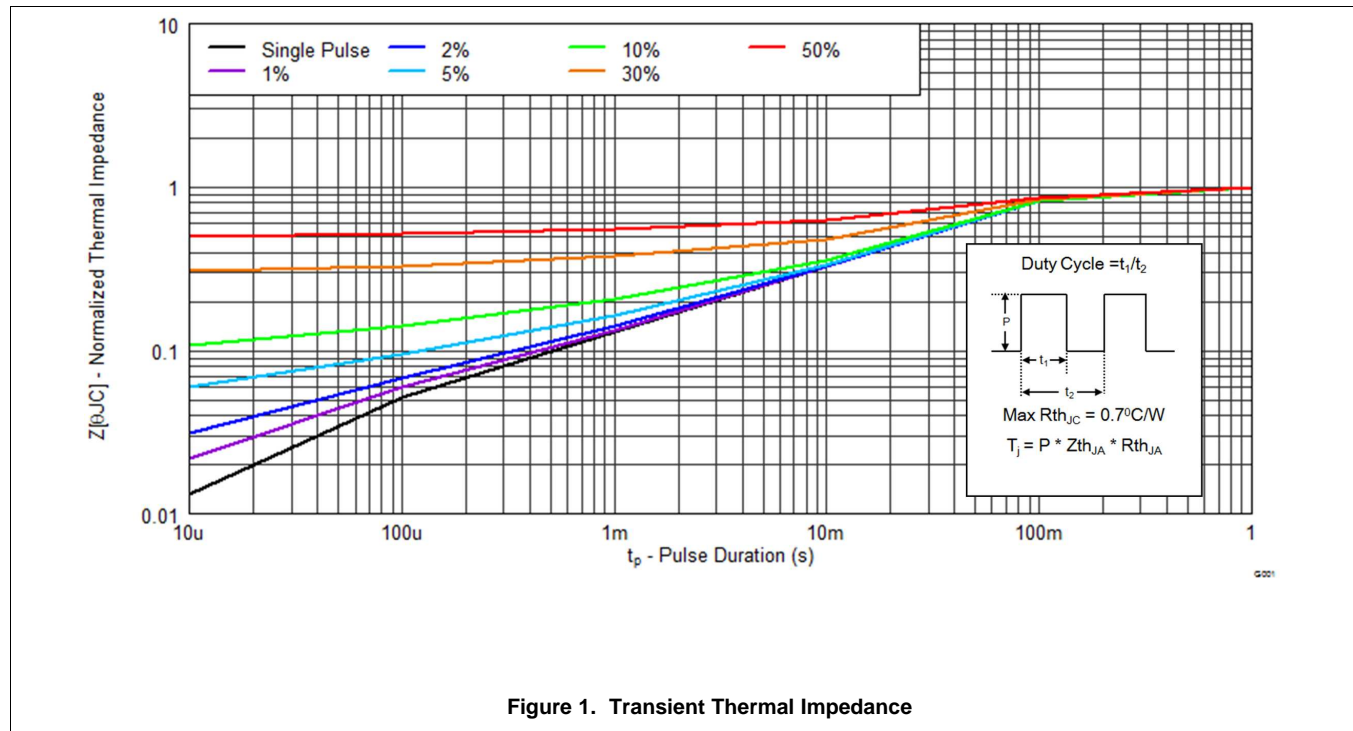


Figure 1. Transient Thermal Impedance

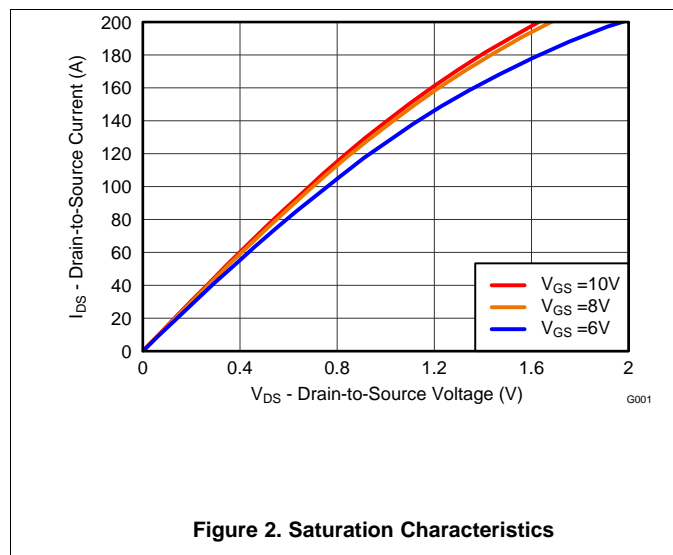


Figure 2. Saturation Characteristics

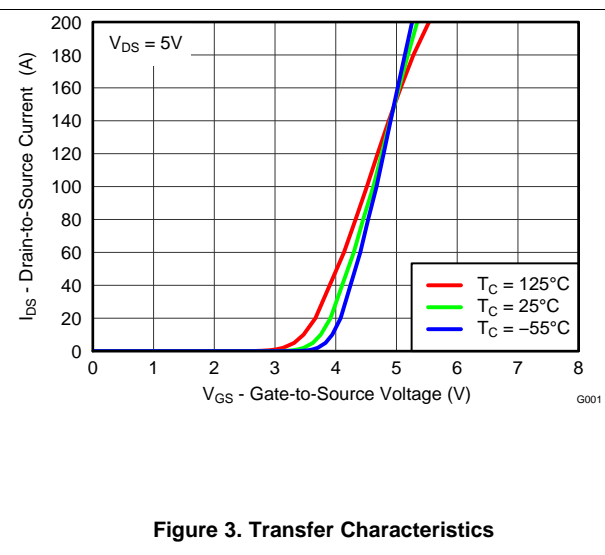


Figure 3. Transfer Characteristics

## Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

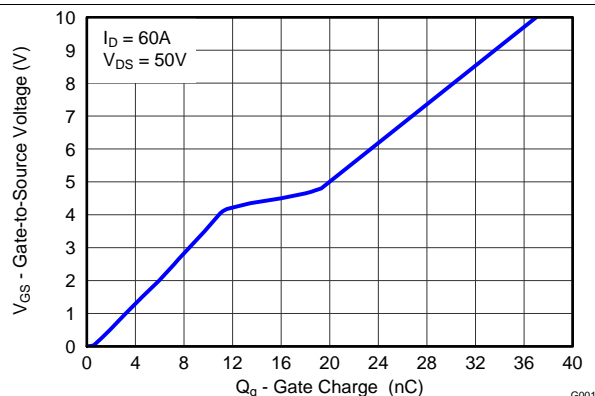


Figure 4. Gate Charge

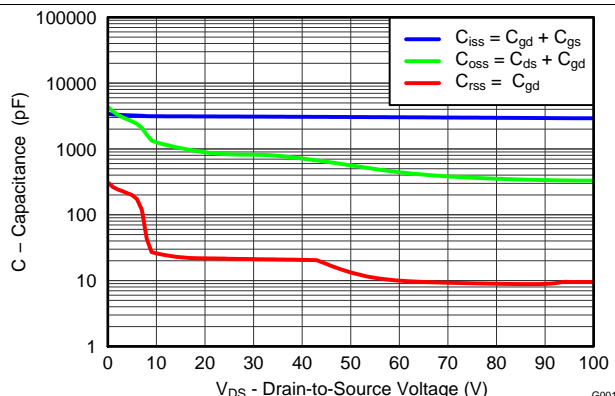


Figure 5. Capacitance

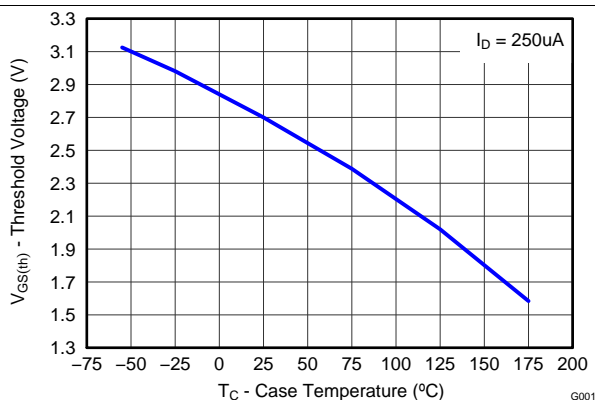


Figure 6. Threshold Voltage vs Temperature

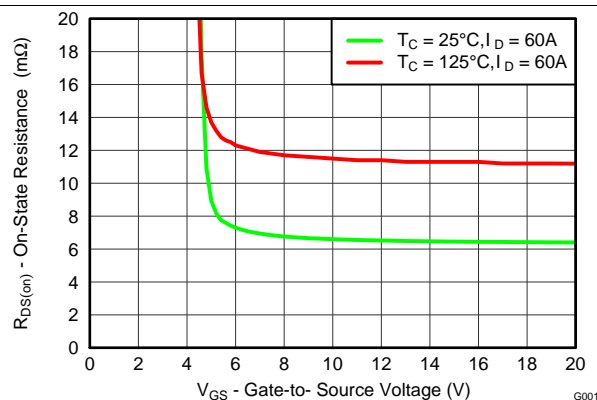


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

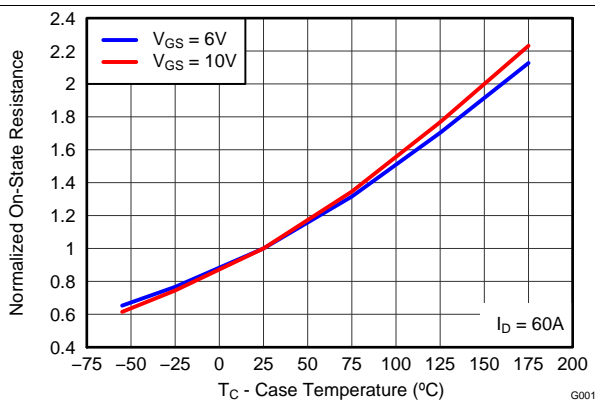


Figure 8. Normalized On-State Resistance vs Temperature

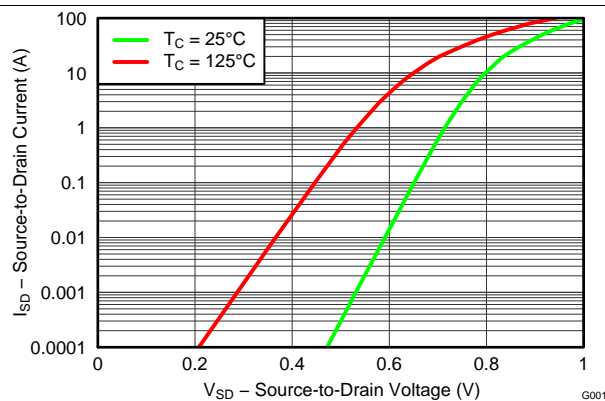
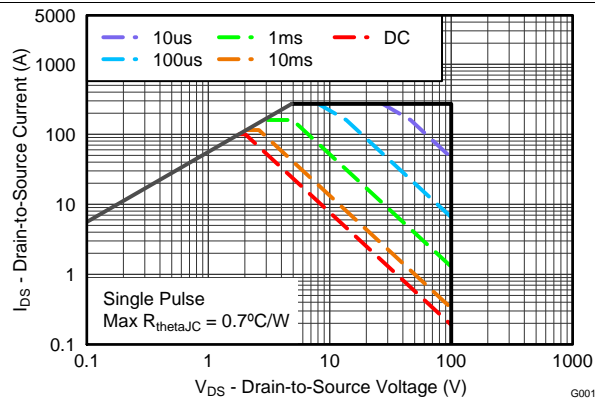


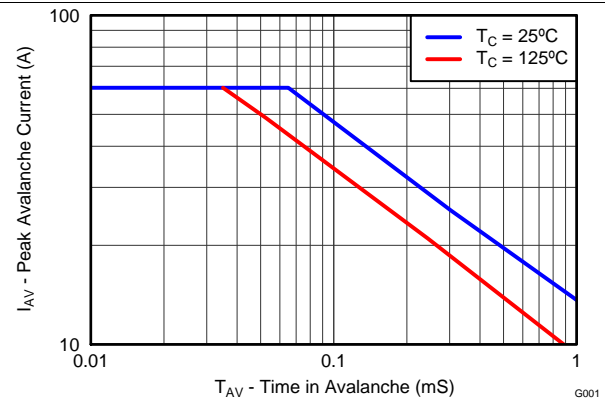
Figure 9. Typical Diode Forward Voltage

## Typical MOSFET Characteristics (continued)

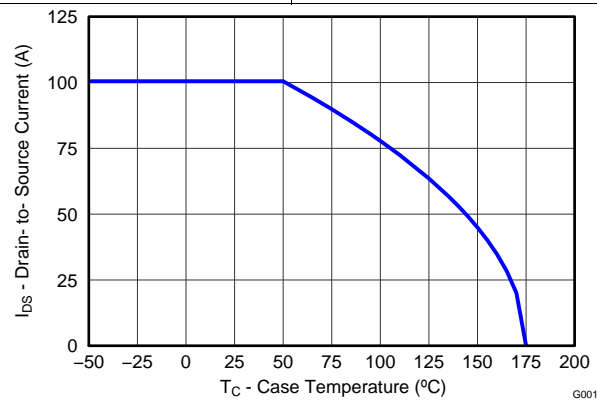
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



**Figure 10. Maximum Safe Operating Area**



**Figure 11. Single Pulse Unclamped Inductive Switching**



**Figure 12. Maximum Drain Current vs Temperature**

## 6 Device and Documentation Support

### 6.1 Trademarks

NexFET is a trademark of Texas Instruments.

### 6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.3 Glossary

[SLYZ022](#) — *TI Glossary*.

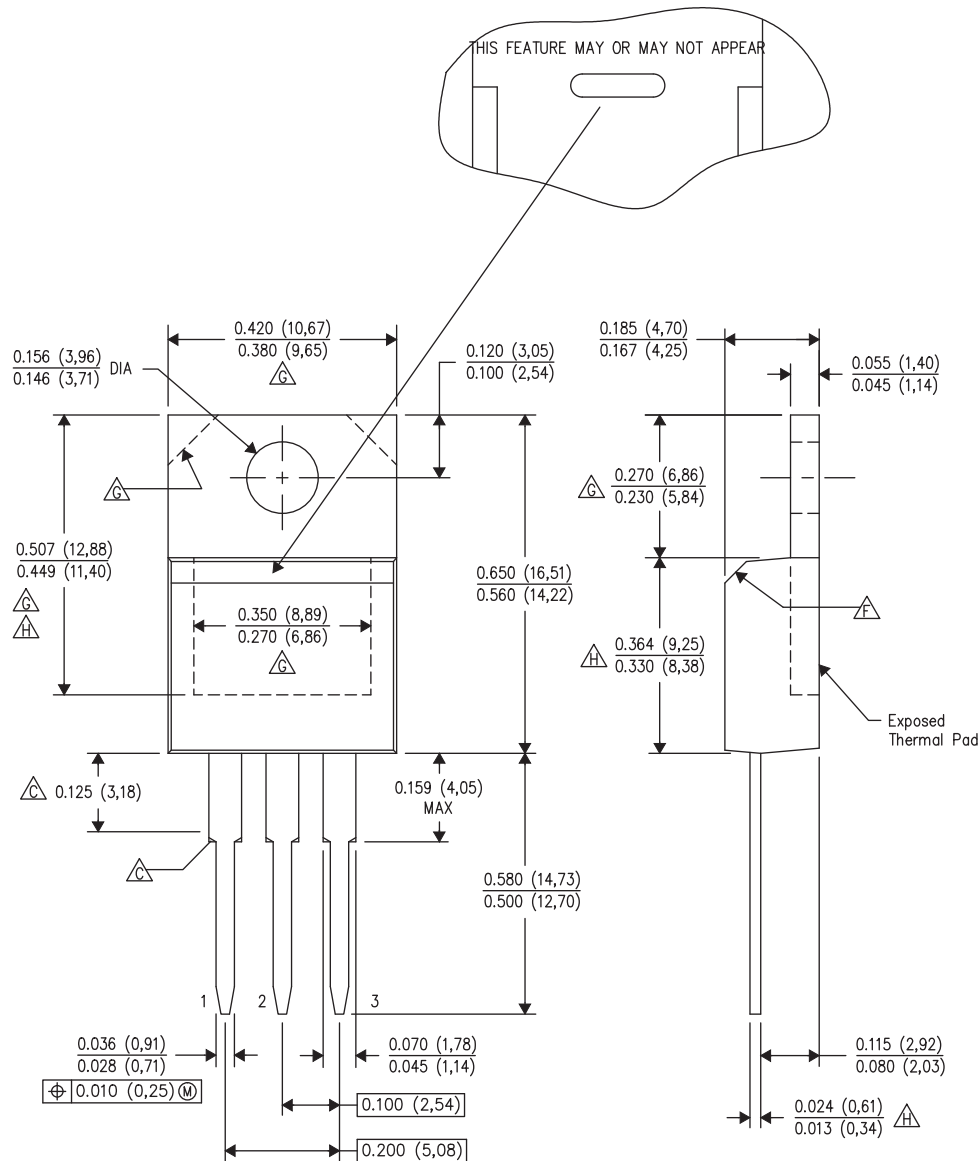
This glossary lists and explains terms, acronyms and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## 7.1 KCS Package Dimensions



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Lead dimensions are not controlled within this area. Chamfer may or may not appear
  - D. All lead dimensions apply before solder dip.
  - E. The center lead is in electrical contact with the mounting tab.
  - F. The chamfer is optional.
  - G. Thermal pad contour optional within these dimensions.
  - H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

### Pin Configuration

Position	Designation
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19531KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS Exempt)	CU SN	N / A for Pkg Type	-55 to 175	CSD19531KCS	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
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### Applications

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Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
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Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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