

## CMOS Hex Buffer

High-Voltage Types (20-Volt Rating)  
3-State Non-Inverting Type

■ CD4503B is a hex noninverting buffer with 3-state outputs having high sink- and source-current capability. Two disable controls are provided, one of which controls four buffers and the other controls the remaining two buffers.

The CD4503B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- 1 TTL-load output drive capability
- 2 output-disable controls
- 3-state outputs
- Pin compatible with industry types MM80C97, MC14503, and 340097
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- 3-state hex buffer for interfacing IC's with data buses
- CMOS to TTL hex buffer

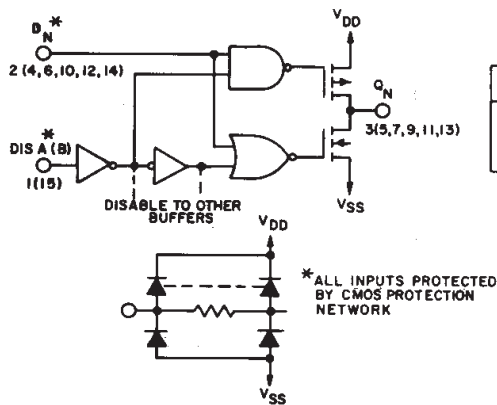
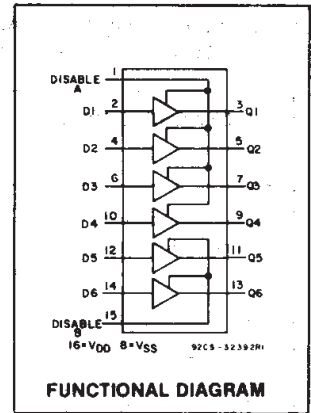


Fig. 1—Logic diagram of 1 to 6 identical buffers.

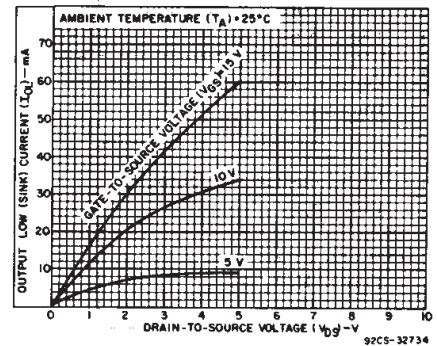


Fig. 2—Typical n-channel output low (sink) current characteristics.

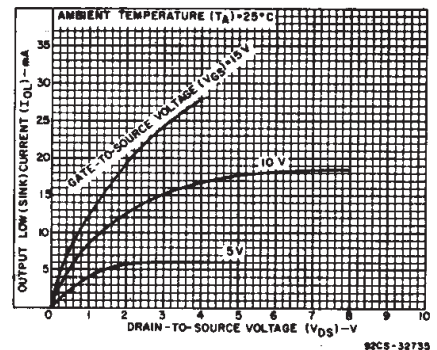


Fig. 3—Minimum n-channel output low (sink) current characteristics.

### MAXIMUM RATINGS, Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)

Voltages referenced to V<sub>SS</sub> Terminal ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V<sub>DD</sub> +0.5V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm$ 10mA

#### POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

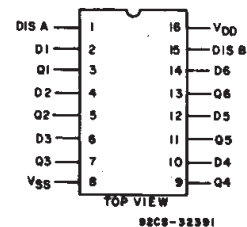
FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55°C to +125°C

STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -65°C to +150°C

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max ..... +265°C



### TERMINAL ASSIGNMENT

# CD4503B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0	5	2.6	2.5	1.4	1.3	2.1	2.3	—	mA
	0.5	0	10	6.5	6.4	3.9	3.8	5.5	6.2	—	
	1.5	0	15	19.2	18.9	11.4	11.2	16.1	23	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	5	5	-1.2	-1.16	-0.7	-0.7	-1.02	-1.9	—	mA
	2.5	5	5	-5.8	-5.7	-3.4	-3	-4.8	-8.1	—	
	9.5	10	10	-3.1	-3	-1.9	-1.8	-2.6	-3.7	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0.05			—	0	0.05	—	V
	—	0,10	10	0.05			—	0	0.05	—	
	—	0,15	15	0.05			—	0	0.05	—	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4.95			4.95	5	—	—	V
	—	0,10	10	9.95			9.95	10	—	—	
	—	0,15	15	14.95			14.95	15	—	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	—	5	1.5			—	—	1.5	—	V
	1.9	—	10	3			—	—	3	—	
	1.5, 13.5	—	15	4			—	—	4	—	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	—	5	3.5			3.5	—	—	—	V
	1.9	—	10	7			7	—	—	—	
	1.5, 13.5	—	15	11			11	—	—	—	
Input Current I <sub>IN</sub> Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA
3-State Output Leakage Current, I <sub>OUT</sub> Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	±10 <sup>-4</sup>	±0.4	

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range)	3	18	V

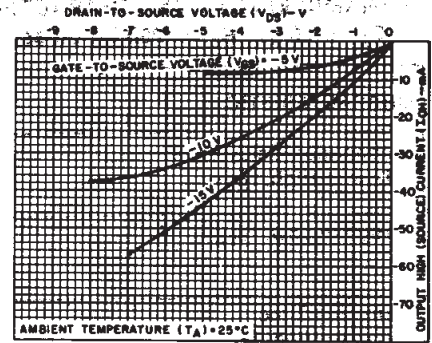


Fig. 4—Typical p-channel output high (source) current characteristics.

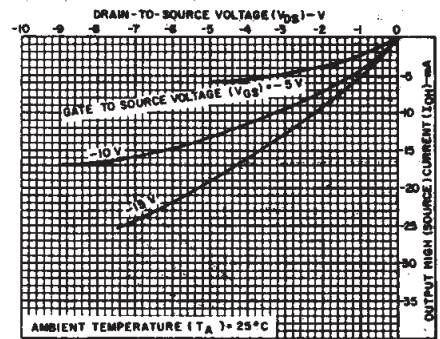


Fig. 5—Minimum p-channel output high (source) current characteristics.

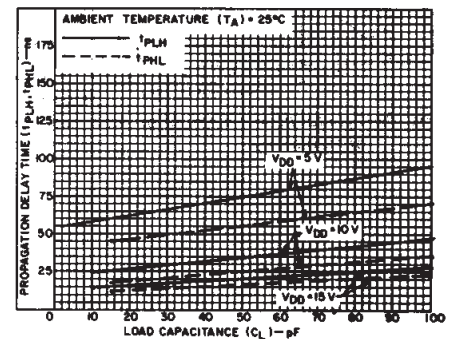


Fig. 6—Typical propagation delay time as a function of load capacitance.

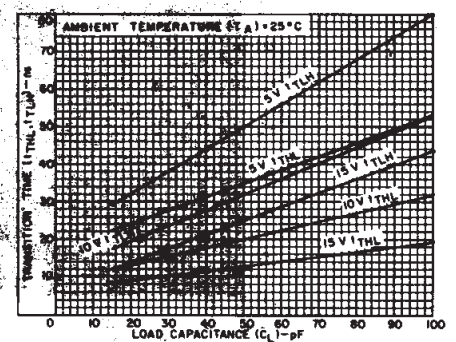


Fig. 7—Typical transition time as a function of load capacitance.

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4503B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$  unless otherwise specified.**

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS
		Typ.	Max.	
Propagation Delay Time: Low-to-High, $t_{PLH}$	5	75	150	ns
	10	35	70	
	15	25	50	
High-to-Low, $t_{PHL}$	5	55	110	ns
	10	25	50	
	15	17	35	
Transition Time: Low-to-High, $t_{TLH}$	5	50	90	ns
	10	30	45	
	15	25	35	
High-to-Low, $t_{THL}$	5	35	70	ns
	10	20	40	
	15	13	25	
3-State Propagation Delay Time: $R_L = 1\text{ k}\Omega$ $t_{PHZ}, t_{PZH}$	5	70	140	ns
	10	30	60	
	15	25	50	
$t_{PZL}, t_{PLZ}$	5	90	180	ns
	10	40	80	
	15	35	70	

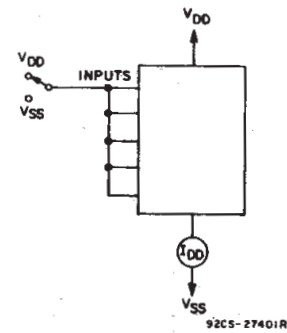


Fig. 10—Quiescent device current test circuit.

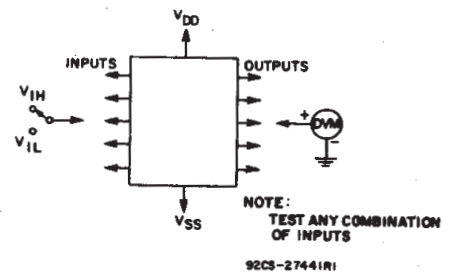


Fig. 11—Input voltage test circuit.

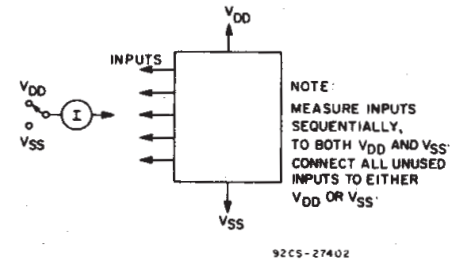


Fig. 12—Input current test circuit.

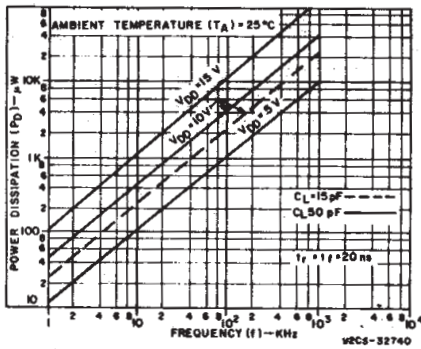


Fig. 8—Typical power dissipation as a function of frequency.

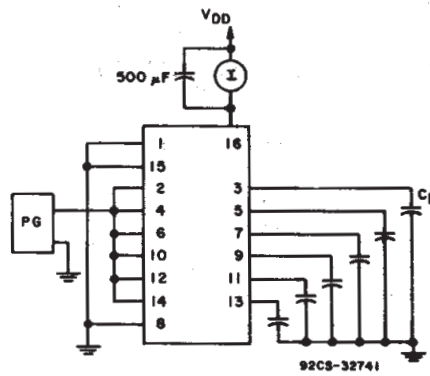
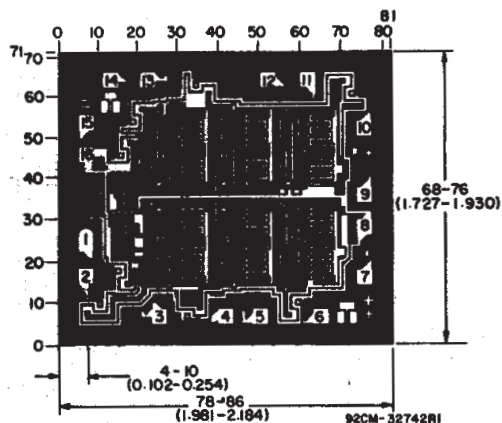


Fig. 9—Dynamic power dissipation test circuit.



## Dimensions and pad layout for CD4503BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD4503BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
CD4503BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Contact TI Distributor or Sales Office
CD4503BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	<a href="#">Purchase Samples</a>
CD4503BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	<a href="#">Purchase Samples</a>
CD4503BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>
CD4503BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD4503BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Purchase Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF CD4503B, CD4503B-MIL :

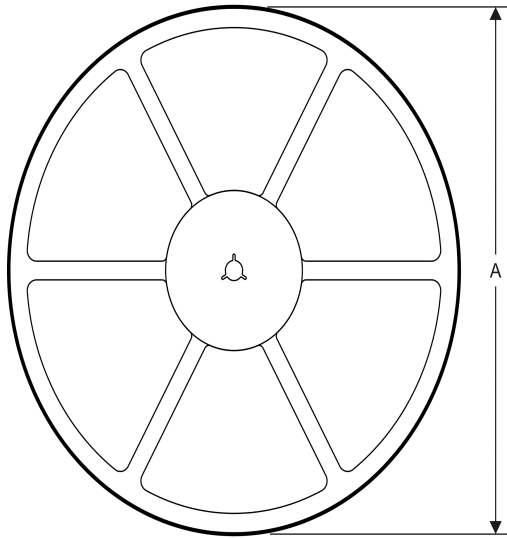
● Catalog: [CD4503B](#)

● Military: [CD4503B-MIL](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4503BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4503BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4503BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4503BNSR	SO	NS	16	2000	367.0	367.0	38.0



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

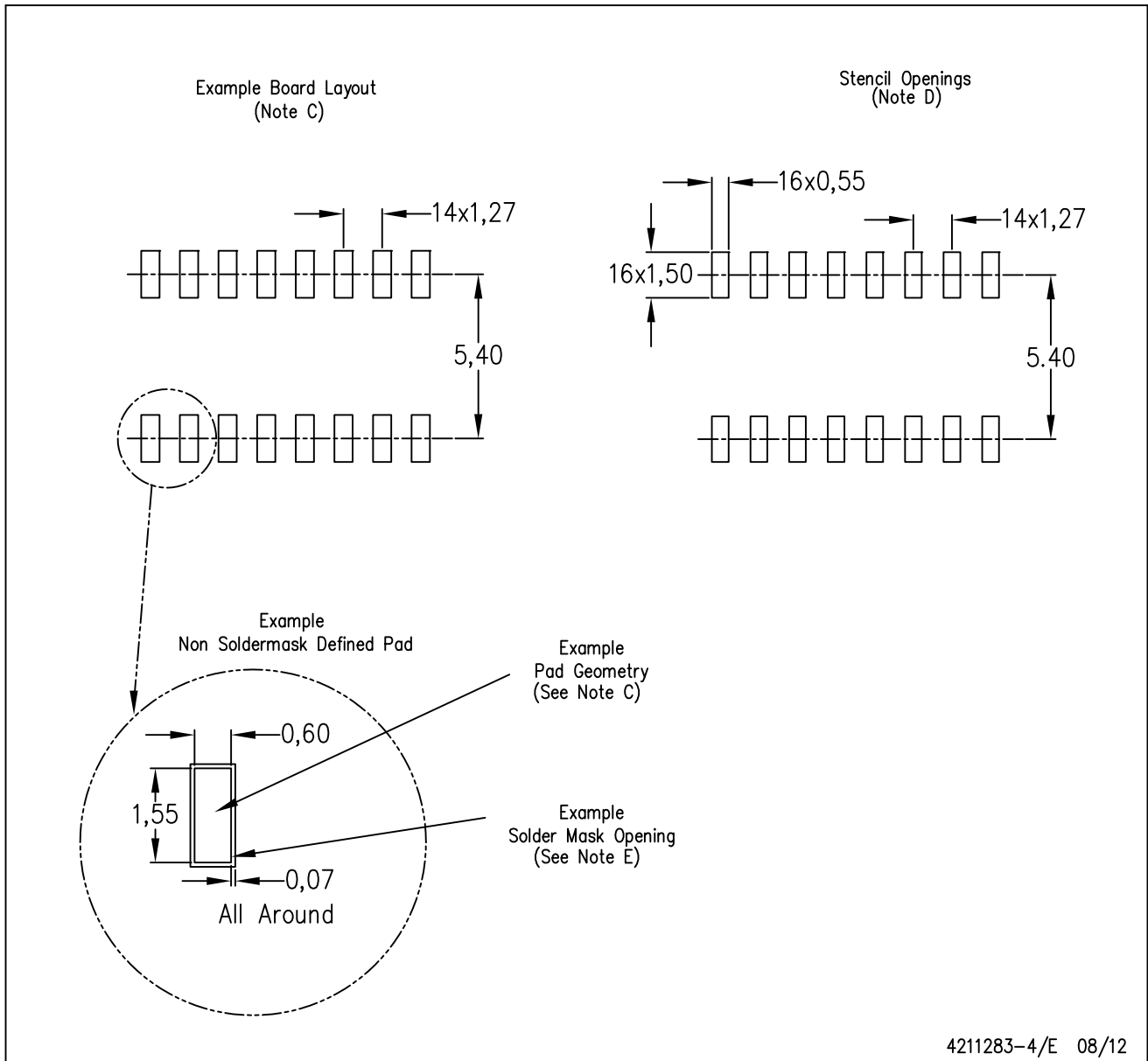


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

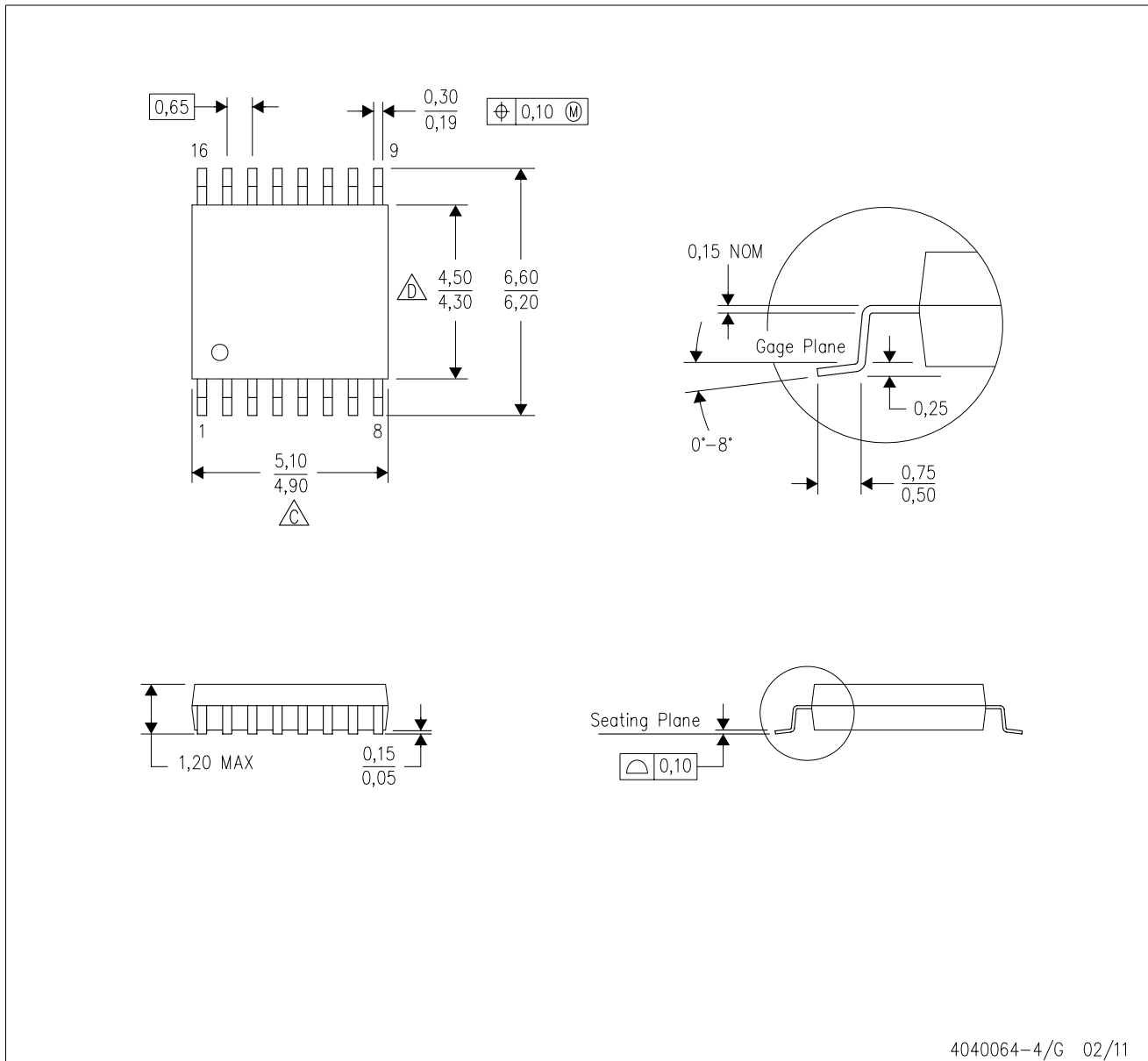


4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

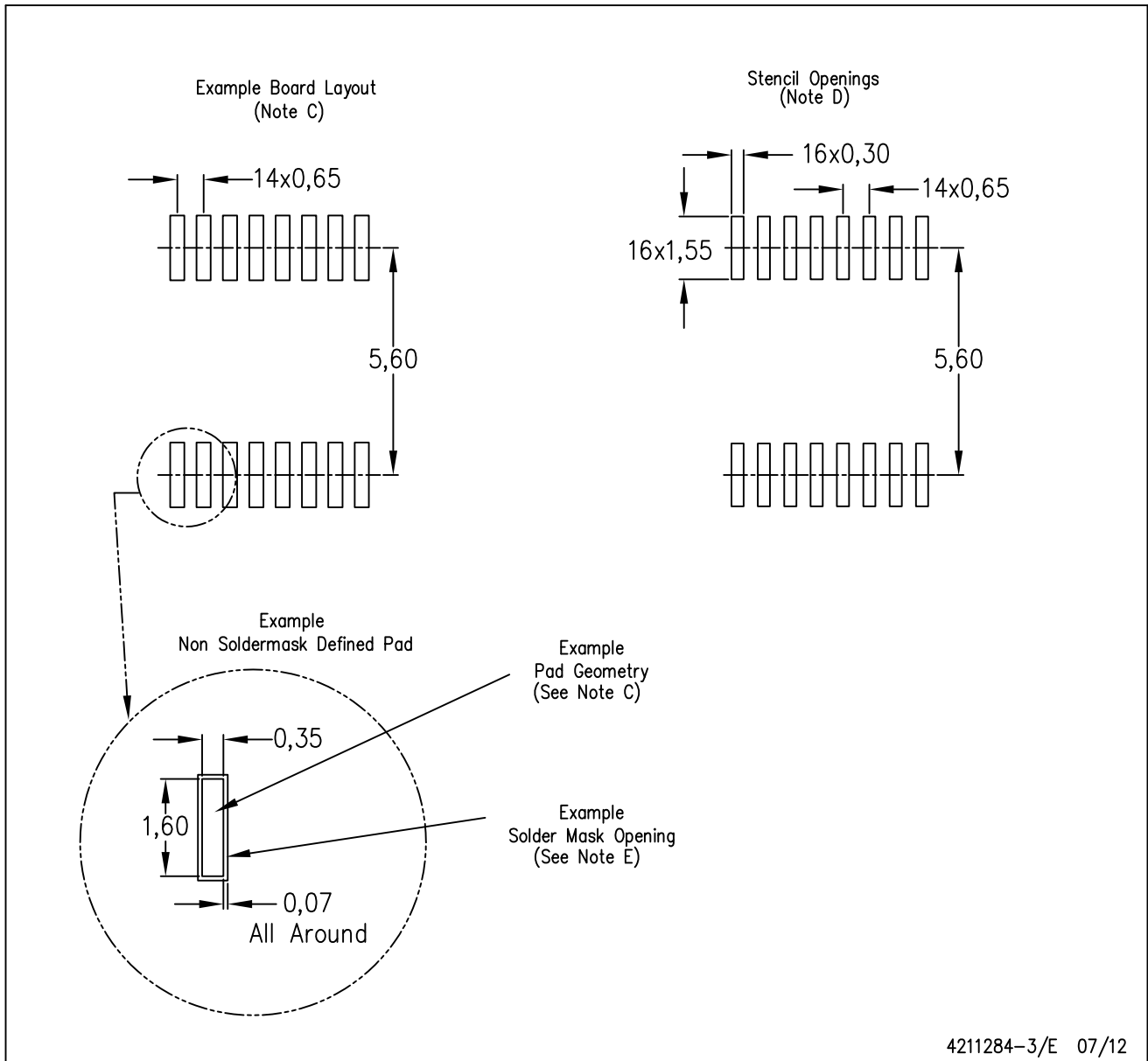


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

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