Dual/Quad Low Power, High Speed JFET Operational Amplifiers

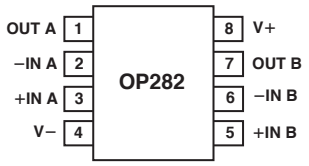
OP282/OP482

FEATURES
High Slew Rate: 9 V/μs
Wide Bandwidth: 4 MHz
Low Supply Current: 250 μA/Amplifier
Low Offset Voltage: 3 mV
Low Bias Current: 100 pA
Fast Settling Time
Common-Mode Range Includes V+
Unity Gain Stable

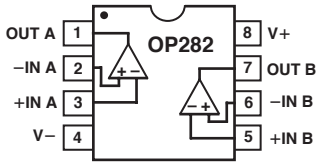
APPLICATIONS
Active Filters
Fast Amplifiers
Integrators
Supply Current Monitoring

PIN CONNECTIONS

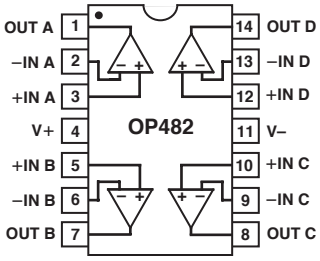
8-Lead Narrow-Body SOIC (S Suffix)



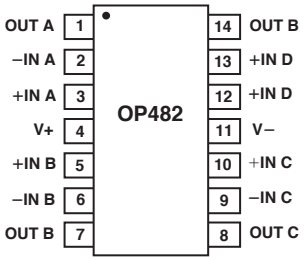
8-Lead Epoxy DIP (P Suffix)



14-Lead Epoxy DIP (P Suffix)



14-Lead Narrow-Body SOIC (S Suffix)



GENERAL DESCRIPTION

The OP282/OP482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. Slew rate exceeds 7 V/μs with supply current under 250 μA per amplifier. These unity gain stable amplifiers have a typical gain bandwidth of 4 MHz.

The JFET input stage of the OP282/OP482 ensures bias current is typically a few picoamps and below 500 pA over the full temperature range. Offset voltage is under 3 mV for the dual and under 4 mV for the quad.

With a wide output swing, within 1.5 V of each supply, low power consumption, and high slew rate, the OP282/OP482 are ideal for battery powered systems or power restricted applications. An input common-mode range that includes the positive supply makes the OP282/OP482 an excellent choice for high-side signal conditioning.

The OP282/OP482 are specified over the extended industrial temperature range. Both dual and quad amplifiers are available in plastic DIP plus SOIC surface mount packages.

REV. C

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Tel: 781/329-4700 **www.analog.com**
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OP282/OP482–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = 25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP282		0.2	3	mV
		OP282, –40 ≤ T_A ≤ +85°C			4.5	mV
	V_{OS}	OP482		0.2	4	mV
		OP482, –40 ≤ T_A ≤ +85°C			6	mV
Input Bias Current	I_B	V_{CM} = 0 V		3	100	pA
		V_{CM} = 0 V, Note 1			500	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	50	pA
		V_{CM} = 0 V, Note 1			250	pA
Input Voltage Range			–11		+15	V
Common-Mode Rejection	CMR	–11 V ≤ V_{CM} ≤ +15 V, –40°C ≤ T_A ≤ +85°C	70	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20			V/mV
		R_L = 10 kΩ, –40°C ≤ T_A ≤ +85°C	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	–13.5	±13.9	13.5	V
Short Circuit Limit	I_{SC}	Source	3	10		mA
		Sink	–8	–12		mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V,				
		–40°C ≤ T_A ≤ +85°C		25	316	µV/V
Supply Current/Amplifier	I_{SY}	V_O = 0 V, 40°C ≤ T_A ≤ 85°C		210	250	µA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	7	9		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	$Ø_O$			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n			0.01		pA/√Hz

NOTE

[1]The input bias and offset currents are tested at $T_A = T_J$ = 85°C. Bias and offset currents are guaranteed but not tested at –40°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Input Voltage[1] . . . . . ±18 V
Differential Input Voltage[1] . . . . . 36 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
P, S Packages . . . . . –65°C to +150°C
Operating Temperature Range
OP282G, OP482G . . . . . –40°C to +85°C
Junction Temperature Range
P, S Packages . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	120	36	°C/W

NOTES
[1]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[2]θ_{JA} is specified for the worst case conditions; i.e., θ_{JA} is specified for device in socket for cerdip, PDIP; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP282GP*	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP282GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP482GP	–40°C to +85°C	14-Pin Plastic DIP	N-14
OP482GS	–40°C to +85°C	14-Pin SOIC	SO-14

*Not for new designs, obsolete April 2002.

For military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

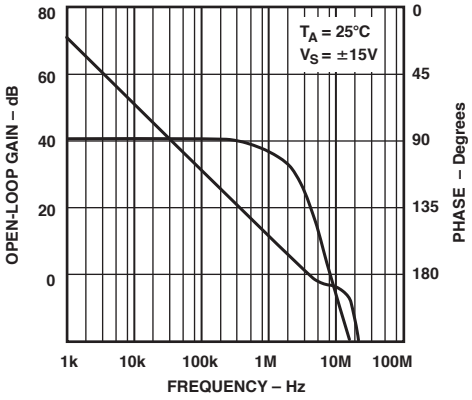
SMD Part Number	ADI Equivalent
5962–9458101M2A*	OP482ARC/883
5962–9458101MCA*	OP482AY/883

*Not for new designs, obsolete April 2002.

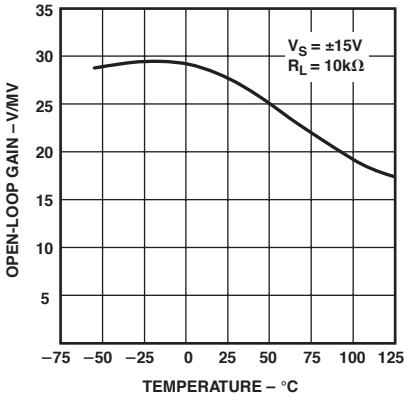
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP282/OP482 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

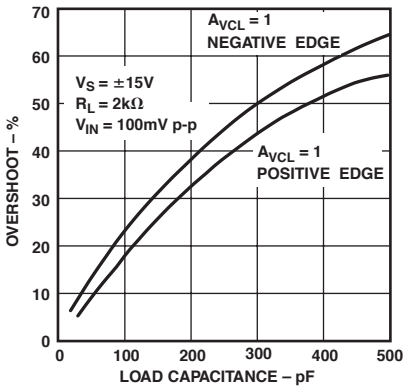
OP282/OP482–Typical Performance Characteristics



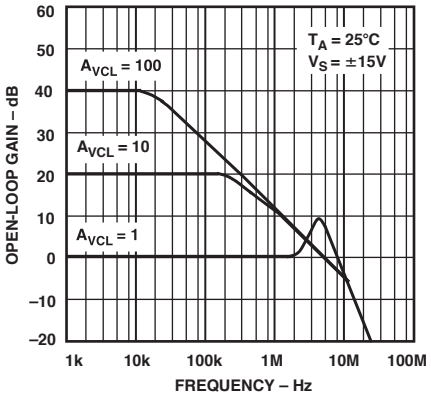
TPC 1. Open-Loop Gain, Phase vs. Frequency



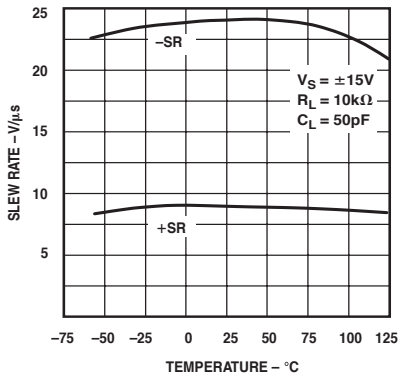
TPC 2. Open-Loop Gain (V/mV)



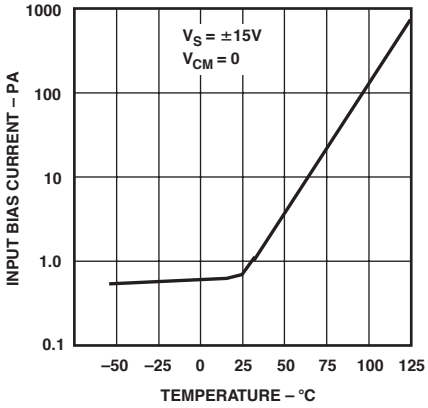
TPC 3. Small Signal Overshoot vs. Load Capacitance



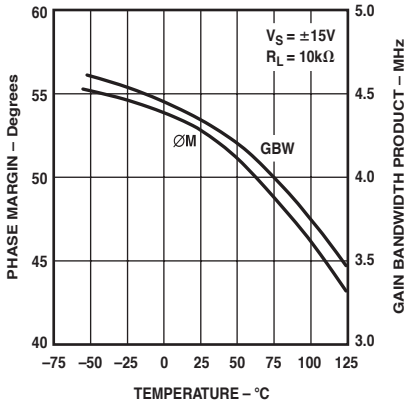
TPC 4. Closed-Loop Gain vs. Frequency



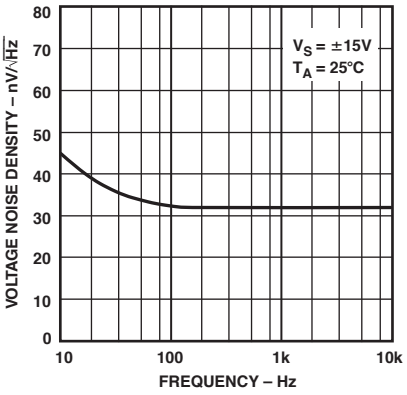
TPC 5. OP282/OP482 Slew Rate vs. Temperature



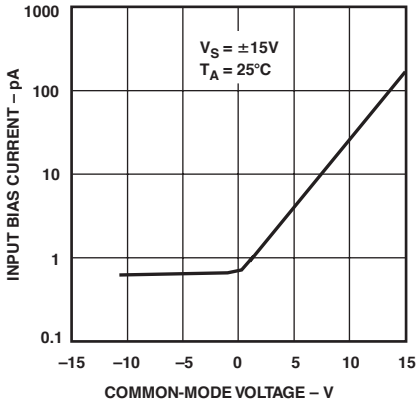
TPC 6. OP282 Input Bias Current vs. Temperature



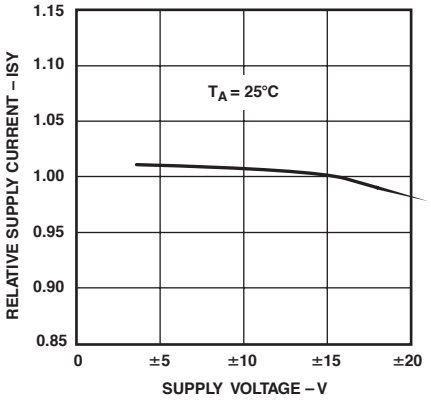
TPC 7. OP482 Phase Margin and Gain Bandwidth Product vs. Temperature



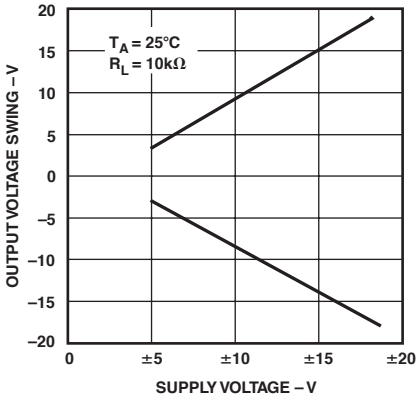
TPC 8. Voltage Noise Density vs. Frequency



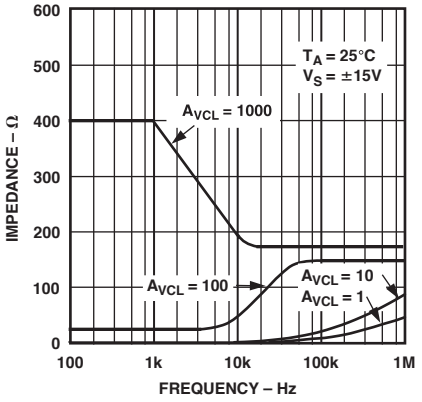
TCP 9. OP282 Input Bias Current vs. Common-Mode Voltage



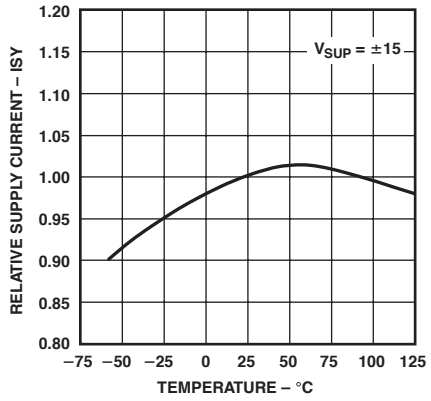
TPC 10. Relative Supply Current vs. Supply Voltage



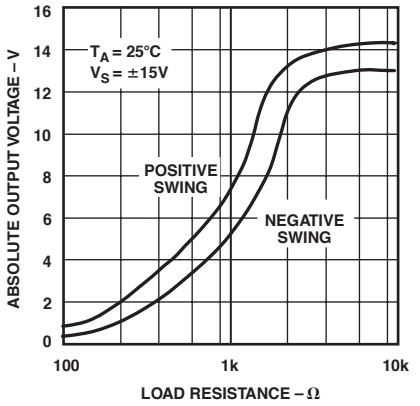
TPC 11. Output Voltage Swing vs. Supply Voltage



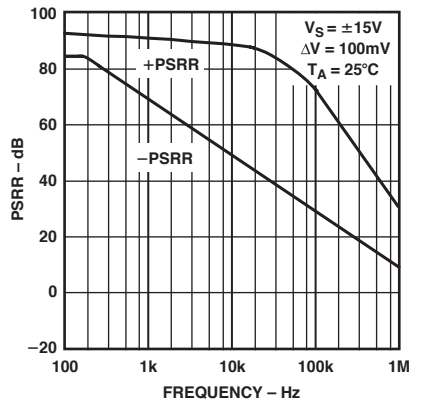
TPC 12. OP482 Closed-Loop Output Impedance vs. Frequency



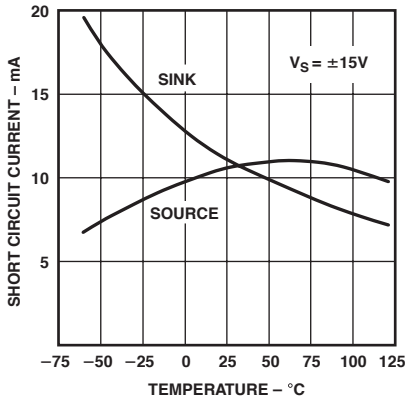
TPC 13. Relative Supply Current vs. Temperature



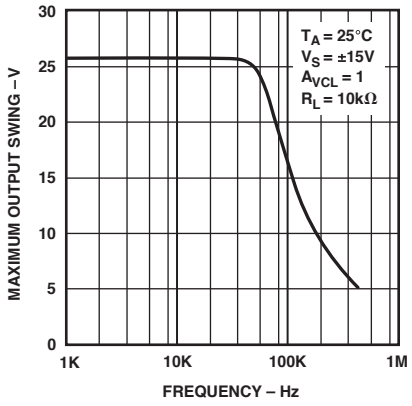
TPC 14. Maximum Output Voltage vs. Load Resistance



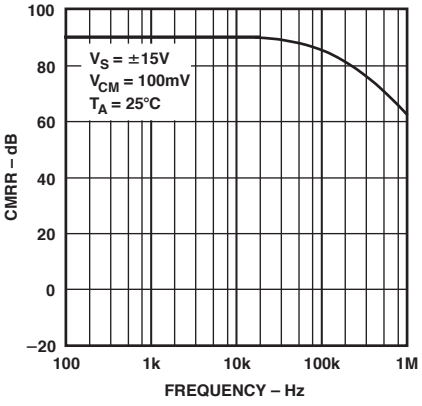
TPC 15. OP282 Power Supply Rejection Ratio (PSRR) vs. Frequency



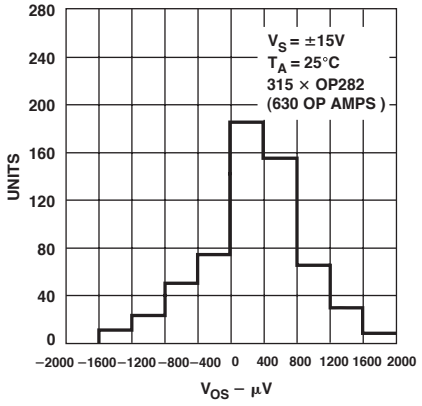
TPC 16. OP282/OP482 Short Circuit Current vs. Temperature



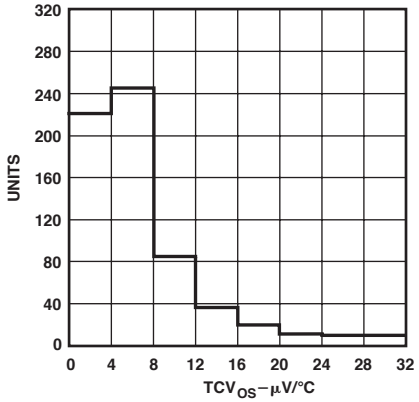
TPC 17. Maximum Output Swing vs. Frequency



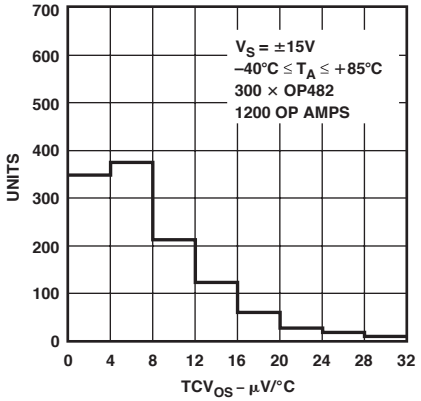
TPC 18. OP282 Common-Mode Rejection Ratio (CMRR) vs. Frequency



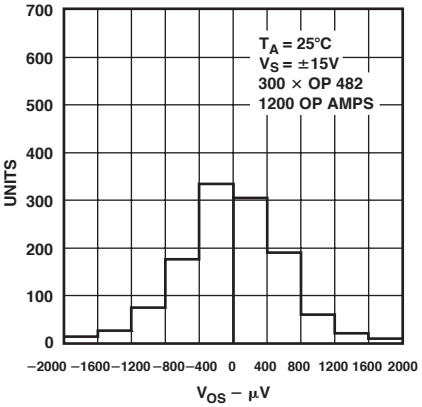
TPC 19. V_{OS} Distribution "P" Package



TPC 20. OP282 TCV_{OS} (µV/°C) Distribution "P" Package



TPC 21. TCV_{OS} Distribution"P" Package



TPC 22. OP482 V_{OS} Distribution "P" Package

APPLICATIONS INFORMATION

The OP282 and OP482 are single and dual JFET op amps that have been optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery powered or low power applications requiring above average performance. Applications benefiting from this performance combination include telecom, geophysical exploration, portable medical equipment, and navigational instrumentation.

HIGH-SIDE SIGNAL CONDITIONING

There are many applications that require the sensing of signals near the positive rail. OP282s and OP482s have been tested and guaranteed over a common-mode range ($-11\ V \le V_{CM} \le +15\ V$) that includes the positive supply.

One application where this is commonly used is in the sensing of power supply currents. This enables it to be used in current sensing applications such as the partial circuit shown in Figure 1. In this circuit, the voltage drop across a low value resistor, such as the 0.1 Ω shown here, is amplified and compared to 7.5 V. The output can then be used for current limiting.

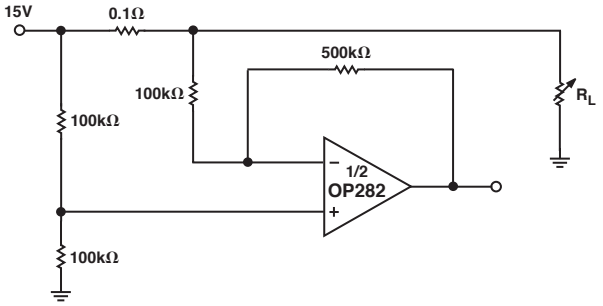


Figure 1. Phase Inversion

PHASE INVERSION

Most JFET-input amplifiers will invert the phase of the input signal if either input exceeds the input common-mode range. For the OP282 and OP482, negative signals in excess of approximately 14 V will cause phase inversion. The cause of this effect is saturation of the input stage leading to the forward-biasing of a drain-gate diode. A simple fix for this in noninverting applications is to place a resistor in series with the noninverting input. This limits the amount of current through the forward-biased diode and prevents the shutting down of the output stage. For the OP282/OP482, a value of 200 kΩ has been found to work. However, this adds a significant amount of noise.

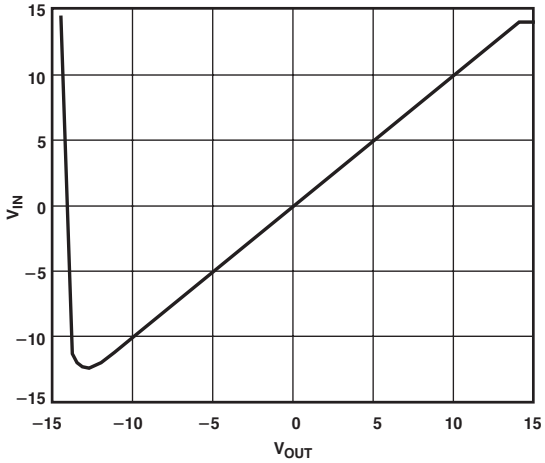


Figure 2. OP282 Phase Reversal

ACTIVE FILTERS

The wide bandwidth and high slew rates of the OP282 and OP482 make either an excellent choice for many filter applications.

There are many types of active filter configurations, but the four most popular configurations are Butterworth, Elliptical, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic as shown in Table I.

Table I.

Type	Selectivity	Overshoot	Phase	Amplitude (Pass Band)	Amplitude (Stop Band)
Butterworth	Moderate	Good		Max Flat	
Chebyshev	Good	Moderate	Nonlinear	Equal Ripple	
Elliptical	Best	Poor		Equal Ripple	Equal Ripple
Bessel (Thompson)	Poor	Best	Linear		

PROGRAMMABLE STATE-VARIABLE FILTER

The circuit shown in Figure 3 can be used to accurately program the "Q," the cutoff frequency f_C, and the gain of a two pole state-variable filter. OP482s have been used in this design because of their high bandwidths, low power, and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

The DACs shown are used in the voltage mode so too many values are dependent only on the accuracy of the DAC and not on the absolute values of the DAC's resistive ladders. This makes this circuit unusually accurate for a programmable filter.

Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation times R1 determines the amount of signal current that charges the integrating capacitor, C1. This cutoff frequency can now be expressed as:

$$fc = \frac{1}{2\pi R_1 C_1}\left(\frac{D_1}{256}\right)$$

where D_1 is the digital code for the DAC.

Gain of this circuit is set by adjusting D_3. The gain equation is:

$$Gain = \frac{R_4}{R_5}\left(\frac{D_3}{256}\right)$$

DAC 2 is used to set the "Q" of the circuit. Adjusting this DAC controls the amount of feedback from the band-pass node to the input summing node. Note that the digital value of the DAC is in the numerator; therefore, zero code is not a valid operating point.

$$Q = \frac{R_2}{R_3}\left(\frac{256}{D_2}\right)$$

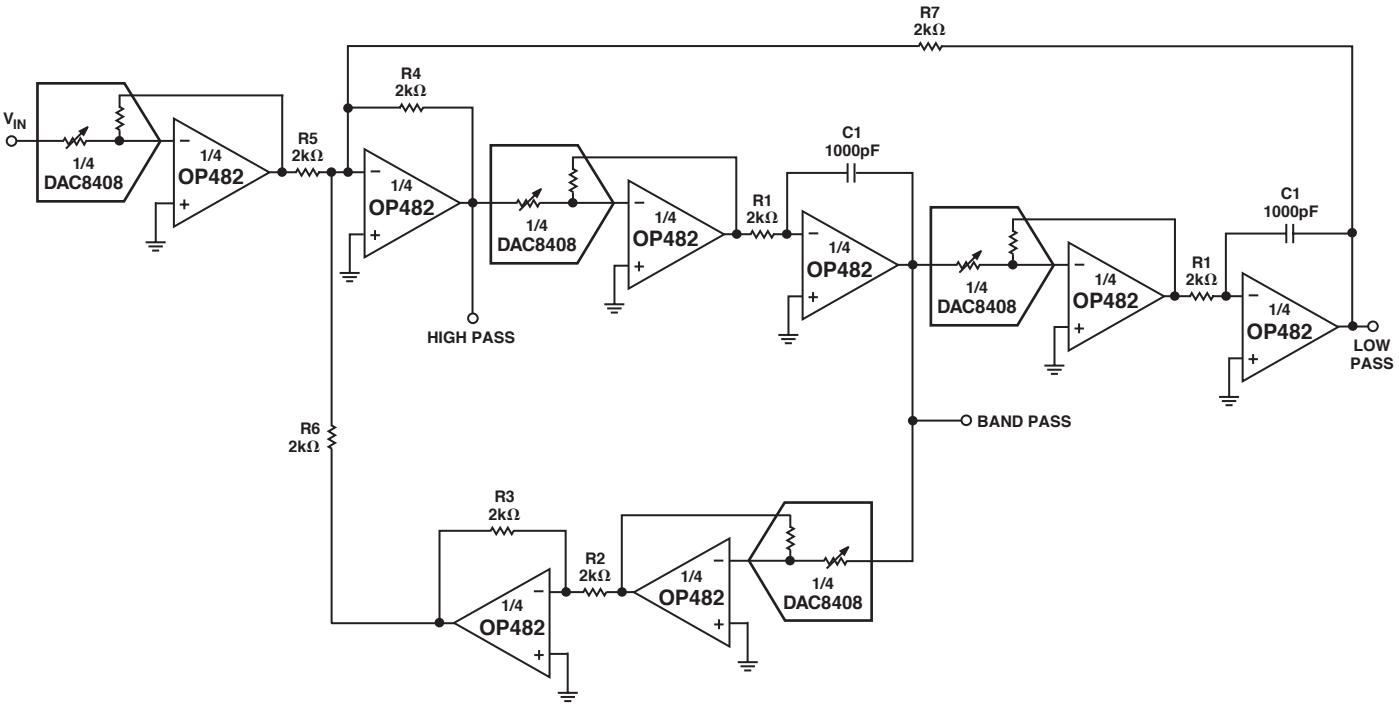


Figure 3.

OP282/OP482 SPICE MACRO MODEL

Figure 4 shows the OP282 SPICE macro model. The model for the OP482 is similar to that of the OP282, but there are some minor changes in the circuit values. Contact ADI for a copy of the latest SPICE model diskette for both listings.

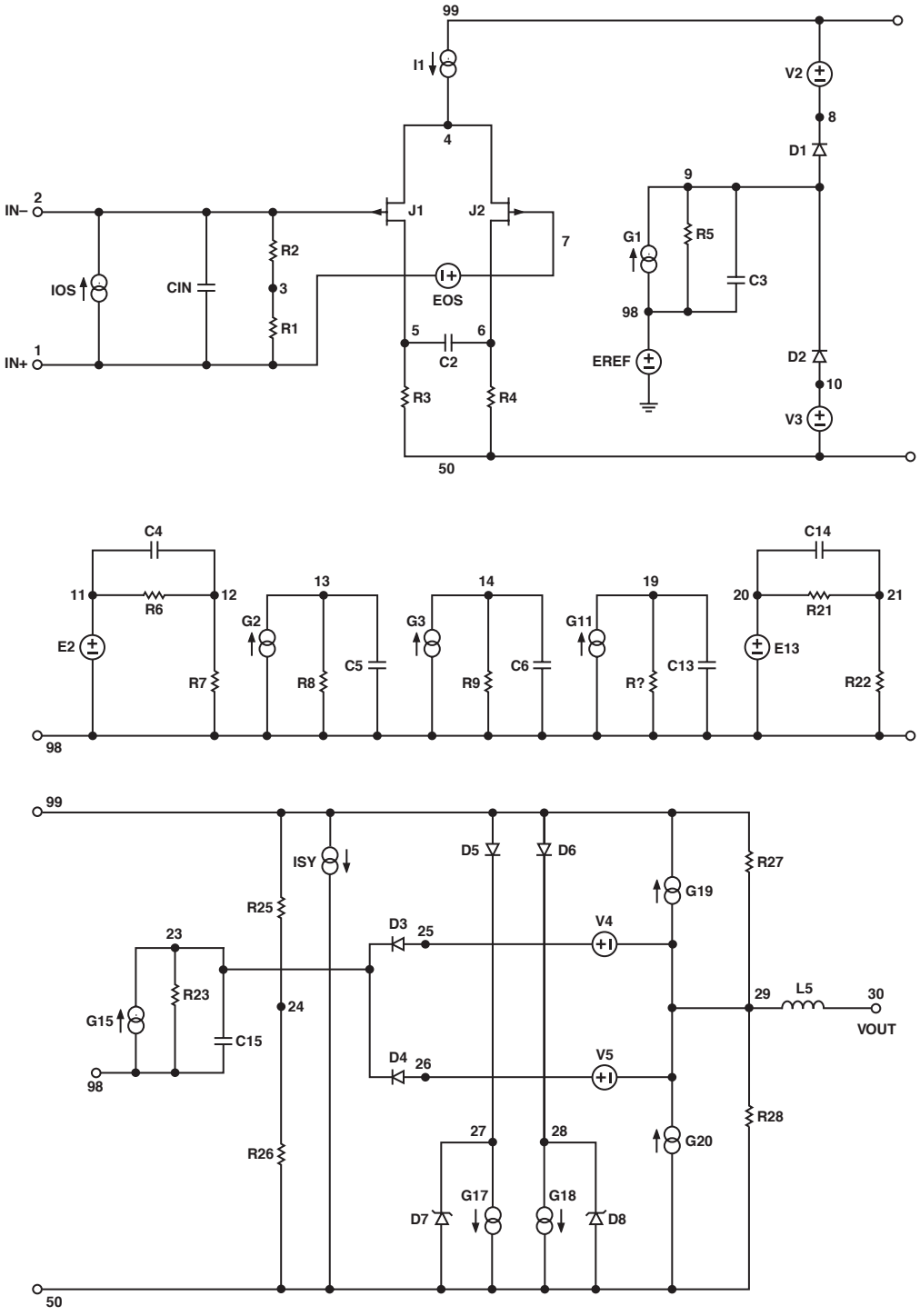


Figure 4.

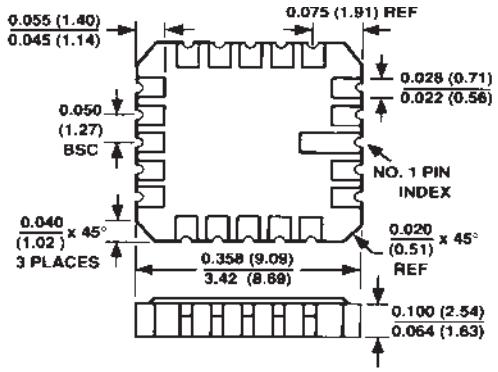
OP282 SPICE MACRO MODEL

```
* Node assignments
*                    noninverting input
*                    |    inverting input
*                    |    |    positive supply
*                    |    |    |    negative supply
*                    |    |    |    |    output
*                    |    |    |    |    |
.SUBCKT OP282        1    2    99   50   30
*
* INPUT STAGE & POLE AT 15 MHZ
*
R1       1    3    5E11
R2       2    3    5E11
R3       5    50   3871.3
R4       6    50   3871.3
CIN      1    2    5E-12
C2       5    6    1.37E-12
I1       99   4    0.1E-3
IOS      1    2    5E-13
EOS      7    1    POLY(1) 21 24 200E-6 1
J1       5    2    4         JX
J2       6    7    4         JX
*
EREF     98   0    24        0 1
*
* GAIN STAGE & POLE AT 124 HZ
*
R5       9    98   1.16E8
C3       9    98   1.11E-11
G1       98   9    5 6       2.58E-4
V2       99   8    1.2
V3       10   50   1.2
D1       9    8    DX
D2       10   9    DX
*
* NEGATIVE ZERO AT 4 MHZ
*
R6       11   12   1E6
R7       12   98   1
C4       11   12   39.8E-15
E2       11   98   9         24 1E6
*
* POLE AT 15 MHZ
*
R8       13   98   1E6
C5       13   98   10.6E-15
G2       98   13   12        24 1E-6
*
* POLE AT 15 MHZ
*
R9       14   98   1E6
C6       14   98   10.6E-15
G3       98   14   13        24 1E-6
*
* POLE AT 15 MHZ
*
R19      19   98   1E6
C13      19   98   10.6E-15
G11      98   19   14        24 1E-6
*
* COMMON-MODE GAIN NETWORK
  WITH ZERO AT 11 KHZ
*
R21      20   21   1E6
R22      21   98   1
C14      20   21   14.38E-12
E13      98   20   3         24 31.62
*
* POLE AT 15 MHZ
*
R23      23   98   1E6
C15      23   98   10.6E-15
G15      98   23   19        24 1E-6
*
* OUTPUT STAGE
*
R25      24   99   5E6
R26      24   50   5E6
ISY      99   50   107E-6
R27      29   99   700
R28      29   50   700
L5       29   30   1E-8
G17      27   50   23        29 1.43E-3
G18      28   50   29        23 1.43E-3
G19      29   99   99        23 1.43E-3
G20      50   29   23        50 1.43E-3
V4       25   29   2.8
V5       29   26   3.5
D3       23   25   DX
D4       26   23   DX
D5       99   27   DX
D6       99   28   DX
D7       50   27   DY
D8       50   28   DY
*
* MODELS USED
*
.MODEL JX PJF(BETA = 3.34E-4
VTO = –2.000 IS = 3E-12)
.MODEL DX D(IS = 1E-15)
.MODEL DY D(IS = 1E-15 BV = 50)
.ENDS OP282
```

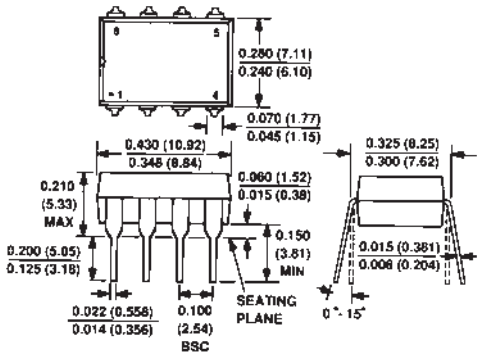
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

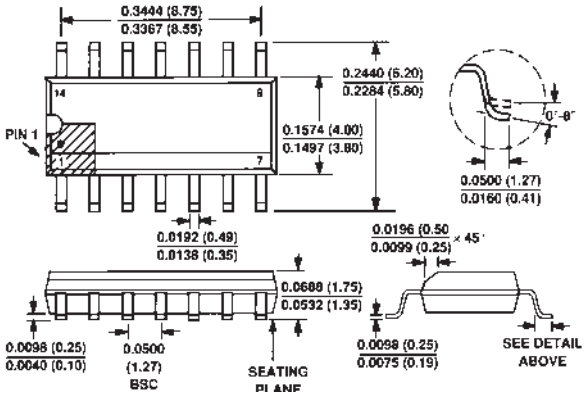
8-Lead Narrow-Body SOIC (S Suffix)



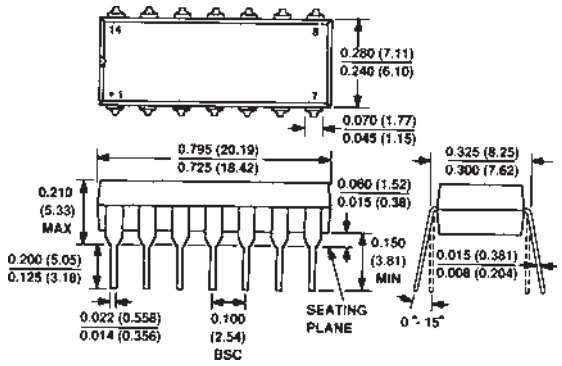
8-Lead Epoxy DIP (P Suffix)



14-Lead Narrow-Body SOIC (S Suffix)



14-Lead Epoxy DIP (P Suffix)



Revision History

Location	Page
Data Sheet changed from REV. B to REV. C.	
Wafer Test Limits deleted	2
Edits to ABSOLUTE MAXIMUM RATINGS	3
Dice Characteristics deleted	3
Edits to ORDERING GUIDE	3
Edits to Figure 1	7
Edits to Figure 3	8
20-Position Chip Carrier (RC Suffix) deleted	11

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