

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74VCXR162245FT****LOW-VOLTAGE 16-BIT BUS TRANSCEIVER  
WITH 3.6V TOLERANT INPUTS AND OUTPUTS**

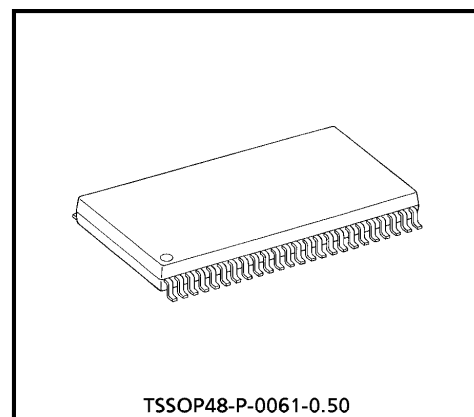
The TC74VCXR162245FT is a high performance CMOS 16-bit BUS TRANSCEIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6V.

This 16bit bus transceiver is controlled by direction control (DIR) inputs and output enable ( $\overline{OE}$ ) inputs which are common to each byte. It can be used as two 8-bit transceivers or one 16-bit transceiver. The direction of data transmission is determined by the level of the DIR inputs. The  $\overline{OE}$  inputs can be used to disable the device so that the busses are effectively isolated.

The 26- $\Omega$  series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge.



TSSOP48-P-0061-0.50

Weight : 0.25g (Typ.)

**FEATURES**

- 26- $\Omega$  Series Resistors on all Outputs.
- Low Voltage Operation :  $V_{CC} = 1.8\sim 3.6V$
- High Speed Operation :  $t_{pd} = 3.4ns$  (max.) at  $V_{CC} = 3.0\sim 3.6V$   
:  $t_{pd} = 4.3ns$  (max.) at  $V_{CC} = 2.3\sim 2.7V$   
:  $t_{pd} = 5.7ns$  (max.) at  $V_{CC} = 1.8V$
- 3.6V Tolerant inputs and outputs.
- Output Current :  $I_{OH}/I_{OL} = \pm 12mA$  (min.) at  $V_{CC} = 3.0V$   
:  $I_{OH}/I_{OL} = \pm 8mA$  (min.) at  $V_{CC} = 2.3V$   
:  $I_{OH}/I_{OL} = \pm 4mA$  (min.) at  $V_{CC} = 1.8V$
- Latch-up Performance :  $\pm 300mA$
- ESD Performance : Human Body Model  $> \pm 2000V$   
: Machine Model  $> \pm 200V$
- Package : TSSOP (Thin Shrink Small Outline Package)
- Bidirectional interface between 2.5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs
- Supports live insertion / withdrawal (Note 3)

Note 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

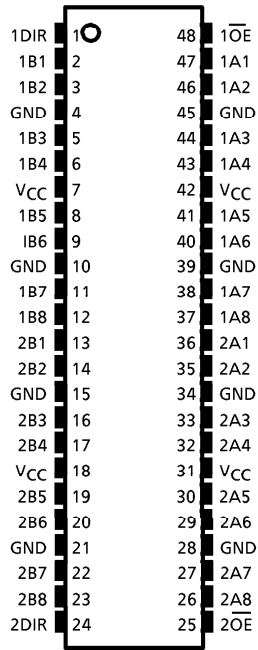
2) All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.

3) To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

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**PIN CONNECTION**



(TOP VIEW)

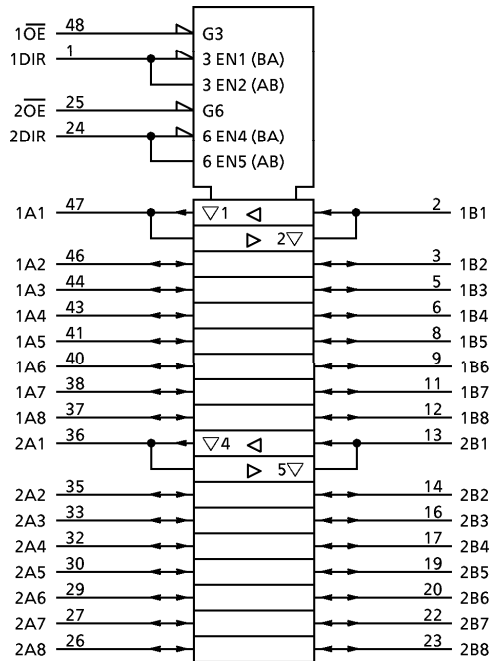
**TRUTH TABLE**

INPUT		FUNCTION		OUTPUT
$\overline{1OE}$	1DIR	BUS 1A1-1A8	BUS 1B1-1B8	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

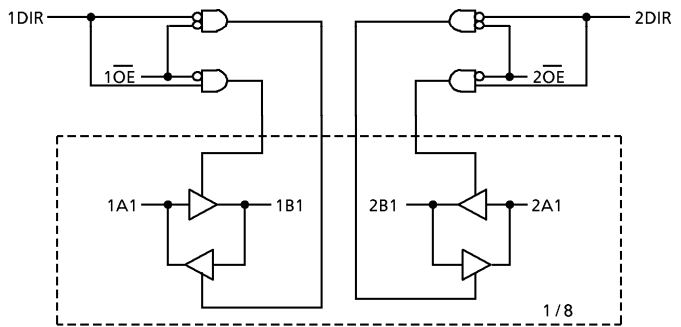
INPUT		FUNCTION		OUTPUT
$\overline{2OE}$	2DIR	BUS 2A1-2A8	BUS 2B1-2B8	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	High Impedance		Z

X : Don't Care  
Z : High impedance

**IEC LOGIC SYMBOL**



**SYSTEM DIAGRAM**



980508EBA2'

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## MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	$V_{CC}$	-0.5~4.6	V
DC Input Voltage (DIR, $\overline{OE}$ )	$V_{IN}$	-0.5~4.6	V
DC Bus I/O Voltage	$V_{I/O}$	-0.5~4.6 (Note 1)	V
		-0.5~ $V_{CC}$ +0.5 (Note 2)	
Input Diode Current	$I_{IK}$	-50	mA
Output Diode Current	$I_{OK}$	$\pm 50$ (Note 3)	mA
DC Output Current	$I_{OUT}$	$\pm 50$	mA
Power Dissipation	$P_D$	400	mW
DC $V_{CC}$ /Ground Current Per Supply Pin	$I_{CC}/I_{GND}$	$\pm 100$	mA
Storage Temperature	$T_{stg}$	-65~150	$^{\circ}C$

(Note 1) Off-State

(Note 2) High or Low State.  $I_{OUT}$  absolute maximum rating must be observed.

(Note 3)  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

## RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}$	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage (DIR, $\overline{OE}$ )	$V_{IN}$	-0.3~3.6	V
Bus I/O Voltage	$V_{I/O}$	0~3.6 (Note 5)	V
		0~ $V_{CC}$ (Note 6)	
Output Current	$I_{OH}/I_{OL}$	$\pm 12$ (Note 7)	mA
		$\pm 8$ (Note 8)	
		$\pm 4$ (Note 9)	
Operating Temperature	$T_{opr}$	-40~85	$^{\circ}C$
Input Rise And Fall Time	$dt/dv$	0~10 (Note 10)	ns/V

(Note 4) Data Retention Only

(Note 5) Off-State

(Note 6) High or Low State

(Note 7)  $V_{CC} = 3.0\sim 3.6V$

(Note 8)  $V_{CC} = 2.3\sim 2.7V$

(Note 9)  $V_{CC} = 1.8V$

(Note 10)  $V_{IN} = 0.8\sim 2.0V$ ,  $V_{CC} = 3.0V$

**ELECTRICAL CHARACTERISTICS**

DC characteristics (Ta = -40~85°C, 2.7V < VCC ≤ 3.6V)

PARAMETER		SYMBOL	TEST CONDITION		VCC (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V <sub>IH</sub>			2.7~3.6	2.0	—	V
	"L" Level	V <sub>IL</sub>			2.7~3.6	—	0.8	
Output Voltage	"H" Level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100μA	2.7~3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -6mA	2.7	2.2	—	
				I <sub>OH</sub> = -8mA	3.0	2.4	—	
				I <sub>OH</sub> = -12mA	3.0	2.2	—	
	"L" Level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100μA	2.7~3.6	—	0.2	
				I <sub>OL</sub> = 6mA	2.7	—	0.4	
				I <sub>OL</sub> = 8mA	3.0	—	0.55	
				I <sub>OL</sub> = 12mA	3.0	—	0.8	
Input Leakage Current		I <sub>IN</sub>	V <sub>IN</sub> = 0~3.6V		2.7~3.6	—	± 5.0	μA
3-State Output Off-State Current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0~3.6V		2.7~3.6	—	± 10.0	μA
Power Off Leakage Current		I <sub>OFF</sub>	V <sub>IN</sub> , V <sub>OUT</sub> = 0~3.6V		0	—	10.0	μA
Quiescent Supply Current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7~3.6	—	20.0	μA
			V <sub>CC</sub> ≤ (V <sub>IN</sub> , V <sub>OUT</sub> ) ≤ 3.6V		2.7~3.6	—	± 20.0	
Increase In I <sub>CC</sub> Per Input		ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		2.7~3.6	—	750	μA

## ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C, 2.3V ≤ V<sub>CC</sub> ≤ 2.7V)

PARAMETER		SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	MIN.	MAX.	UNIT	
Input Voltage	"H" Level	V <sub>IH</sub>		2.3~2.7	1.6	—	V	
	"L" Level	V <sub>IL</sub>		2.3~2.7	—	0.7		
Output Voltage	"H" Level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.3~2.7	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -4mA	2.3	2.0	—	
				I <sub>OH</sub> = -6mA	2.3	1.8	—	
				I <sub>OH</sub> = -8mA	2.3	1.7	—	
	"L" Level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.3~2.7	—	0.2	
				I <sub>OL</sub> = 6mA	2.3	—	0.4	
				I <sub>OL</sub> = 8mA	2.3	—	0.6	
Input Leakage Current		I <sub>IN</sub>	V <sub>IN</sub> = 0~3.6V	2.3~2.7	—	± 5.0	μA	
3-State Output Off-State Current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0~3.6V	2.3~2.7	—	± 10.0	μA	
Power Off Leakage Current		I <sub>OFF</sub>	V <sub>IN</sub> , V <sub>OUT</sub> = 0~3.6V	0	—	10.0	μA	
Quiescent Supply Current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	2.3~2.7	—	20.0	μA	
			V <sub>CC</sub> ≤ (V <sub>IN</sub> , V <sub>OUT</sub> ) ≤ 3.6V <sub>CC</sub>	2.3~2.7	—	± 20.0		

**ELECTRICAL CHARACTERISTICS**

DC characteristics (Ta = -40~85°C, 1.8V ≤ VCC < 2.3V)

PARAMETER		SYMBOL	TEST CONDITION		VCC (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V <sub>IH</sub>			1.8~2.3	0.7 × V <sub>CC</sub>	—	V
	"L" Level	V <sub>IL</sub>			1.8~2.3	—	0.2 × V <sub>CC</sub>	
Output Voltage	"H" Level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100μA	1.8	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -4mA	1.8	1.4	—	
	"L" Level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100μA	1.8	—	0.2	
				I <sub>OL</sub> = 4mA	1.8	—	0.3	
Input Leakage Current		I <sub>IN</sub>	V <sub>IN</sub> = 0~3.6V		1.8	—	± 5.0	μA
3-State Output Off-State Current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0~3.6V		1.8	—	± 10.0	μA
Power Off Leakage Current		I <sub>OFF</sub>	V <sub>IN</sub> , V <sub>OUT</sub> = 0~3.6V		0	—	10.0	μA
Quiescent Supply Current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		1.8	—	20.0	μA
			V <sub>CC</sub> ≤ (V <sub>IN</sub> , V <sub>OUT</sub> ) ≤ 3.6V		1.8	—	± 20.0	

AC characteristics (Ta = -40~85°C, Input t<sub>r</sub> = t<sub>f</sub> = 2.0ns, C<sub>L</sub> = 30pF, R<sub>L</sub> = 500Ω)

PARAMETER		SYMBOL	TEST CONDITION		VCC (V)	MIN.	MAX.	UNIT
Propagation Delay Time	t <sub>pLH</sub> t <sub>pHL</sub>	(Fig.1, 2)			1.8	1.5	5.7	ns
					2.5 ± 0.2	1.0	4.3	
					3.3 ± 0.3	0.8	3.4	
3-State Output Enable Time	t <sub>pZL</sub> t <sub>pZH</sub>	(Fig.1, 3)			1.8	1.5	7.6	ns
					2.5 ± 0.2	1.0	5.7	
					3.3 ± 0.3	0.8	4.2	
3-State Output Disable Time	t <sub>pLZ</sub> t <sub>pHZ</sub>	(Fig.1, 3)			1.8	1.5	5.7	ns
					2.5 ± 0.2	1.0	4.8	
					3.3 ± 0.3	0.8	4.1	
Output To Output Skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 11)			1.8	—	0.5	ns
					2.5 ± 0.2	—	0.5	
					3.3 ± 0.3	—	0.5	

For C<sub>L</sub> = 50pF, add approximately 300ps to the AC maximum specification.

(Note 11) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic switching characteristics (Ta = 25°C, Input tr = tf = 2.0ns, CL = 30pF)

PARAMETER	SYMBOL	TEST CONDITION	VCC (V)	TYP.	UNIT
Quiet Output Maximum Dynamic VOL	VOLP	VIH = 1.8V, VIL = 0V (Note 12)	1.8	0.15	V
		VIH = 2.5V, VIL = 0V (Note 12)	2.5	0.25	
		VIH = 3.3V, VIL = 0V (Note 12)	3.3	0.35	
Quiet Output Minimum Dynamic VOL	VOLV	VIH = 1.8V, VIL = 0V (Note 12)	1.8	-0.15	V
		VIH = 2.5V, VIL = 0V (Note 12)	2.5	-0.25	
		VIH = 3.3V, VIL = 0V (Note 12)	3.3	-0.35	
Quiet Output Minimum Dynamic VOH	VOHV	VIH = 1.8V, VIL = 0V (Note 12)	1.8	1.55	V
		VIH = 2.5V, VIL = 0V (Note 12)	2.5	2.05	
		VIH = 3.3V, VIL = 0V (Note 12)	3.3	2.65	

(Note 12) Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

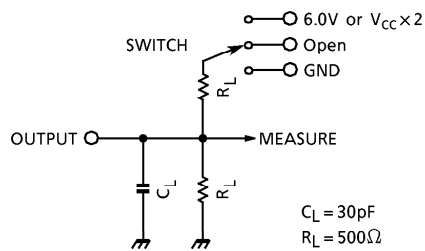
PARAMETER	SYMBOL	TEST CONDITION	VCC (V)	TYP.	UNIT
Input Capacitance	CIN	DIR, $\overline{OE}$	1.8, 2.5, 3.3	6	pF
Bus I/O Capacitance	CI/O	An, Bn	1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	CPD	fIN = 10MHz (Note 13)	1.8, 2.5, 3.3	20	pF

(Note 13) CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16 \text{ (per bit)}$$

Fig.1 Test circuit



PARAMETER	SWITCH
$t_{pLH}, t_{pHL}$	Open
$t_{pLZ}, t_{pZL}$	6.0V @ $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ @ $V_{CC} = 2.5 \pm 0.2V$ @ $V_{CC} = 1.8V$
$t_{pHZ}, t_{pZH}$	GND

**AC WAVEFORM**

Fig.2  $t_{pLH}, t_{pHL}$

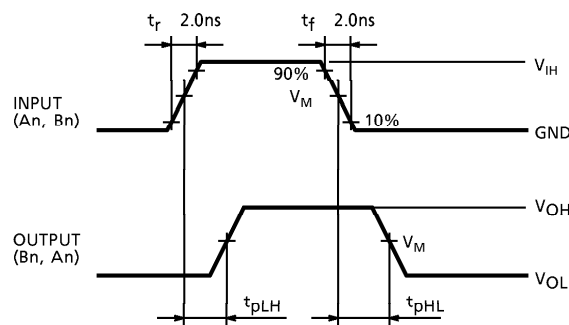
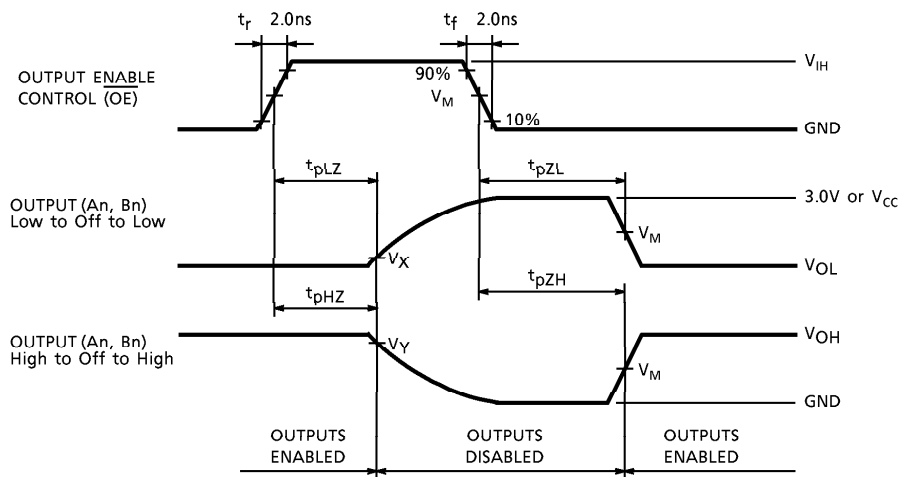


Fig.3  $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$



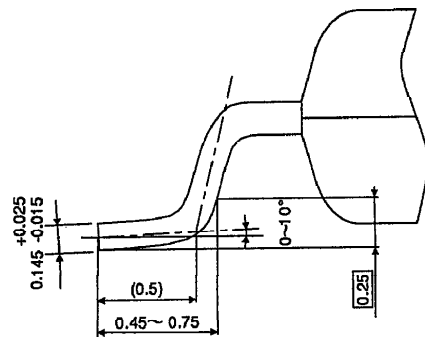
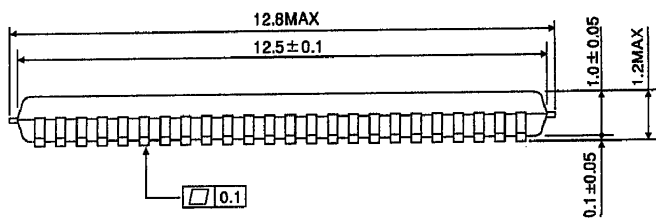
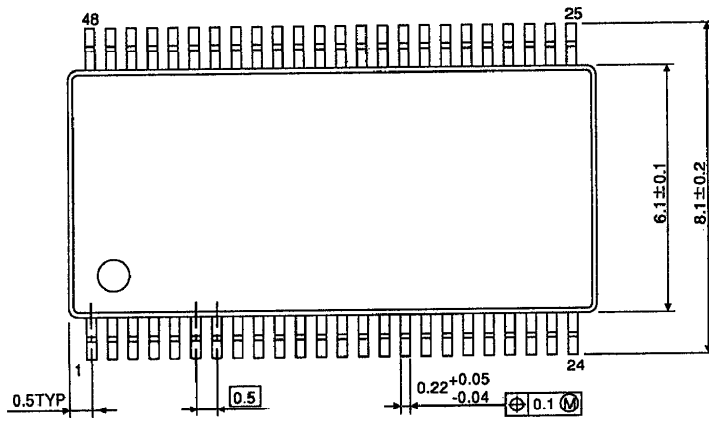
SYMBOL	$V_{CC}$		
	$3.3 \pm 0.3V$	$2.5 \pm 0.2V$	$1.8V$
$V_{IH}$	$2.7V$	$V_{CC}$	$V_{CC}$
$V_M$	$1.5V$	$V_{CC} / 2$	$V_{CC} / 2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$



**OUTLINE DRAWING**

TSSOP48-P-0061-0.50

Unit : mm



Weight : 0.25g (Typ.)