

TC74HC4094AP, TC74HC4094AF, TC74HC4094AFN

8-BIT SHIFT AND STORE REGISTER (3-STATE)

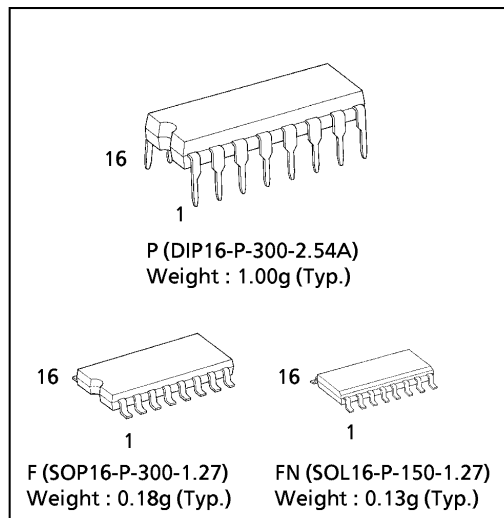
The TC74HC4094A is a high speed CMOS 8-BIT SHIFT AND STROBE REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It consists of an 8-bit shift register and an 8-bit latch with 3-state output buffers. Data is shifted serially through the shift register on the positive going transition of the CK input. The output of the last stage (Q_s) can be used to cascade several devices. Data on the Q_s output is transferred to a second output (Q's) on the following negative transition of the CK input. The data in each stage of the shift register is provided to a corresponding latch, on the negative going transition of the STROBE input. When STROBE is held high, data propagates through the latch to a 3-state output buffer. This buffer is enabled when OUTPUT ENABLE input is set high. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

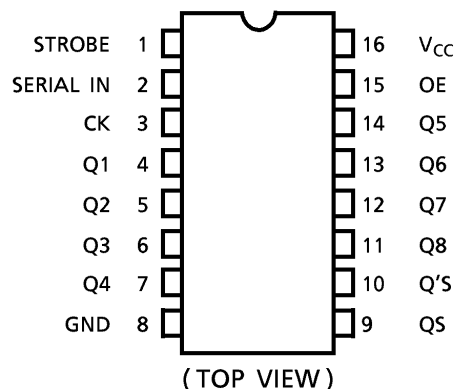
FEATURES:

- High Speed..... $f_{MAX} = 73\text{MHz}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Output Drive Capability 10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 4094B

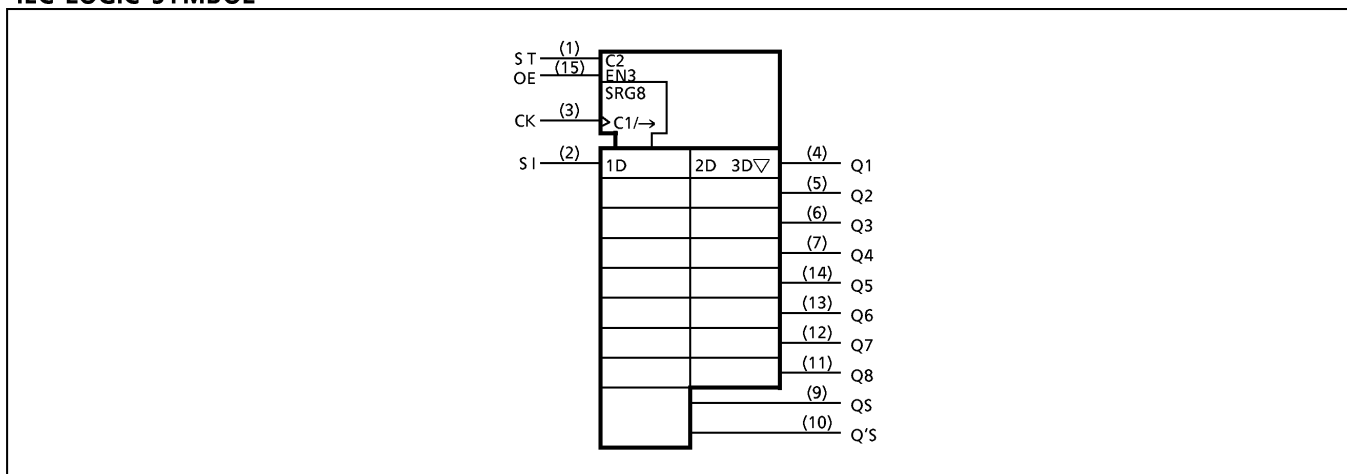
(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



IEC LOGIC SYMBOL



980508EBA2

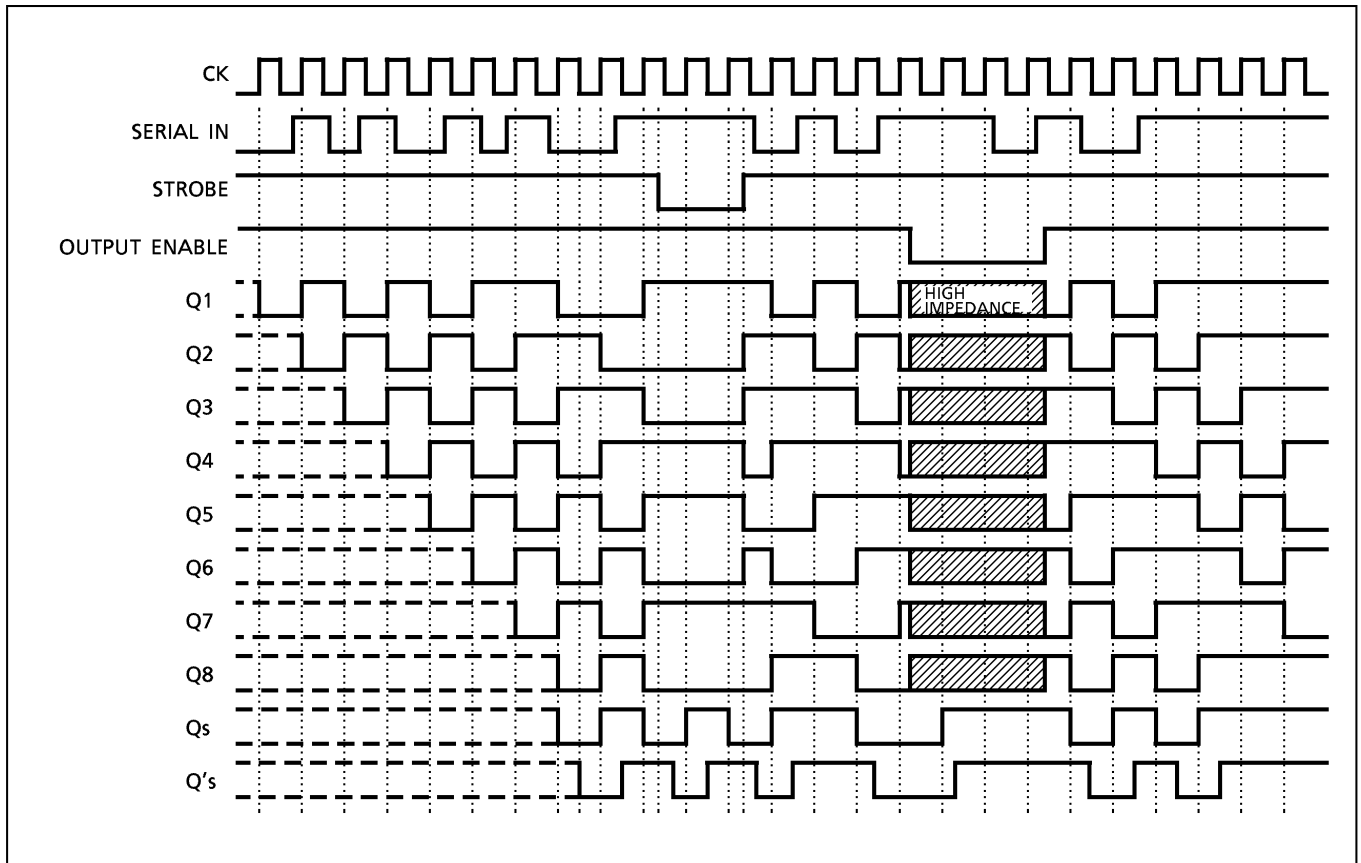
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TRUTH TABLE

CK	OE	ST	SI	PARA. OUT		SERI. OUT	
				Q ₁	Q _n	Q _s	Q' _s
	H	H	L	L	Q _{n-1}	Q ₇	NC
	H	H	H	H	Q _{n-1}	Q ₇	NC
	H	L	*	NC	NC	Q ₇	NC
	L	*	*	Z	Z	Q ₇	NC
	H	*	*	NC	NC	NC	Q _s
	L	*	*	Z	Z	NC	Q _s

X : DON'T CARE
 NC : NO CHANGE
 Z : HIGH IMPEDANCE

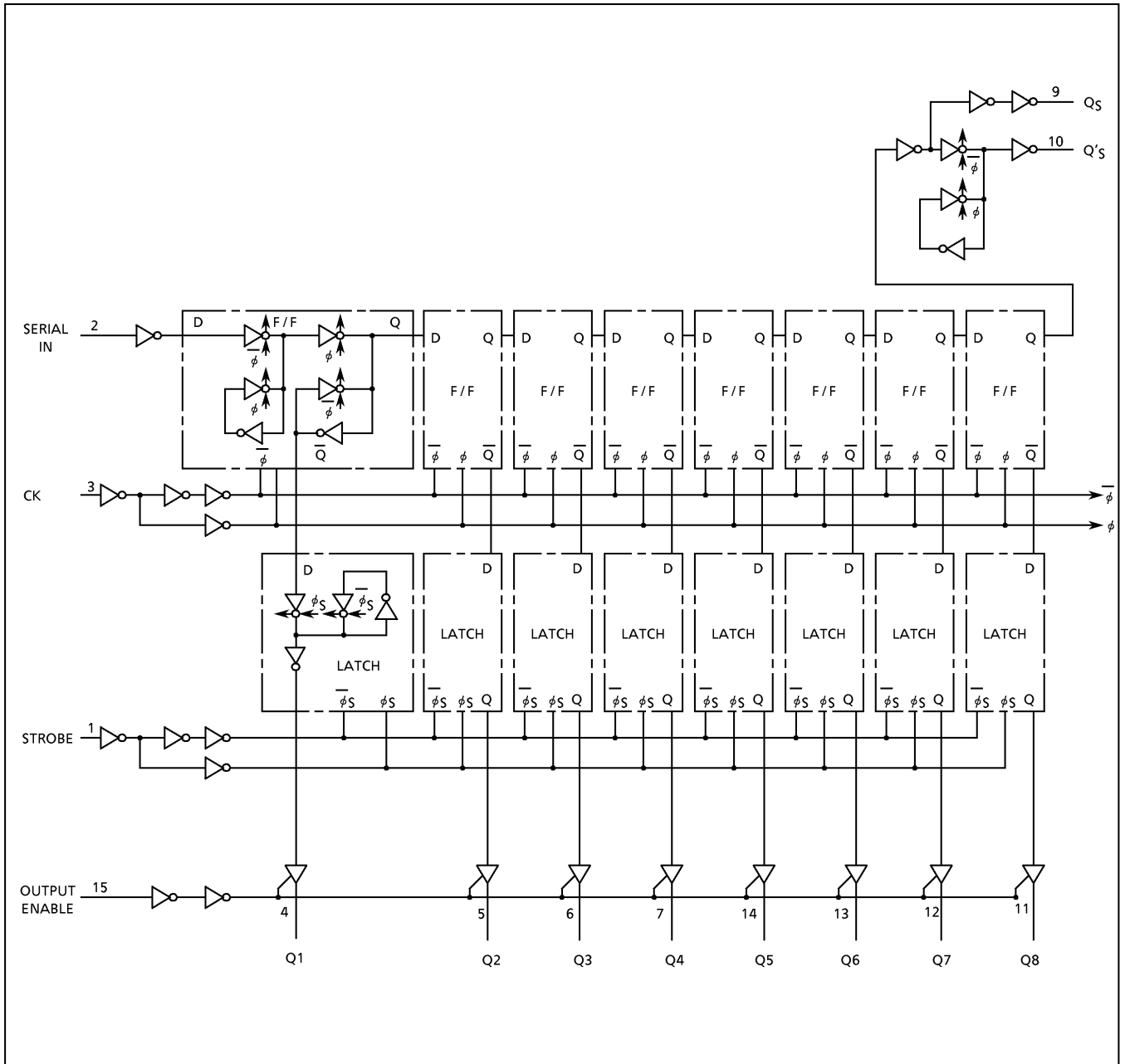
TIMING CHART



980508EBA2'

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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC} = 2.0\text{V}$) 0~500 ($V_{CC} = 4.5\text{V}$) 0~400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
		4.5	$I_{OH} = -4\text{ mA}$ $I_{OH} = -5.2\text{ mA}$	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
		4.5	$I_{OL} = 4\text{ mA}$ $I_{OL} = 5.2\text{ mA}$	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	6.0	—	—	± 0.5	—	± 5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0		

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$		$T_a = -40\sim 85^\circ\text{C}$	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width (STROBE)	$t_{W(H)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (SERIAL)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (STROBE)	t_s		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Hold Time (SERIAL)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Hold Time (STROBE)	t_h		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	30	24	
			6.0	—	35	28	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CK—Qn)	t_{pLH} t_{pHL}		—	22	35	
Propagation Delay Time (CK—QS, Q'S)	t_{pLH} t_{pHL}		—	16	25	
Propagation Delay Time (STROBE—Qn)	t_{pLH} t_{pHL}		—	16	27	
3-State Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1\text{K}\Omega$	—	13	25	
Maximum Clock Frequency	f_{MAX}		33	73	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		UNIT	
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (CK—Qn)	t_{pLH} t_{pHL}		2.0	—	92	200	—	250	
			4.5	—	26	40	—	50	
			6.0	—	20	34	—	43	
Propagation Delay Time (CK—QS, Q'S)	t_{pLH} t_{pHL}		2.0	—	65	150	—	190	
			4.5	—	19	30	—	38	
			6.0	—	15	26	—	32	
Propagation Delay Time (STROBE—Qn)	t_{pLH} t_{pHL}		2.0	—	75	160	—	200	
			4.5	—	20	32	—	40	
			6.0	—	16	27	—	34	
3-State Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1\text{K}\Omega$	2.0	—	58	150	—	190	
			4.5	—	16	30	—	38	
			6.0	—	13	26	—	32	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1\text{K}\Omega$	2.0	—	35	150	—	190	
			4.5	—	16	30	—	38	
			6.0	—	13	26	—	32	
Maximum Clock Frequency	f_{MAX}		2.0	6	16	—	5	—	MHz
			4.5	30	66	—	24	—	
			6.0	35	80	—	28	—	
Input Capacitance	C_{IN}		—	5	10	—	10	pF	
Bus Input Capacitance	C_{OUT}		—	10	—	—	—		
Power Dissipation Capacitance	C_{PD} (1)		—	140	—	—	—		

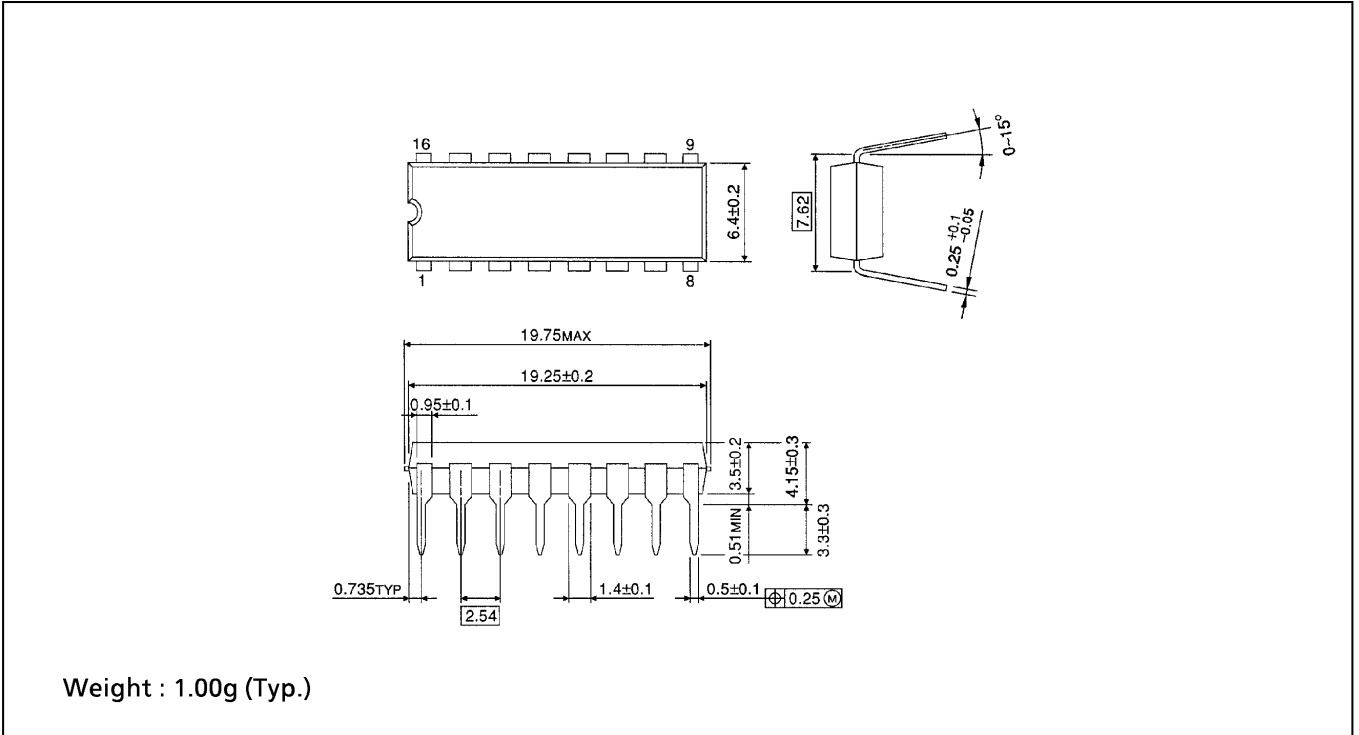
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

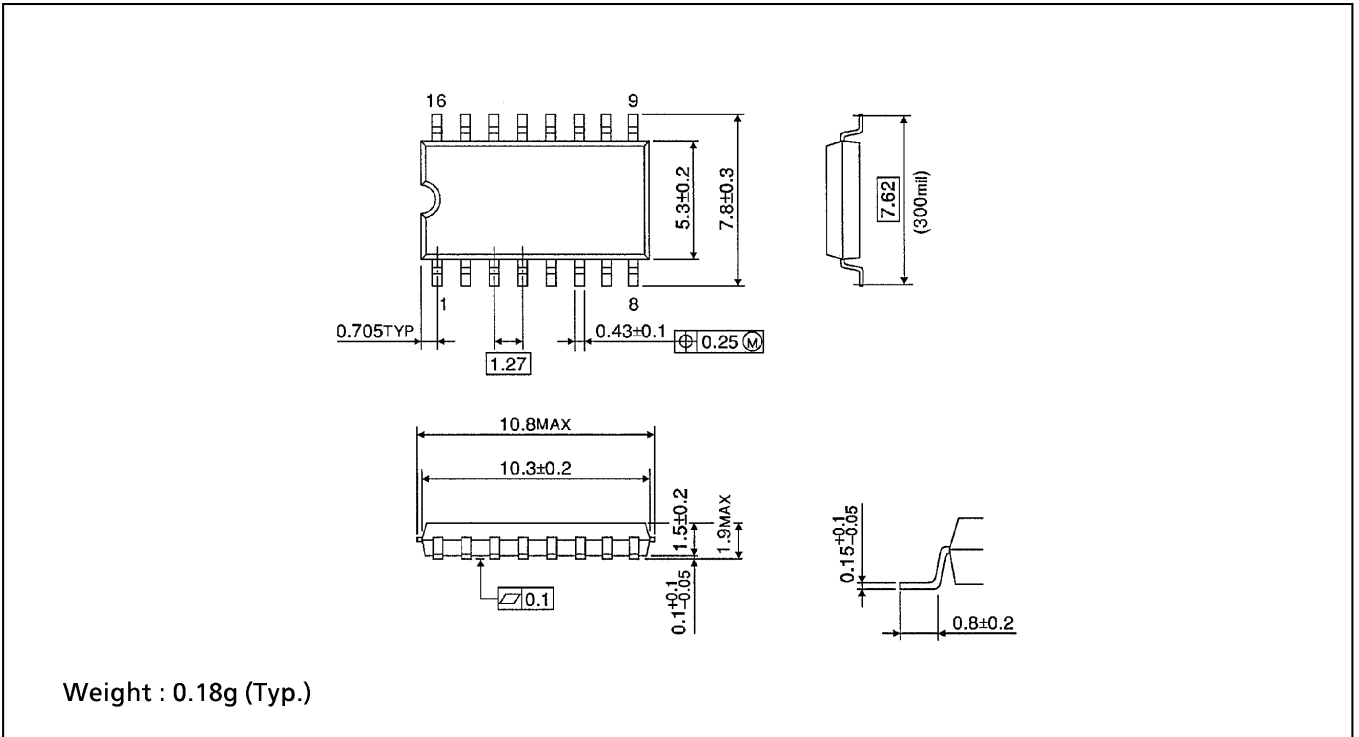
DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

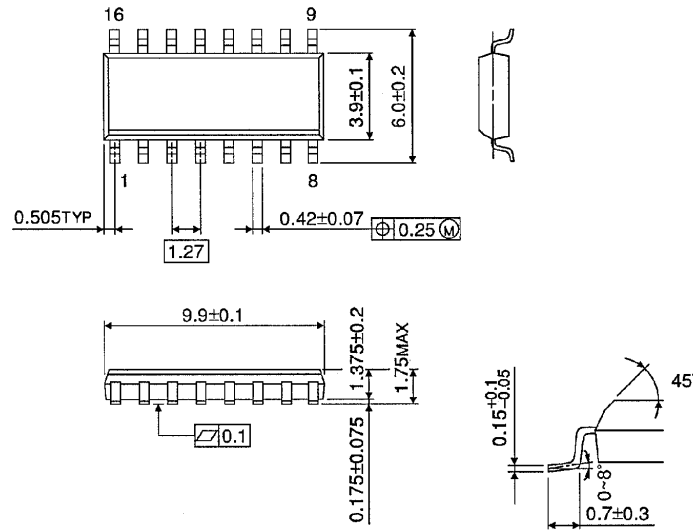
Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)