TA7233P

T-74-05-01

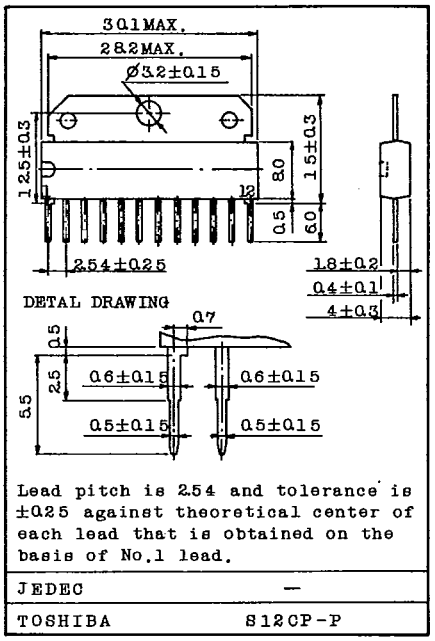
TENTATIVE

DUAL AUDIO POWER AMPLIFIER.

The TA7233P is a dual audio power amplifier for consumer applications.
It is suitable for power amplifier of portable stereo radio cassette and stereo receiver.

. High Power:
  $P_{OUT(1)}$=4.5W(Typ.)/CH
  (V_{CC}=12V, f=1kHz, THD=10%, R_L=4Ω)
  $P_{OUT(2)}$=2.5W(Typ.)/CH
  (V_{CC}=9V, f=1kHz, THD=10%, R_L=4Ω)
. Low Supply Current
  : I_{CCQ}=35mA(Typ.) (V_{CC}=12V, V_{in}=0)
. Thermal Shut Down Protector
. Audio Muting Function
. Operating Supply Voltage : $V_{CC(opr)}$=6～12V

Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	—
TOSHIBA	S12CP-P

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	16	V
Output Current (Peak/CH)	$I_{O(peak)}$	2.5	A
Power Dissipation	P_D	12.5	W
Operating Temperature	T_{opr}	-20～75	°C
Storage Temperature	T_{stg}	-55～150	°C

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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC}=12V, R_L=4Ω, R_g=600Ω, f=1kHz, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	I_{CCQ}		V_{in}=0	-	35	60	mA
Output Power	$P_{OUT}(1)$		THD=10%	3.8	4.5	-	W
	$P_{OUT}(2)$		THD=10%, V_{CC}=9V	2.0	2.5	-	
Total Harmonic Distortion	THD		P_{OUT}=1W/CH.	-	0.1	0.8	%
Voltage Gain	$G_V(1)$		R_f=150Ω V_{OUT}=0.775V_{rms}	43	45	47	dB
	$G_V(2)$		R_f=0, V_{OUT}=0.775V_{rms}	-	57	-	
Input Resistance	R_{IN}		-	-	30	-	kΩ
Output Noise Voltage	V_{NO}		R_g=10kΩ BW=20Hz ~ 20kHz	-	0.4	0.7	mV_{rms}
Ripple Rejection Ratio	R.R		R_g=600Ω f_{ripple}=100Hz	-	45	-	dB
Cross Talk	CT		R_g=10kΩ, Ampl↔2 V_{OUT}=0dBm, f=1kHz	-	60	-	dB
Input Offset Voltage	V_5, V_7		-	-	35	60	mV

TYPICAL DC VOLTAGE OF EACH TERMINAL

(V_{CC}=12V, Ta=25°C)

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
DC Voltage (V)	11.5	6	6.7	0.7	0.035	GND	0.035	0.7	GND	6	11.5	V_{CC}

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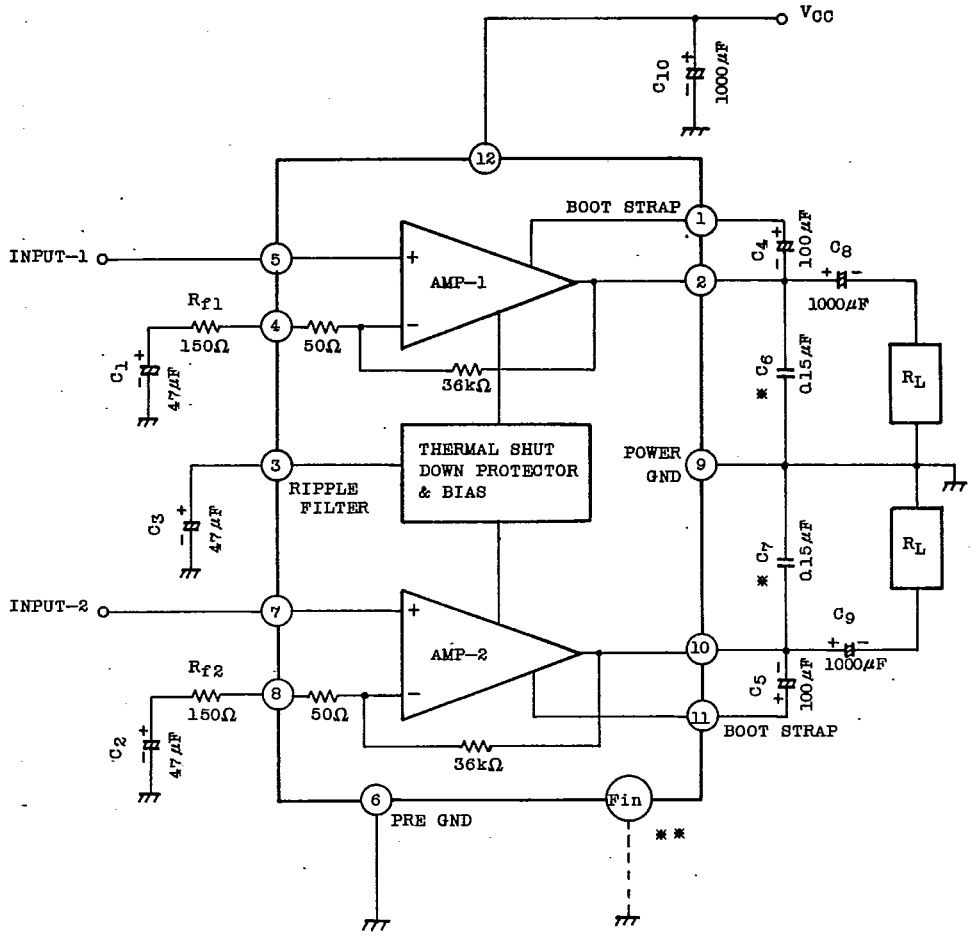
BLOCK DIAGRAM, TEST CIRCUIT



* C_6, C_7 : Polystiroll capacitor

** Heat Sink (Fin) : Connect to GND or open

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APPLICATION INFORMATION

1. VOLTAGE GAIN ADJUSTMENT

The voltage gain : G_V is determined by R_1, R_2 and R_f.

$$G_V = 20\log \frac{R_f+R_1+R_2}{R_f+R_1}$$

When $R_f=0$

$G_V=57dB$(Typ.)

When $R_f=150\Omega$

$G_V=45dB$(Typ.) is given.

The recommended voltage gain is more than 40dB.

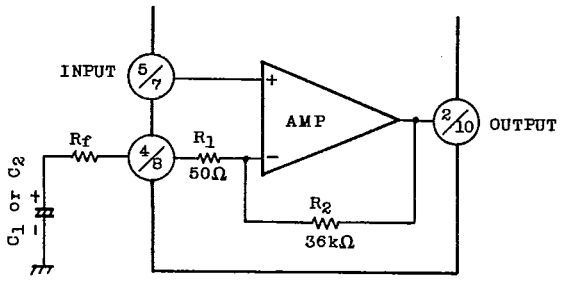

Fig. 1

2. AUDIO MUTING

Audio muting can be accomplished by connecting 3 pin(ripple filter) to GND as shown in Fig.2.

Then, the bias circuit are cut off.

Amount of muting attenuation is about 60dB.

The ripple filter : C_3 is in dead states at muting on. Therefore, the ripple rejection ratio should be checked at muting on/off in applications.

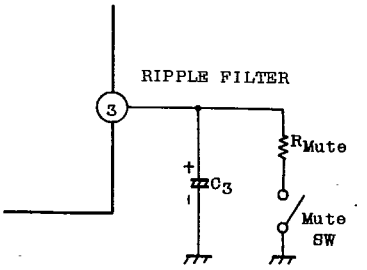

Fig. 2

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3. INPUT AMPLIFIER

The first stage is a PNP transistor, the input terminal voltage (Q_1 base) is 60mV and less, and the volume : V_R can be directly coupled without a coupling capacitor.
But volume slide noise should be checked at volume up/down in applications.

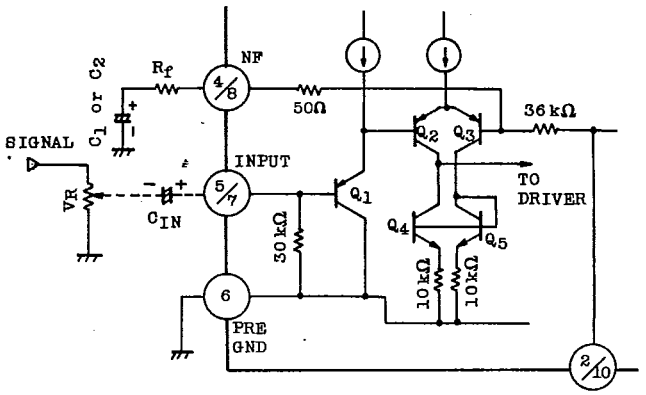

Fig. 3

4. THERMAL SHUT DOWN CIRCUIT

This IC built in thermal shut down protector.
The operating temperature of thermal shut down circuit is 160°C (Typ.)

5. CAPACITOR C_6, C_7

The purpose of capacitor C_6, C_7 are to prevent oscillation.
These capacitors need to be small temperature coefficient.
So celamic capacitor is unsuitable.
The voltage gain less than 40dB results occasionally in a parastic oscillation.
The following capacitor layout is recommended to refer the standard print board.

6. INPUT VOLTAGE

The maximum input voltage is $300mV_{rms}$(typ.). (at V_{CC}=12V, R_L=4Ω, f=1kHz)
When input voltage is more $300mV_{rms}$, the output wave is turn up.

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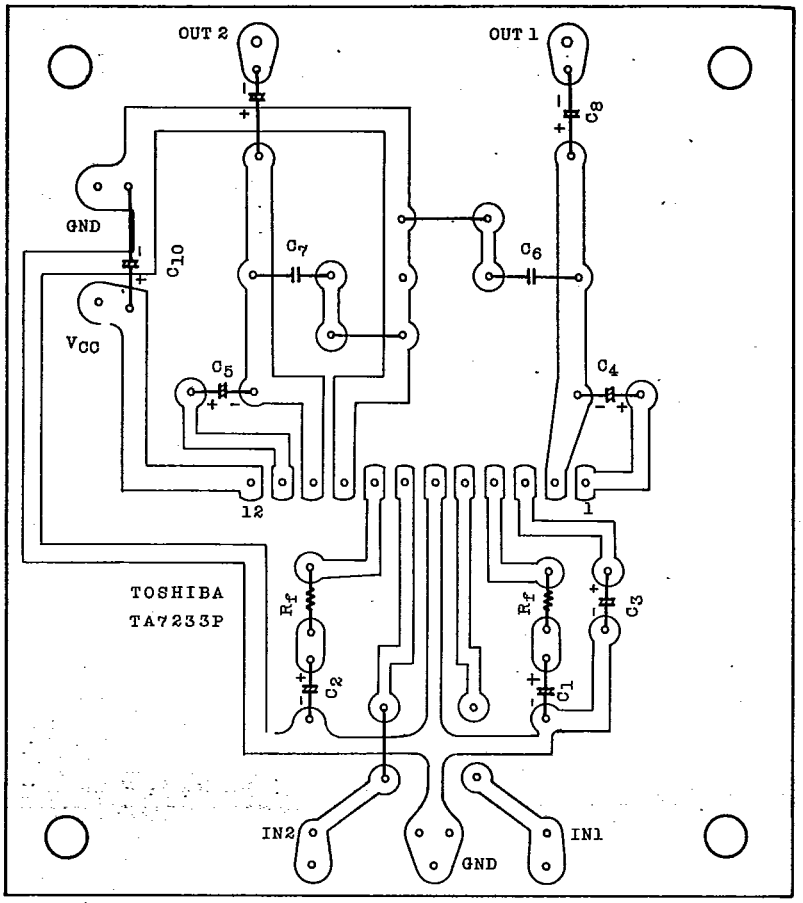
STANDARD PRINT PATTERN



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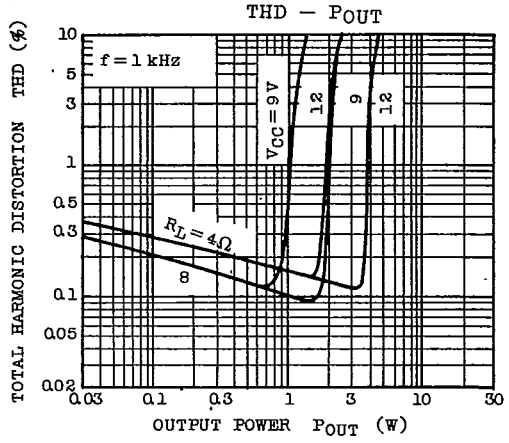
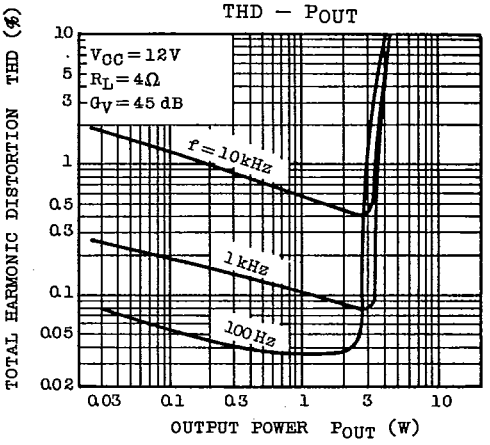
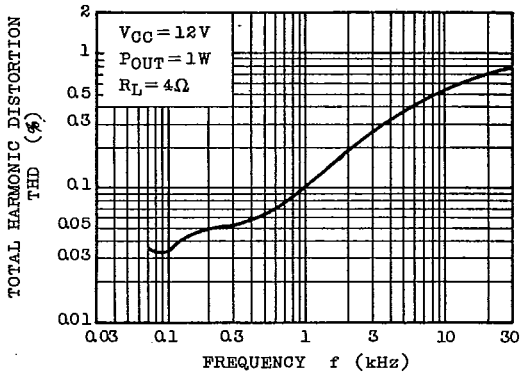
THD – P_{OUT}



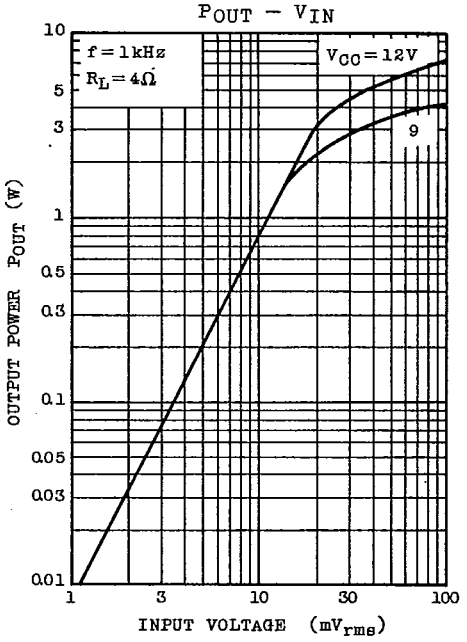
THD – P_{OUT}



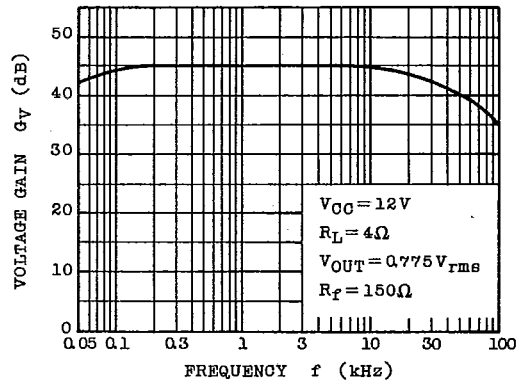
THD – f



P_{OUT} – V_{IN}



G_V – f



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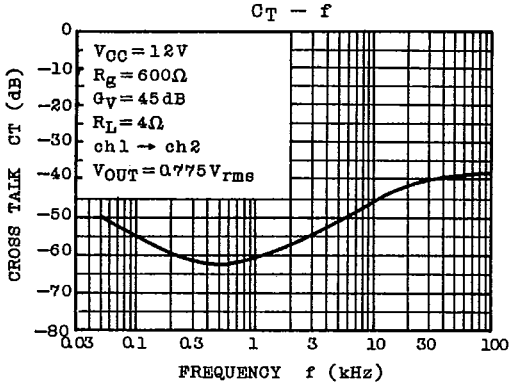
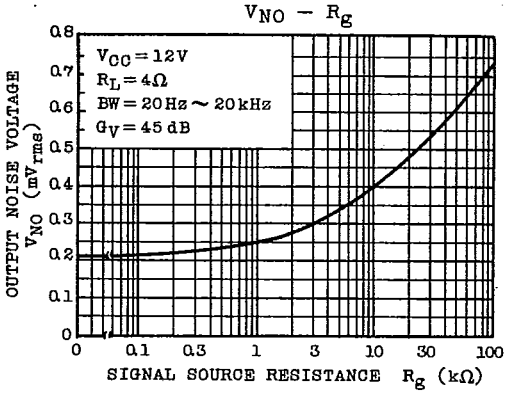
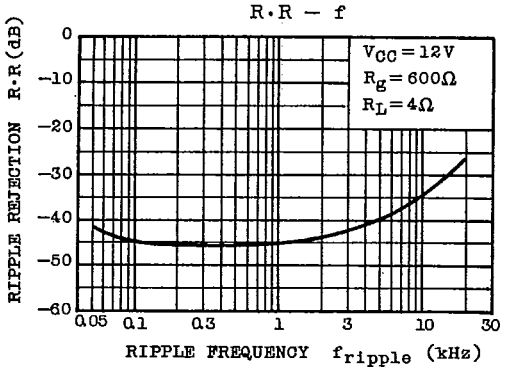
C_T – f



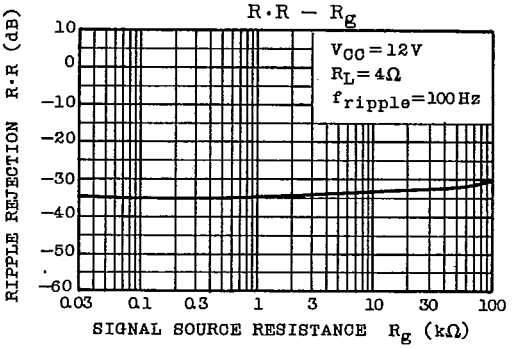
V_{NO} – R_g



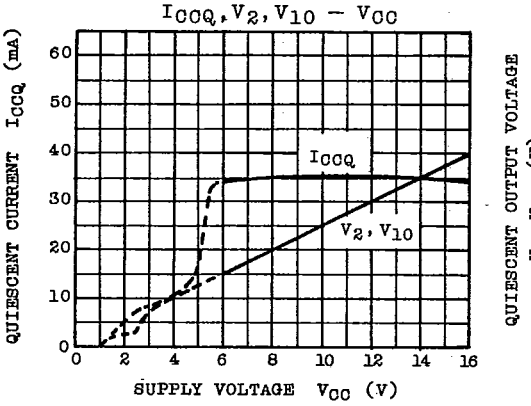
R·R – f



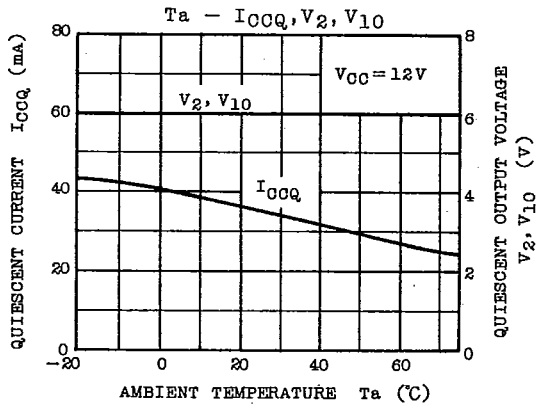
R·R – R_g



I_{CCQ}, V_2, V_{10} – V_{CC}



Ta – I_{CCQ}, V_2, V_{10}



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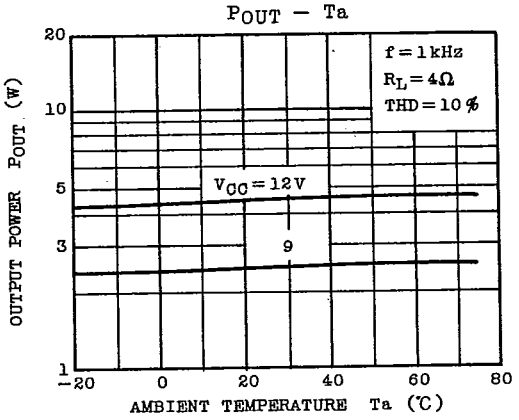
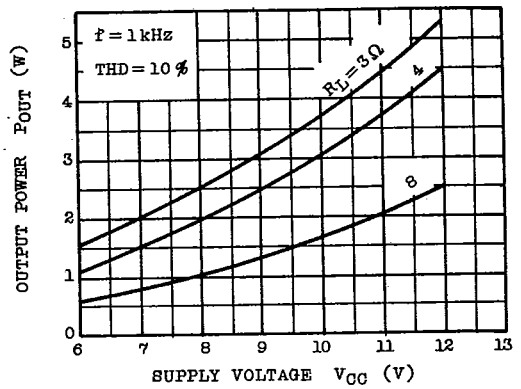
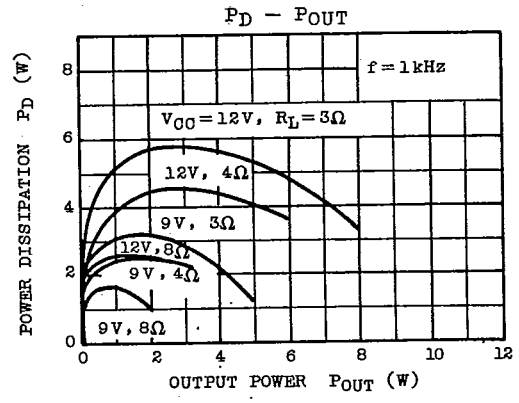
P_{OUT} – Ta



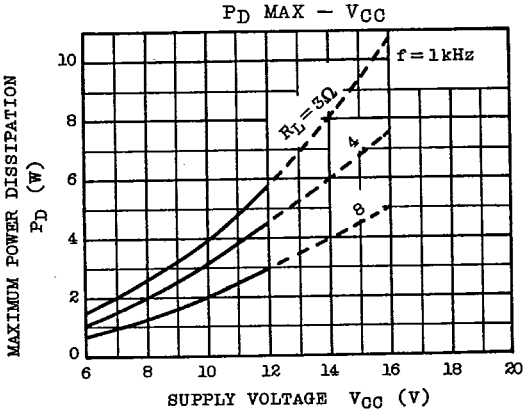
P_{OUT} – V_{CC}



P_D – P_{OUT}



P_D MAX – V_{CC}



P_D – Ta