

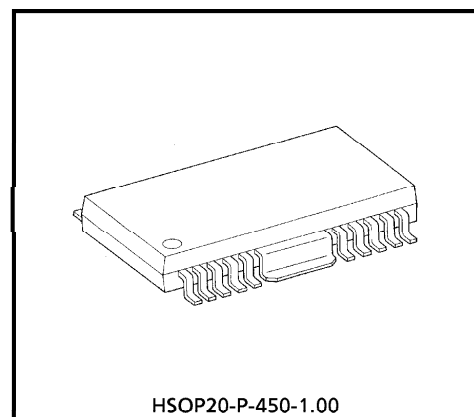
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

**TA2058F****POWER DRIVER IC FOR CD PLAYER**

TA2058F is a power driver IC developed for CD players. This IC have built-in 4 channel BTL power amplifiers which drives focus-coil and tracking coil for 3-beam pick-up head, disc motor and feed motor.

**FEATURES**

- 4 channel BTL linear drivers
- Few external parts
- Fixed voltage gain  
:  $G_v = 15\text{dB}$  (Typ.)
- High output power  
:  $V_{OM1} = 5V_{p-p}$  (Typ.)  $V_{CC} = 5V$ ,  $R_L = 50\Omega$   
:  $V_{OM2} = 6V_{p-p}$  (Typ.)  $V_{CC} = 6V$ ,  $R_L = 50\Omega$
- Thermal shut down protector
- Input reference voltage short protector
- Small Package  
: Power-flat package 1mm pitch 20pins
- Operation Supply Voltage Range  
:  $V_{CC(opr)} = 4.0 \sim 10.0V$  ( $T_a = 25^\circ\text{C}$ )

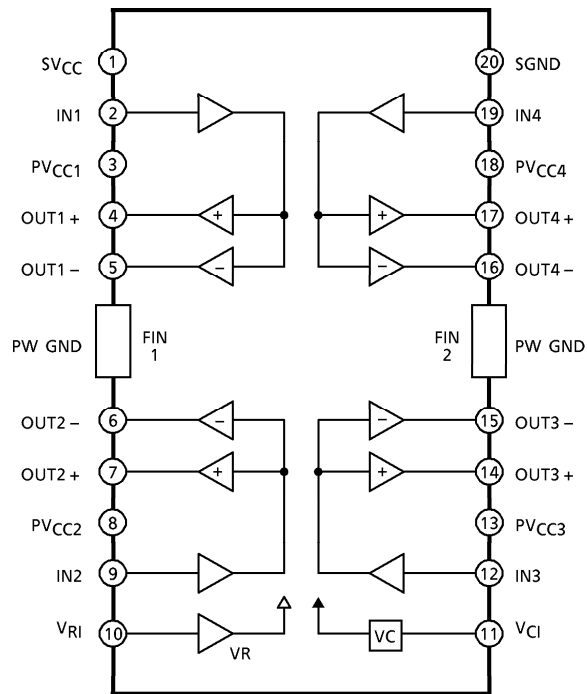


Weight : 0.8g (Typ.)

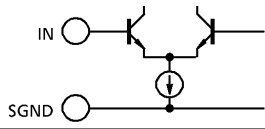
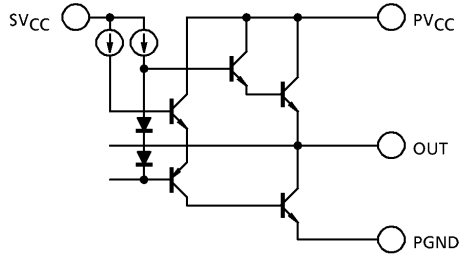
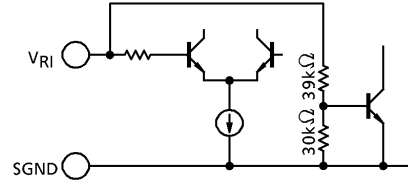
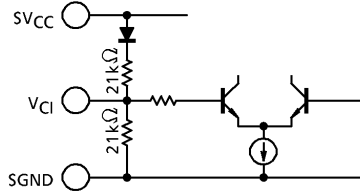
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**BLOCK DIAGRAM**



**TERMINAL EXPLANATION**

TERMINAL No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT
1	SV <sub>CC</sub>	Supply terminal of small signal	
2	IN1	Input for CH1 <ul style="list-style-type: none"> <li>Not biased inside.</li> </ul>	
3	PV <sub>CC1</sub>	Supply terminal of output stage for CH1 <ul style="list-style-type: none"> <li>Supply terminal of output stage are not connected to other channel terminal.</li> </ul>	
4	OUT1 +	Non-inverted output for CH1	
5	OUT1 -	Inverted output for CH1	
FIN1	PGND	Power GND <ul style="list-style-type: none"> <li>Connected to FIN2 and substrate.</li> </ul>	
6	OUT2 -	Inverted output for CH2	
7	OUT2 +	Non-inverted output for CH2	
8	PV <sub>CC2</sub>	Supply terminal of output stage for CH2	
9	IN2	Input for CH2	
10	V <sub>R1</sub>	Input reference voltage <ul style="list-style-type: none"> <li>Under condition of <math>V_{R1} \leq 1.8V</math>, internal bias circuit is shut off.</li> </ul>	
11	V <sub>Cl</sub>	Output reference voltage <ul style="list-style-type: none"> <li><math>V_{OUT} = V_{Cl} = (V_{CC} - V_F) / 2</math></li> </ul>	
12	IN3	Input for CH3	Same as CH1
13	PV <sub>CC3</sub>	Supply terminal of output stage for CH3	
14	OUT3 +	Non-inverted output for CH3	
15	OUT3 -	Inverted output for CH3	Connected to FIN1
FIN2	PGND	Power GND	
16	OUT4 -	Inverted output for CH4	Same as CH1
17	OUT4 +	Non-inverted output for CH4	
18	PV <sub>CC4</sub>	Supply terminal of output stage for CH4	
19	IN4	Input for CH4	
20	SGND	Small signal GND	

## MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>CC</sub>	14	V
Power Dissipation	P <sub>D</sub> (Note 1)	2 (Note 2)	W
Operating Temperature	T <sub>opr</sub>	-30~85	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

(Note 1) : Mounted on 50mm × 50mm × 1.6mm size board with copper area 60% over.

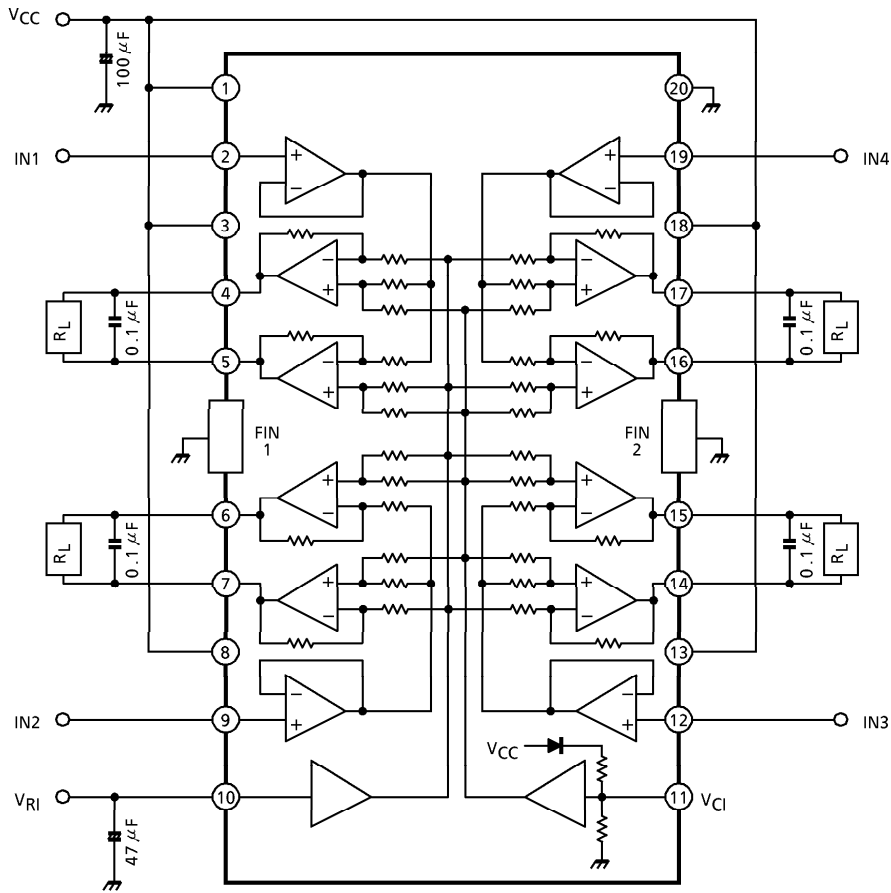
(Note 2) : Derated above Ta = 25°C, in the proportion of 62.5mW/°C.

## ELECTRICAL CHARACTERISTICS

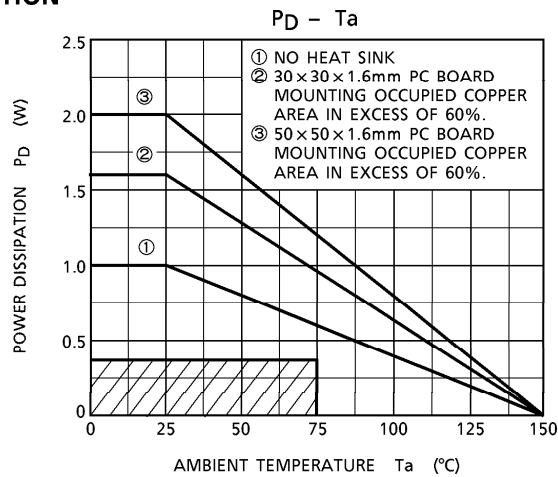
(Unless otherwise specified, V<sub>CC</sub> = 5V, R<sub>L</sub> = 5Ω, R<sub>g</sub> = 620Ω, V<sub>RI</sub> = 2.1V, f = 1kHz, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V <sub>CC</sub>	—		4.0	—	10.0	V
Quiescent Current	I <sub>CCQ</sub>	—	V <sub>in</sub> = 0, R <sub>L</sub> = OPEN	20	35	60	mA
Input Offset Current	I <sub>IIN</sub>	—	V <sub>IN</sub> = 2.1V	—	250	800	nA
V <sub>RI</sub> Terminal Offset Current	I <sub>I0</sub>	—	V <sub>RI</sub> = 2.1V	—	35	120	μA
Output Offset Voltage	V <sub>O</sub> OS1	—	V <sub>CC</sub> = 5V, R <sub>g</sub> = 0Ω	-30	—	30	mV
	V <sub>O</sub> OS2	—	V <sub>CC</sub> = 8V, R <sub>g</sub> = 0Ω	-50	—	50	
	V <sub>O</sub> OS3	—	V <sub>CC</sub> = 12V, R <sub>g</sub> = 0Ω	-100	—	100	
Reference Output Voltage	V <sub>OUT</sub>	—		—	2.1	—	V
Maximum Output Voltage	V <sub>OM1</sub>	—	V <sub>CC</sub> = 5V	4.0	5.0	—	V <sub>p-p</sub>
	V <sub>OM2</sub>	—	V <sub>CC</sub> = 6V	5.0	6.0	—	
Voltage Gain	G <sub>v</sub>	—	V <sub>in</sub> = 100mV <sub>rms</sub>	14.5	15.5	16.5	dB
Frequency Response	f <sub>c</sub>	—	V <sub>in</sub> = 100mV <sub>rms</sub>	—	100	—	kHz
Total Harmonic Distortion	THD	—	V <sub>in</sub> = 100mV <sub>rms</sub>	—	-50	—	dB
Slew Rate	S.R.	—	V <sub>out</sub> = 2V <sub>p-p</sub>	—	1.0	—	V / μs
Cross Talk	C.T.	—	V <sub>out</sub> = 1V <sub>rms</sub>	—	-60	—	dB
Ripple Rejection Ratio	R.R.	—	f <sub>rip</sub> = 100Hz, V <sub>rip</sub> = 100mV <sub>rms</sub>	—	-60	—	dB
Thermal Shut Down Temperature	T <sub>TSD</sub>	—	Chip temperature	—	150	—	°C
V <sub>RI</sub> ~GND Short Protection Voltage	V <sub>RI</sub> OFF	—		1.4	1.6	1.8	V

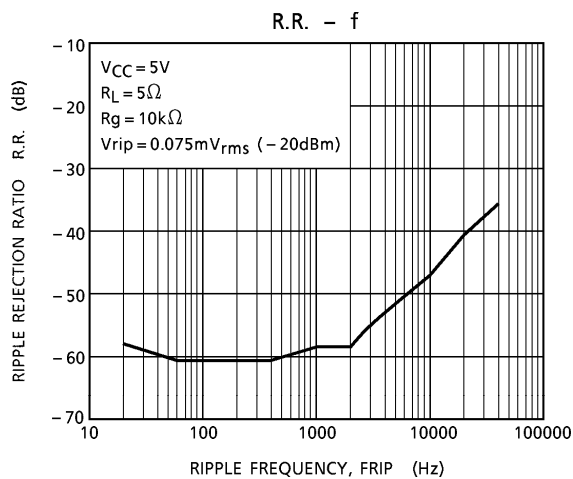
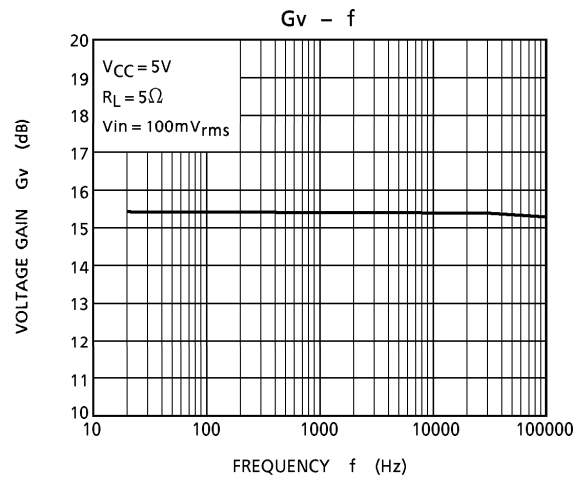
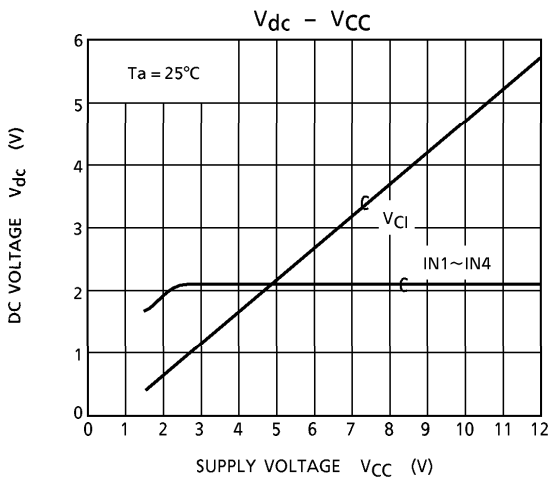
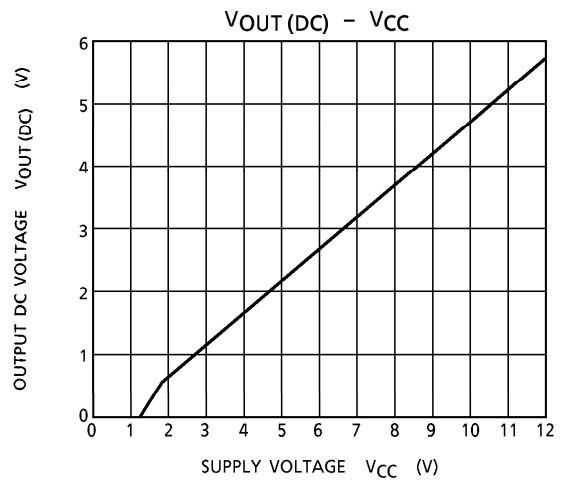
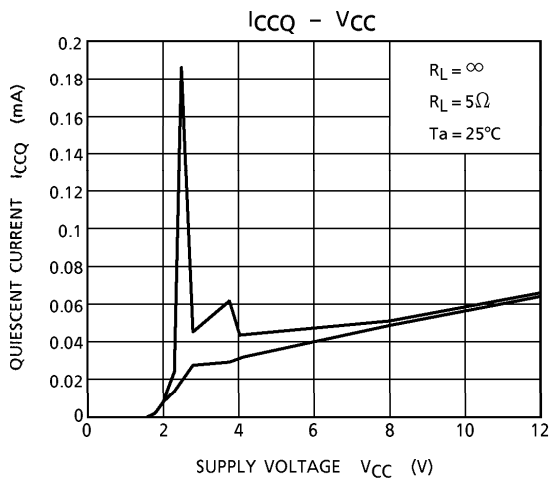
TEST CIRCUIT

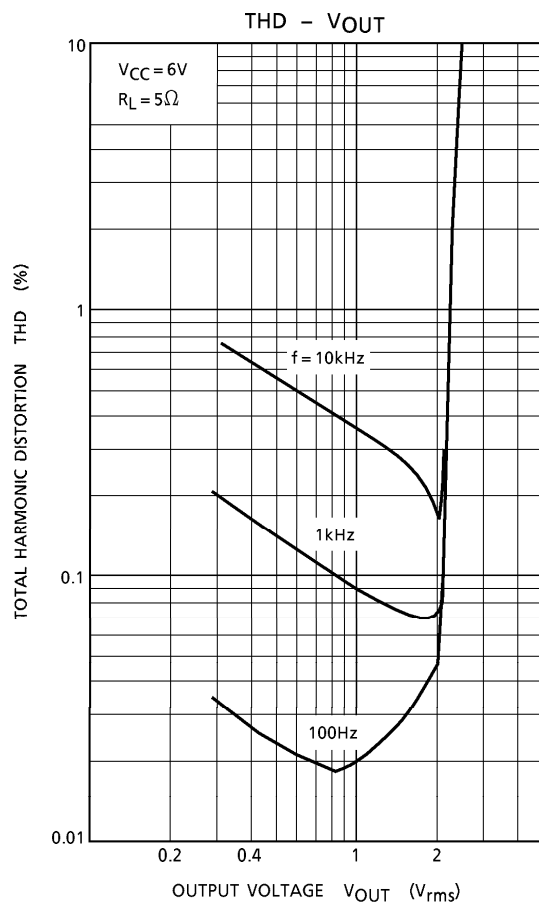
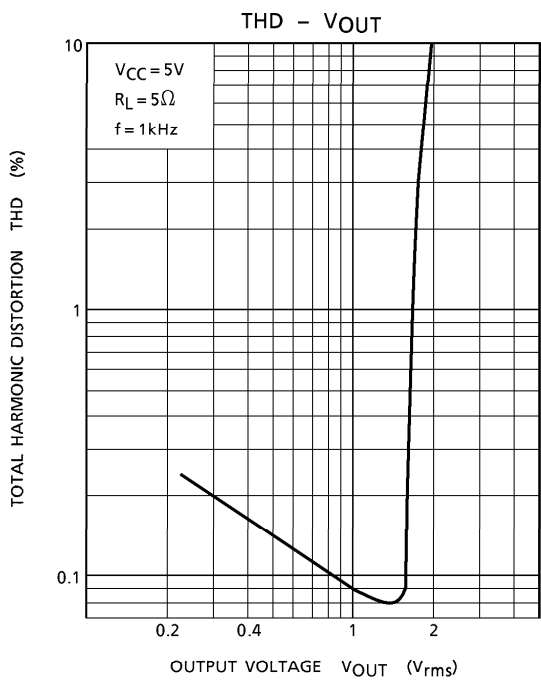


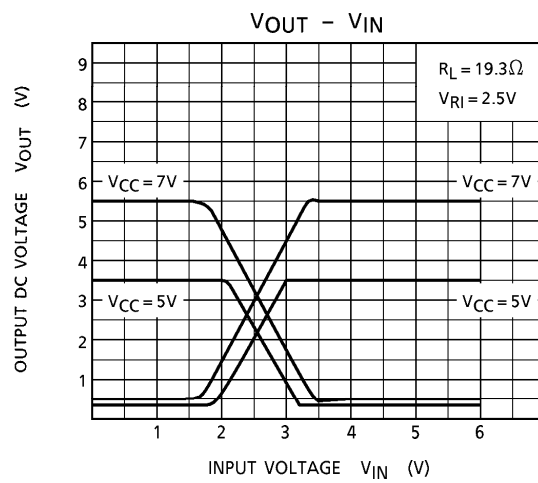
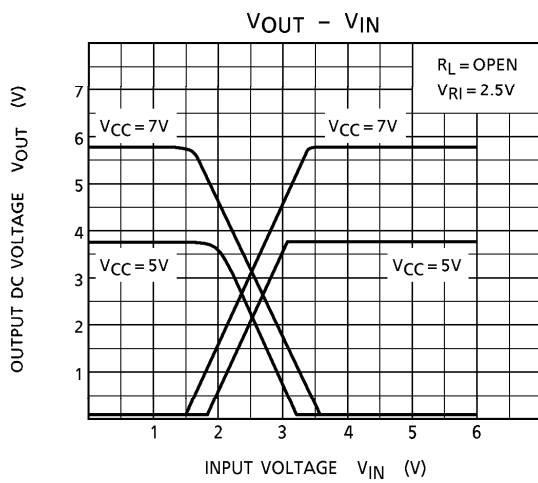
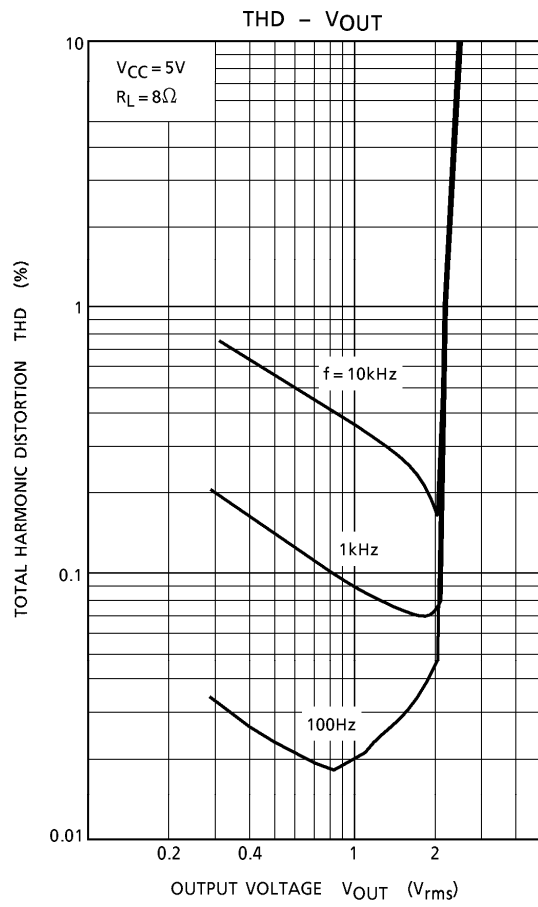
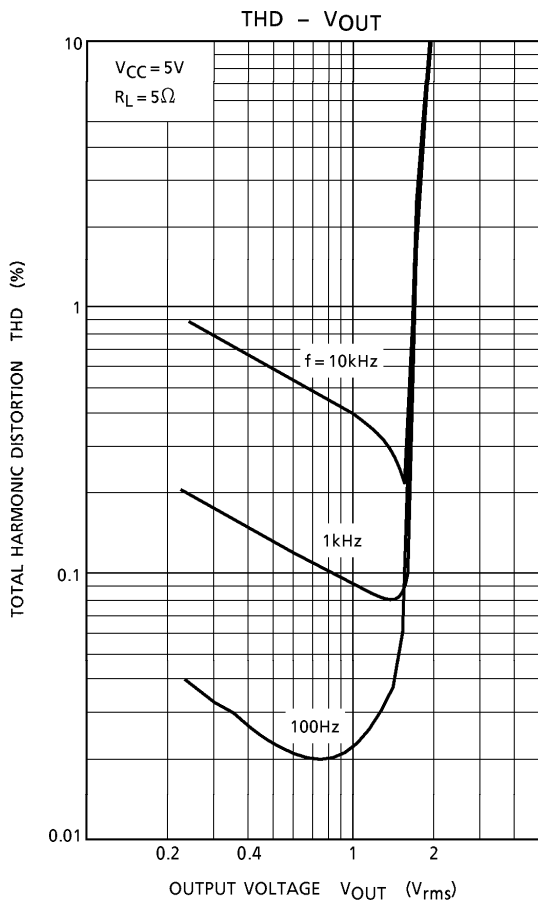
HSOP 20 POWER DISSIPATION



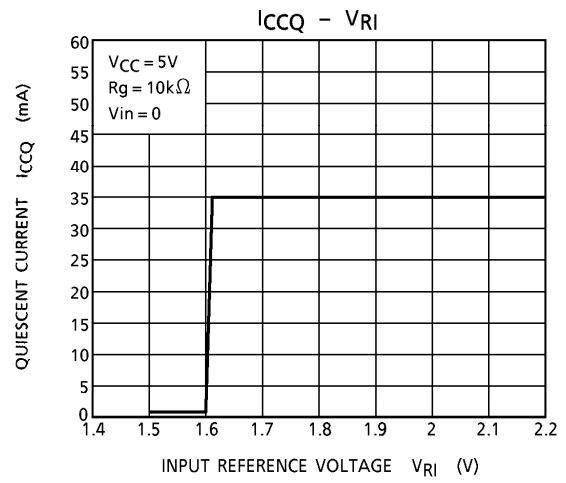
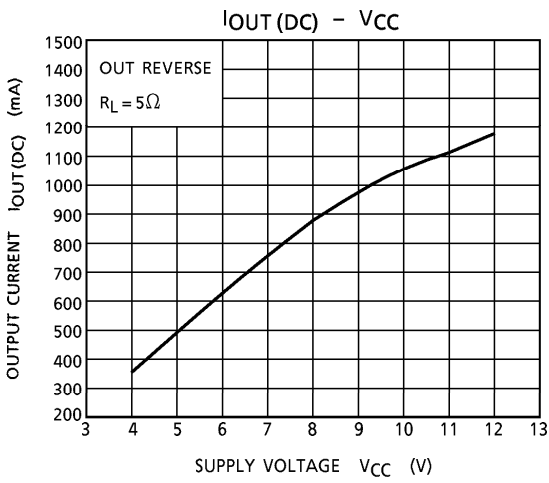
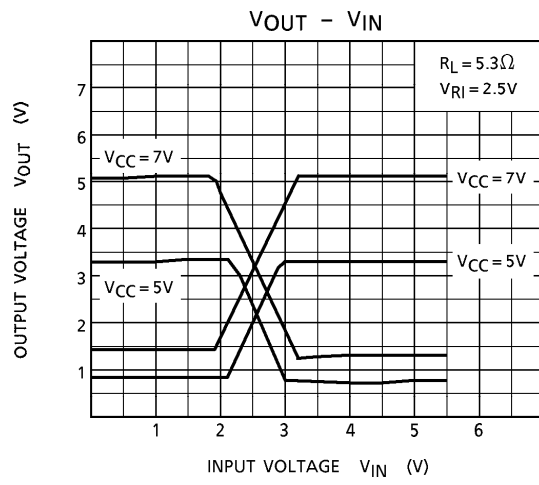
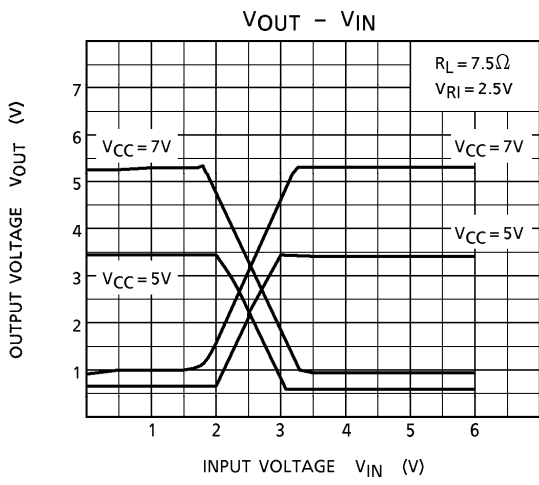
(Note) In case of normal use, power dissipation of IC only is oblique line portion.









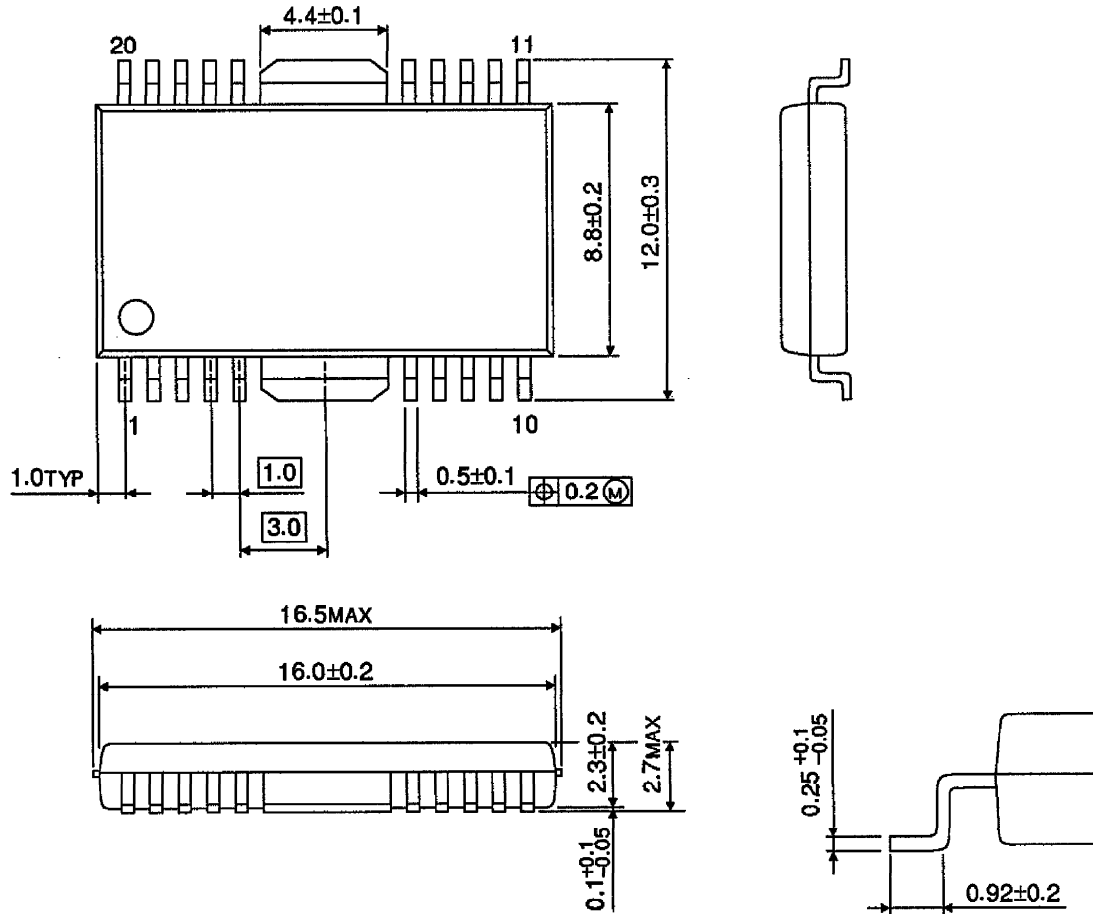


**PRECAUTION USE**

- Input Stage
  - Input stages are consisted of differential circuit of NPN Tr, and have built-in IB compensation circuit.
- Built-in Driver
  - Each channel driver consists of BTL configuration linear amplifier.
  - Voltage gain is fixed :  $G_V = 15.5\text{dB}$  (Typ.)
  - Voltage loss for output stage is  $2V_{BE} + V_{CE}(\text{sat})$  for positive cycle,  $V_{CE}(\text{sat})$  for negative cycle, because of no-bootstrap circuit. So, output DC voltage is designed as less than  $1/2V_{CC}$ .
- $V_{RI}$  Terminal
  - $V_{RI}$  is reference voltage terminal for input signal.
  - If reference voltage from servo IC drop less than 1.8V, protection circuit operates and shut off bias circuit inside. This operation is to prevent load from moving undesirably in case of  $V_{RI}$  drop for accident or some reason.
- $V_{CI}$  Terminal
  - Output DC voltage is determined by circuit of this terminal inside as ;  
$$V_{CI} = V_{OUT}(\text{DC}) = (V_{CC} - V_F) / 2$$
  - Output signal dynamic range is depend on  $V_{CC}$ . On the other hand, input signal dynamic range is determined by  $V_{RI}$  as mentioned and voltage gain is fixed inside. So, maximum output voltage does not increase as  $V_{CC}$  increases.
  - Because of BTL configuration, Ripple Rejection Ratio does not improve not much when capacitor is connected to  $V_{CI}$  terminal to GND.
- GND
  - Large signal GND is for output stage and small signal GND is for stages from input circuit to pre-output stage.
  - These GND pins are not connected inside.
  - Phin① and Phin② are connected to Bedflame, and it is connected to substrate.
  - It is advised that you make a Printed Board layout of small signal GND and large signal GND should be isolated each other.
- Oscillation preventive capacitor
  - We recommend to use the capacitor of  $0.1\mu\text{F}$ , between each output terminals. But perform the temperature test to check the oscillation allowance, since the oscillation allowance is varied according to the causes described below.
    - 1) Supply voltage
    - 2) Ambient temperature
    - 3) Load impedance
    - 4) Capacity value of condenser
    - 5) Kind of condenser
    - 6) Layout of Printed board
- We recommend to connect Pass-condenser, which is about 10 to  $100\mu\text{F}$  between  $V_{RI}$  terminal and GND.
- $V_{CI}$  terminal is recommend to use "OPEN".

**OUTLINE DRAWING**  
HSOP20-P-450-1.00

Unit : mm



Weight : 0.8g (Typ.)