

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74HC4051AP, TC74HC4051AF, TC74HC4051AFT**  
**TC74HC4052AP, TC74HC4052AF, TC74HC4052AFT**  
**TC74HC4053AP, TC74HC4053AF, TC74HC4053AFN, TC74HC4053AFT**

**TC74HC4051AP/AF/AFT 8 - CHANNEL ANALOG MULTIPLEXER / DEMULTIPLEXER**  
**TC74HC4052AP/AF/AFT DUAL 4 - CHANNEL ANALOG MULTIPLEXER / DEMULTIPLEXER**  
**TC74HC4053AP/AF/AFN/AFT TRIPLE 2 - CHANNEL ANALOG MULTIPLEXER / DEMULTIPLEXER**

The TC74HC4051A/4052A/4053A are high speed CMOS ANALOG MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C<sup>2</sup>MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4051A has an 8 channel configuration, the TC74HC4052A has a 4 channel×2 configuration and the TC74HC4053A has a 2 channel×3 configuration.

The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal (V<sub>CC</sub>-V<sub>EE</sub>) can then be switched by the small logical amplitude (V<sub>CC</sub>-GND) control signal.

For example, in the case of V<sub>CC</sub>=5V, GND=0V, V<sub>EE</sub>=-5V, signals between -5V and +5V can be switched from the logical circuit with a single power supply of 5V. As the ON-resistance of each switch is low, they can be connected to circuits with low input impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**FEATURES :**

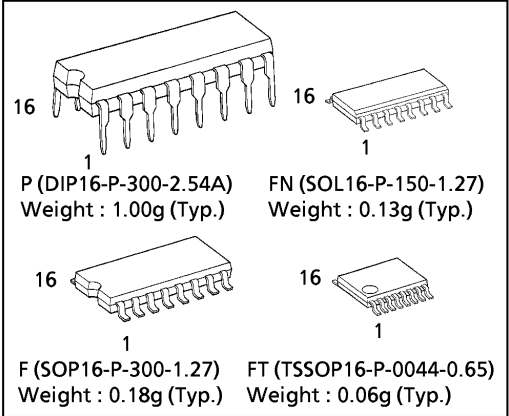
- High Speed.....t<sub>pd</sub> = 15ns(typ.) at V<sub>CC</sub> = 5V  
V<sub>EE</sub> = 0V
- Low Power Dissipation.....I<sub>CC</sub> = 4μA(Max.) at Ta = 25°C
- High Noise Immunity.....V<sub>NIH</sub> = V<sub>NIL</sub> = 28% V<sub>CC</sub> (Min.)
- Low ON Resistance.....R<sub>ON</sub> = 50Ω (typ.)  
at V<sub>CC</sub>-V<sub>EE</sub> = 9V
- High Noise Immunity.....THD = 0.02% (typ.)  
at V<sub>CC</sub>-V<sub>EE</sub> = 9V
- Pin and Function Compatible with 4051/4052/4053B

**TRUTH TABLE**

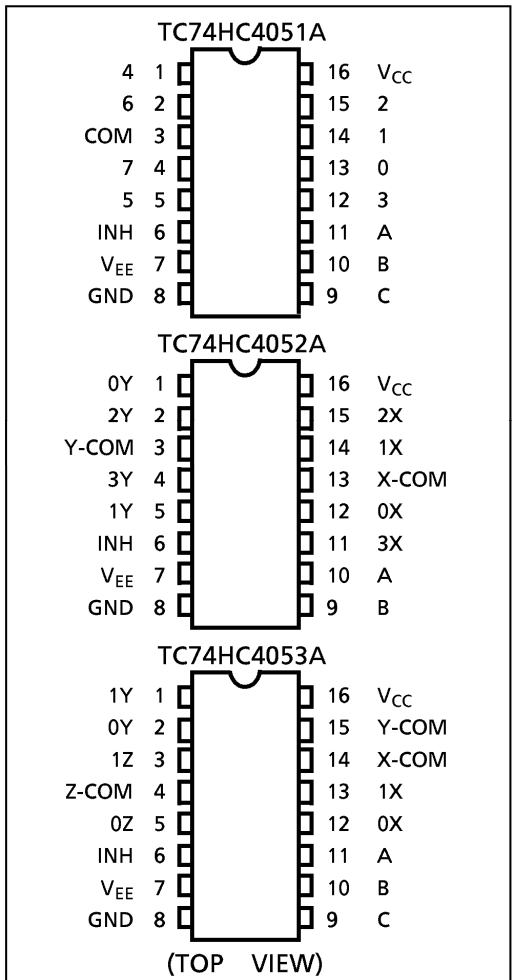
CONTROL INPUTS				"ON" CHANNEL		
INHIBIT	C*	B	A	HC4051A	HC4052A	HC4053A
L	L	L	L	0	0X, 0Y	0X,0Y,0Z
L	L	L	H	1	1X, 1Y	1X,0Y,0Z
L	L	H	L	2	2X, 2Y	0X,1Y,0Z
L	L	H	H	3	3X, 3Y	1X,1Y,0Z
L	H	L	L	4	--	0X,0Y,1Z
L	H	L	H	5	--	1X,0Y,1Z
L	H	H	L	6	--	0X,1Y,1Z
L	H	H	H	7	--	1X,1Y,1Z
H	X	X	X	NONE	NONE	NONE

X : Don't Care, \* : Except HC4052A

(Note) The JEDEC SOP (FN) is not available in Japan.



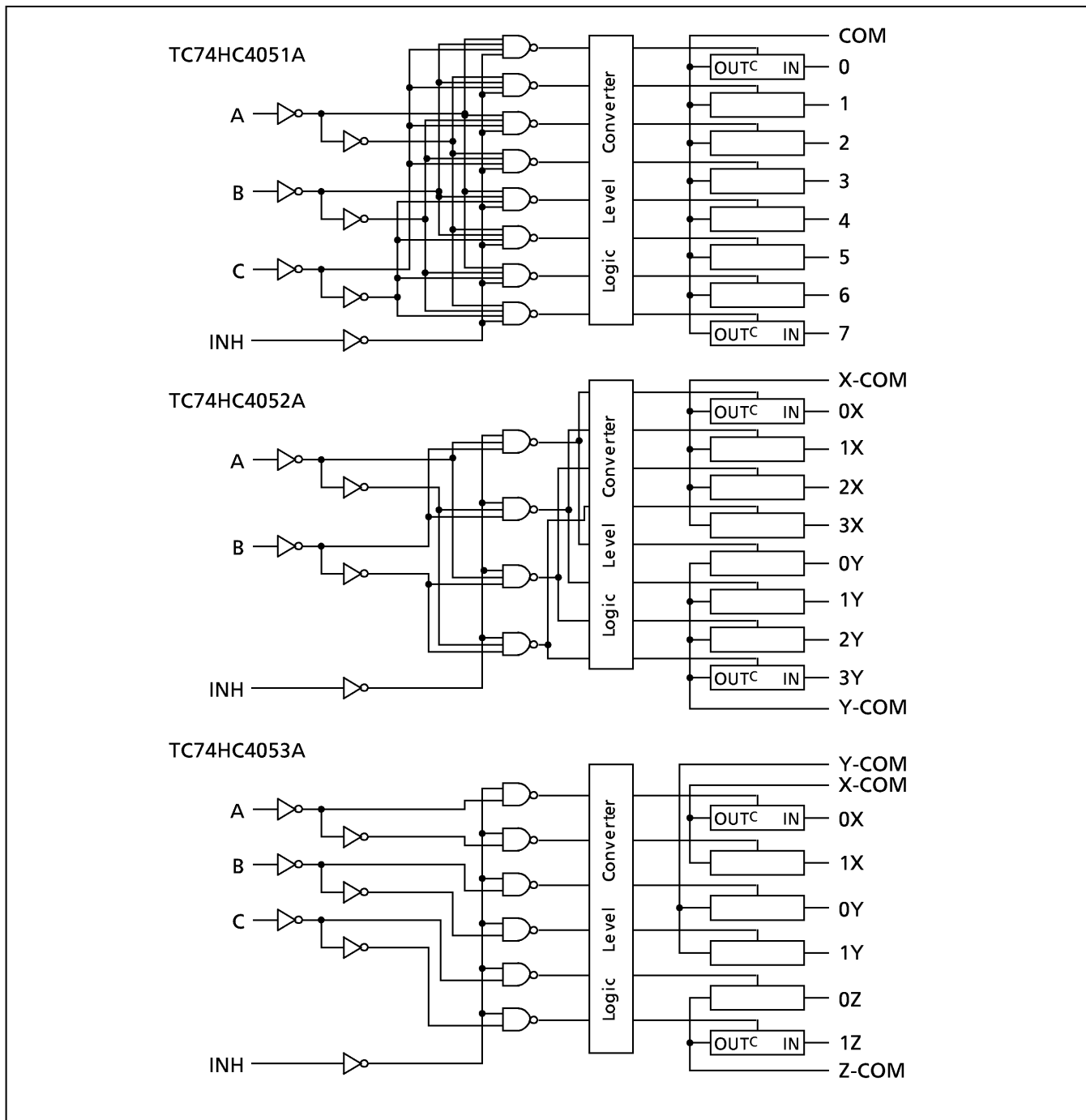
**PIN ASSIGNMENT**



961001EBA2

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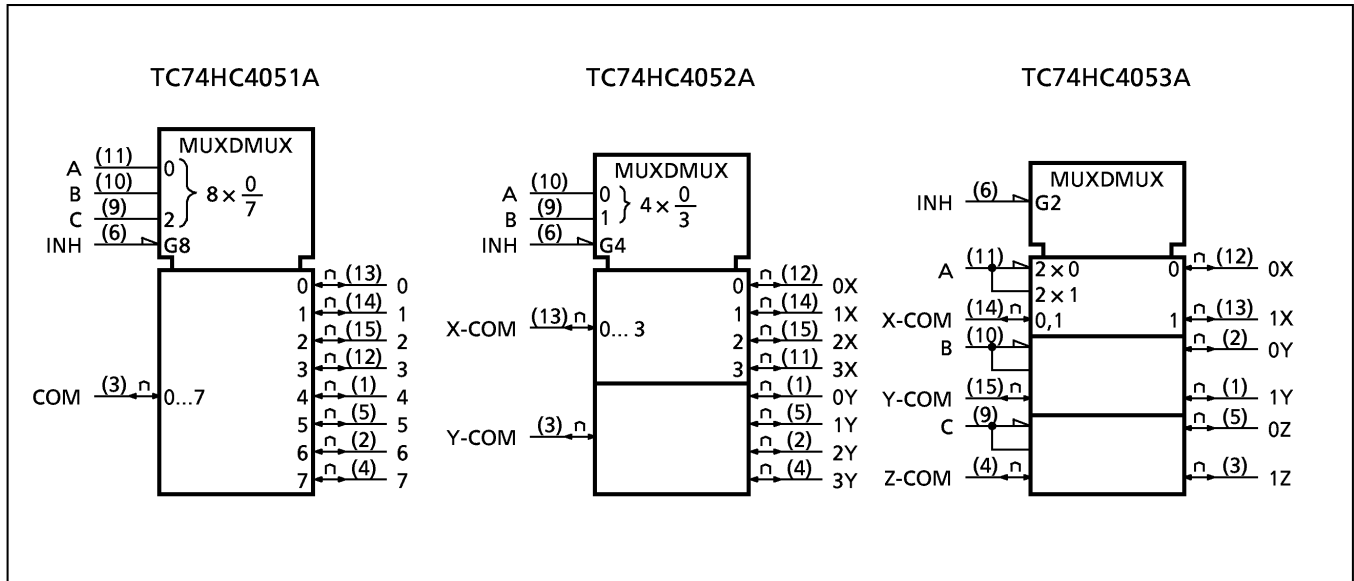
**SYSTEM DIAGRAM**



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**IEC LOGIC SYMBOL**



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
Supply Voltage Range	$V_{CC}-V_{EE}$	-0.5~13	V
Control Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
Switch I/O Voltage	$V_{I/O}$	$V_{EE}-0.5\sim V_{CC}+0.5$	V
Control Input Diode Current	$I_{ICK}$	$\pm 20$	mA
I/O Diode Current	$I_{IOK}$	$\pm 20$	mA
Switch through Current	$I_T$	$\pm 25$	mA
DC $V_{CC}$ or Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP, TSSOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^\circ\text{C}\sim 65^\circ\text{C}$ . From  $T_a = 65^\circ\text{C}$  to  $85^\circ\text{C}$  a derating factor of  $-10\text{mW}/^\circ\text{C}$  shall be applied until 300mW.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	2~6	V
Supply Voltage Range	$V_{EE}$	-6~0	V
Supply Voltage Range	$V_{CC}-V_{EE}$	2~12	V
Control Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Switch I/O Voltage	$V_{I/O}$	$V_{EE}\sim V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Control Input Rise and Fall Time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~500 ( $V_{CC} = 4.5\text{V}$ ) 0~400 ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V <sub>EE</sub> (V)	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Control Input Voltage	V <sub>IHC</sub>			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Control Input Voltage	V <sub>ILC</sub>			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	
ON Resistance	R <sub>ON</sub>	V <sub>IN</sub> = V <sub>ILC</sub> or V <sub>IHC</sub> V <sub>I/O</sub> = V <sub>CC</sub> to V <sub>EE</sub> I <sub>I/O</sub> ≤ 2mA	GND -4.5 -6.0	4.5 4.5 6.0	— — —	85 55 50	180 120 100	— — —	225 150 125	Ω
		V <sub>IN</sub> = V <sub>ILC</sub> or V <sub>IHC</sub> V <sub>I/O</sub> = V <sub>CC</sub> or V <sub>EE</sub> I <sub>I/O</sub> ≤ 2mA	GND GND -4.5 -6.0	2.0 4.5 4.5 6.0	— — — —	150 70 50 45	— 150 100 80	— — — —	— 190 125 100	
Difference of ON Resistance Between Switches	ΔR <sub>ON</sub>	V <sub>IN</sub> = V <sub>ILC</sub> or V <sub>IHC</sub> V <sub>I/O</sub> = V <sub>CC</sub> to V <sub>EE</sub> I <sub>I/O</sub> ≤ 2mA	GND -4.5 -6.0	4.5 4.5 6.0	— — —	10 5 5	30 12 10	— — —	35 15 12	
Input / Output Leakage Current (SWITCH OFF)	I <sub>OFF</sub>	V <sub>OS</sub> = V <sub>CC</sub> or GND V <sub>IS</sub> = GND or V <sub>CC</sub> V <sub>IN</sub> = V <sub>ILC</sub> or V <sub>IHC</sub>	GND -6.0	6.0 6.0	— —	— —	± 60 ± 100	— —	± 600 ± 1000	nA
Switch Input Leakage Current (SWITCH ON)	I <sub>IZ</sub>	V <sub>OS</sub> = V <sub>CC</sub> or GND V <sub>IN</sub> = V <sub>ILC</sub> or V <sub>IHC</sub>	GND -6.0	6.0 6.0	— —	— —	± 60 ± 100	— —	± 600 ± 1000	
Control Input Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	GND	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	GND -6.0	6.0 6.0	— —	— —	4.0 8.0	— —	40.0 80.0	

**AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns, GND = 0V)**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>EE</sub> (V)	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Phase difference between Input and Output	φ I/O	ALL TYPES	GND	2.0	—	25	60	—	75	ns
			GND	4.5	—	6	12	—	15	
			GND	6.0	—	5	10	—	13	
			-4.5	4.5	—	4	—	—	—	
Output Enable Time	t <sub>pZL</sub> t <sub>pZH</sub>	*1 4051	GND	2.0	—	64	225	—	280	
			GND	4.5	—	18	45	—	56	
			GND	6.0	—	15	38	—	48	
		*1 4052	GND	2.0	—	64	225	—	280	
			GND	4.5	—	18	45	—	56	
			GND	6.0	—	15	38	—	48	
		*1 4053	GND	2.0	—	50	225	—	280	
			GND	4.5	—	14	45	—	56	
			GND	6.0	—	12	38	—	48	
Output Disable Time	t <sub>pLZ</sub> t <sub>pHZ</sub>	*1 4051	GND	2.0	—	100	250	—	315	
			GND	4.5	—	33	50	—	63	
			GND	6.0	—	28	43	—	54	
		*1 4052	GND	2.0	—	100	250	—	315	
			GND	4.5	—	33	50	—	63	
			GND	6.0	—	28	43	—	54	
		*1 4053	GND	2.0	—	95	225	—	280	
			GND	4.5	—	30	45	—	56	
			GND	6.0	—	26	38	—	48	
Control Input Capacitance	C <sub>in</sub>	ALL TYPES	—	—	—	5	10	—	10	
COMMON Terminal Capacitance	C <sub>IS</sub>	4051	—	—	—	36	70	—	70	
		4052	-5.0	5.0	—	19	40	—	40	
		4053	—	—	—	11	20	—	20	
SWITCH Terminal Capacitance	C <sub>OS</sub>	4051	—	—	—	7	15	—	15	
		4052	-5.0	5.0	—	7	15	—	15	
		4053	—	—	—	7	15	—	15	
Feedthrough Capacitance	C <sub>IOS</sub>	4051	—	—	—	0.95	2	—	2	
		4052	-5.0	5.0	—	0.85	2	—	2	
		4053	—	—	—	0.75	2	—	2	
Power Dissipation Capacitance	C <sub>PD</sub>	*2 4051	—	—	—	70	—	—	—	
		4052	GND	5.0	—	71	—	—	—	
		4053	—	—	—	67	—	—	—	

\* 1: R<sub>L</sub> = 1kΩ

\* 2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

**ANALOG SWITCH CHARACTERISTICS ( GND = 0V, Ta = 25°C )**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>EE</sub> (V)		TYP.	UNIT	
			V <sub>CC</sub> (V)				
Sine Wave Distortion ( T . H . D )		R <sub>L</sub> = 10kΩ C <sub>L</sub> = 50pF f <sub>IN</sub> = 1kHz V <sub>IN</sub> = 4.0V <sub>p-p</sub> V <sub>IN</sub> = 8.0V <sub>p-p</sub> V <sub>IN</sub> = 11.0V <sub>p-p</sub>	-2.25 -4.5 -6.0	2.25 4.5 6.0	0.025 0.020 0.018	%	
Frequency Response ( Switch ON )	f <sub>MAX</sub>	Adjust f <sub>IN</sub> Voltage to obtain 0dBm at V <sub>OS</sub> Increase f <sub>IN</sub> Frequency until dB Meter reads -3dB  R <sub>L</sub> = 50Ω, C <sub>L</sub> = 10pF f <sub>IN</sub> = 1MHz, Sine Wave	*1 ALL	-2.25	2.25	120	MHz
			*2 4051 4052 4053			45 70 95	
			*1 ALL	-4.5	4.5	190	
			*2 4051 4052 4053			70 110 150	
			*1 ALL	-6.0	6.0	200	
			*2 4051 4052 4053			85 140 190	
Feed through Attenuation ( Switch OFF )		V <sub>in</sub> is centered at ( V <sub>CC</sub> - V <sub>EE</sub> ) / 2 Adjust input for 0dBm R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF f <sub>IN</sub> = 1MHz, Sine Wave	-2.25 -4.5 -6.0	2.25 4.5 6.0	-50 -50 -50	dB	
Crosstalk ( Control Input to Signal Output )		R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF f <sub>IN</sub> = 1MHz, Square Wave ( t <sub>r</sub> = t <sub>f</sub> = 6ns )	-2.25 -4.5 -6.0	2.25 4.5 6.0	60 140 200	mV	
Crosstalk ( Between any switches )		Adjust V <sub>IN</sub> to obtain 0dBm at Input R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF f <sub>IN</sub> = 1MHz, Sine Wave	-2.25 -4.5 -6.0	2.25 4.5 6.0	-50 -50 -50	dB	

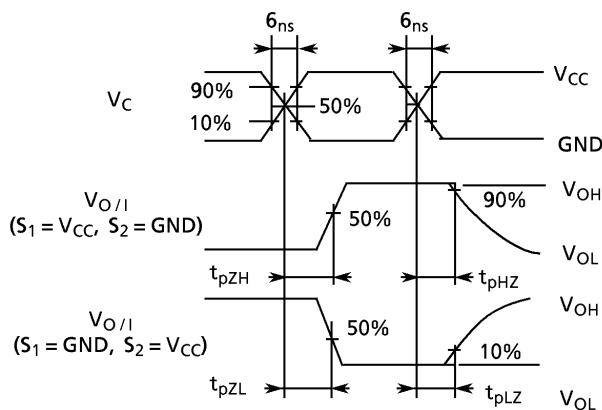
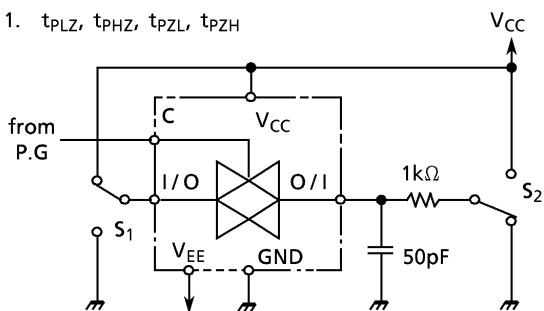
\* 1 : Input COMMON Terminal, and measured at SWITCH Terminal.

\* 2 : Input SWITCH Terminal, and measured at COMMON Terminal.

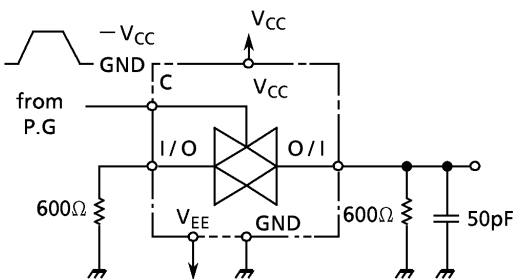
NOTE : These characteristics are determined by design of devices.

SWITCHING CHARACTERISTICS TEST CIRCUITS

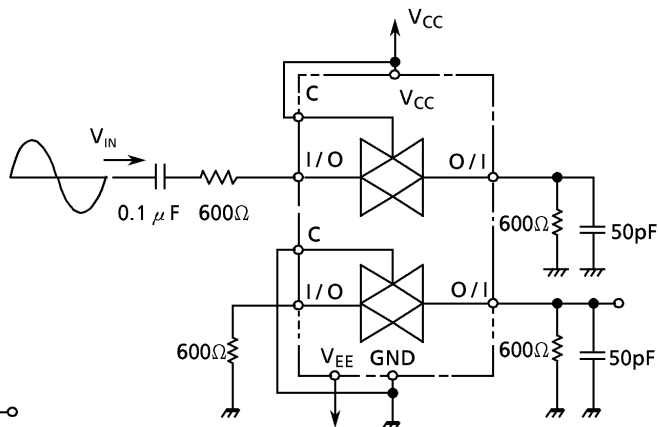
1.  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$



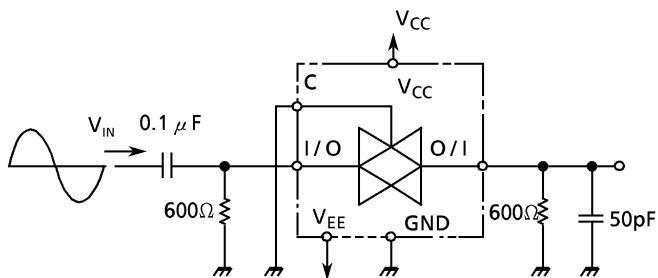
2. CROSS TALK (CONTROL INPUT - SWITCH OUTPUT)  
 $f_{in} = 1\text{MHz}$  duty = 50%  $t_r = t_f = 6\text{ns}$



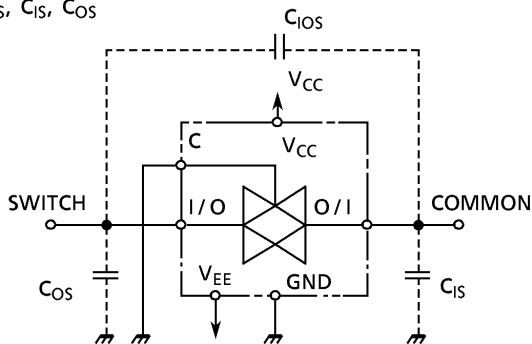
5. CROSS TALK (BETWEEN ANY TWO SWITCHES)



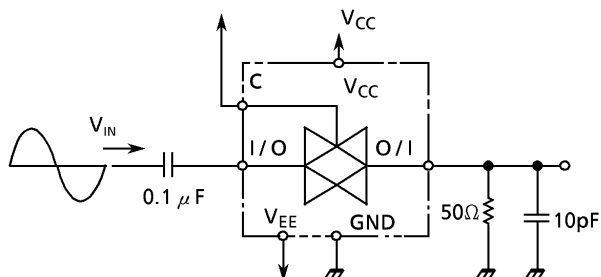
3. FEEDTHROUGH ATTENUATION



4.  $C_{iOs}$ ,  $C_{iS}$ ,  $C_{oS}$

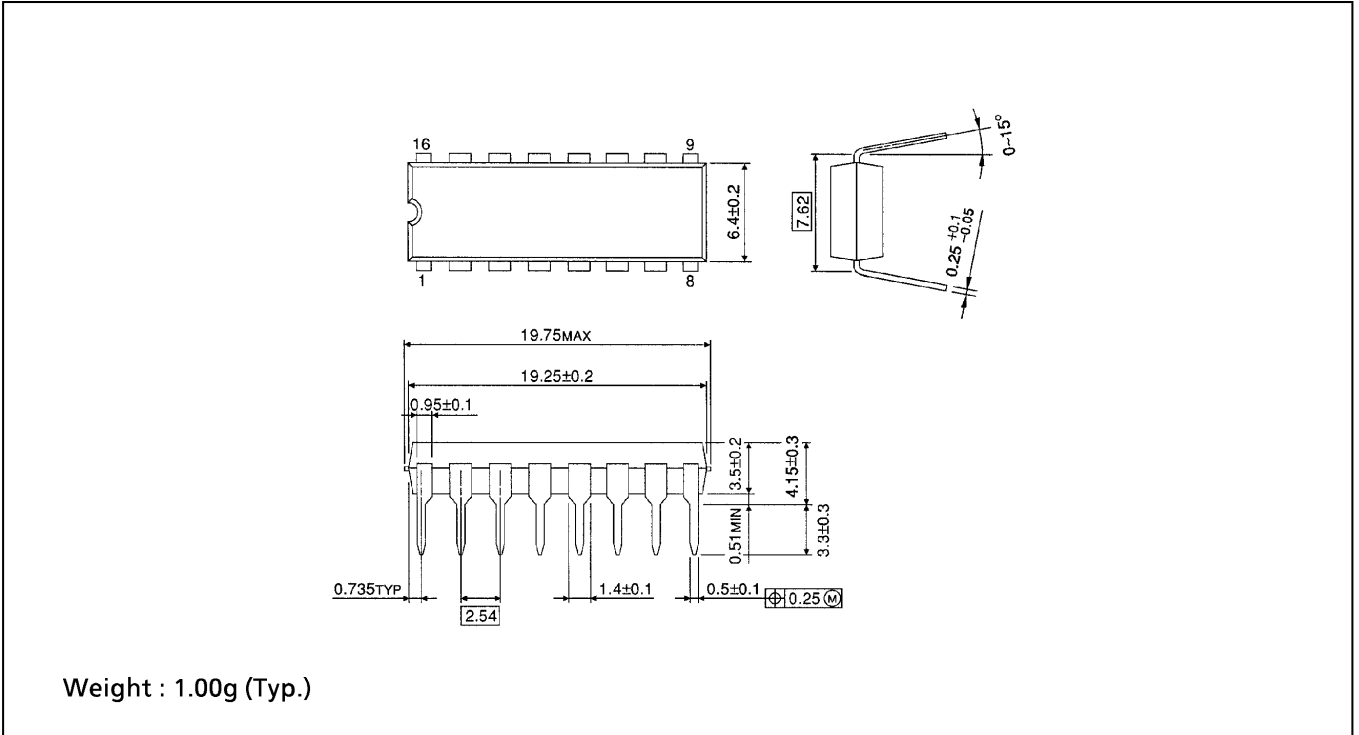


6. FREQUENCY RESPONSE (SWITCH ON)



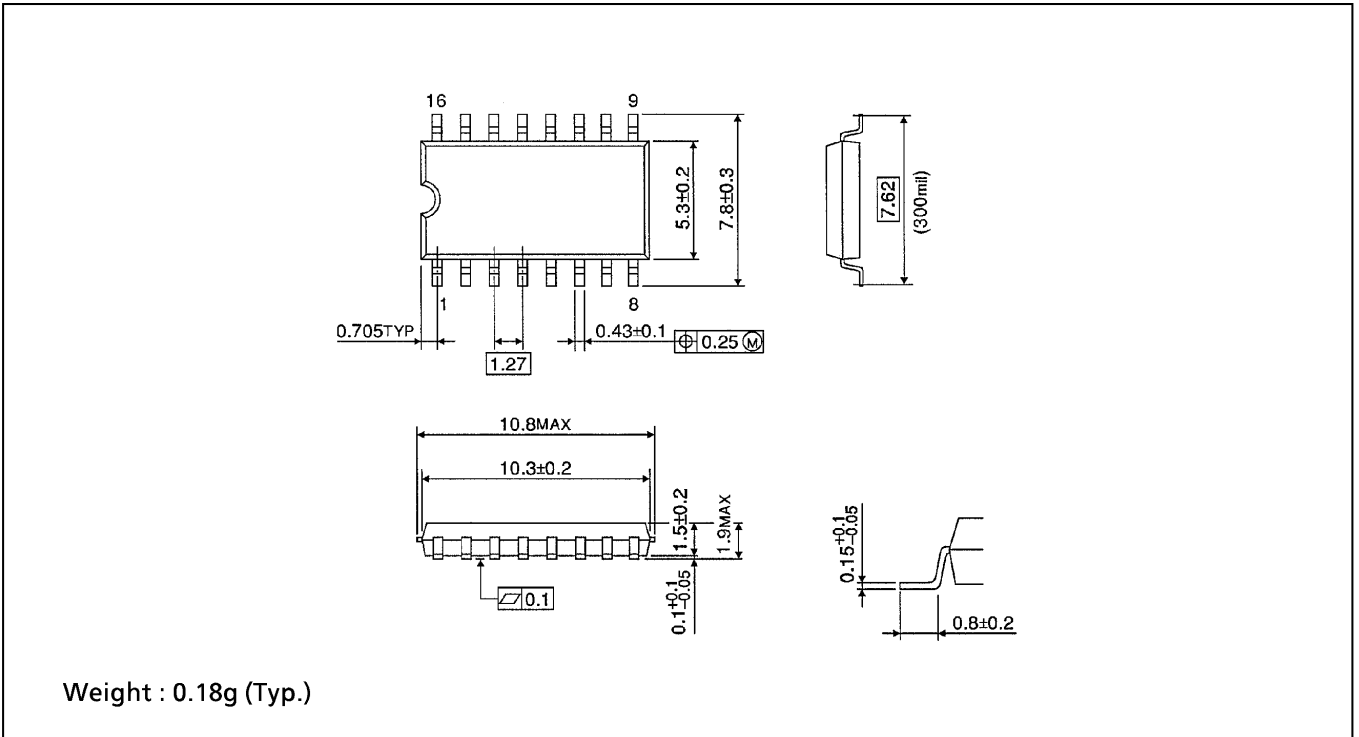
**DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)**

Unit in mm



**SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)**

Unit in mm

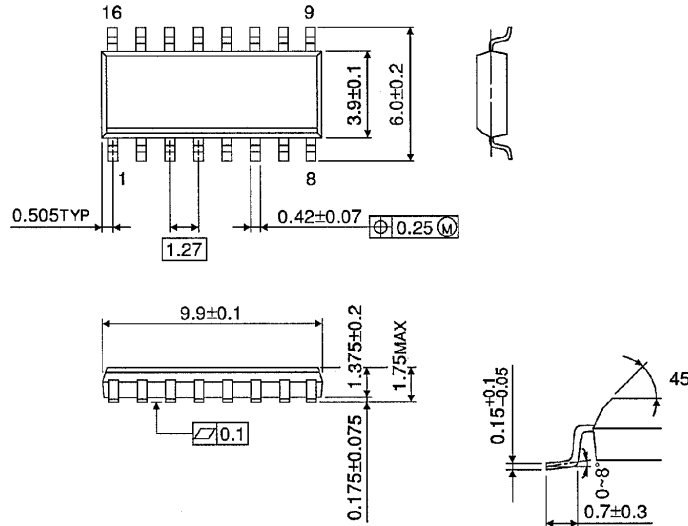




**SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)**

Unit in mm

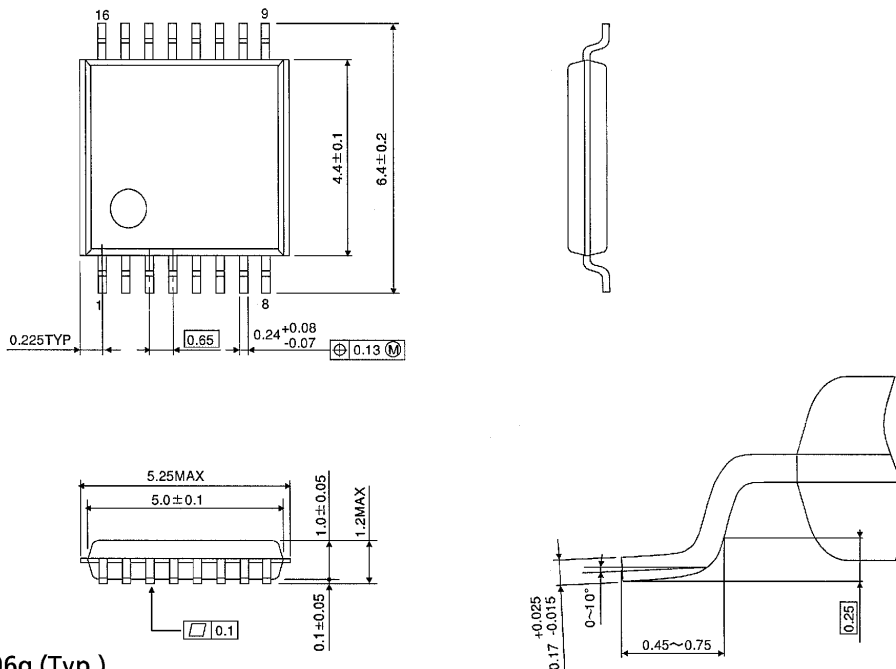
(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

**TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65)**

Unit in mm



Weight : 0.06g (Typ.)