

SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

- Eight Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- pnp Inputs Reduce dc Loading on Data Lines

description

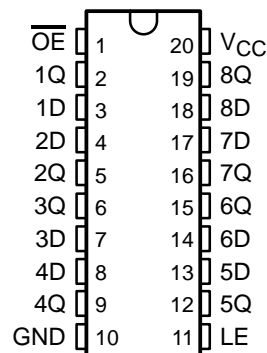
These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

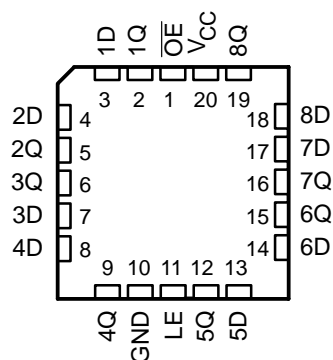
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

SN54ALS373A, . . . J OR W PACKAGE
SN54AS373 . . . J PACKAGE
SN74ALS373A, SN74AS373 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS373A, SN54AS373 . . . FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

ORDERING INFORMATION

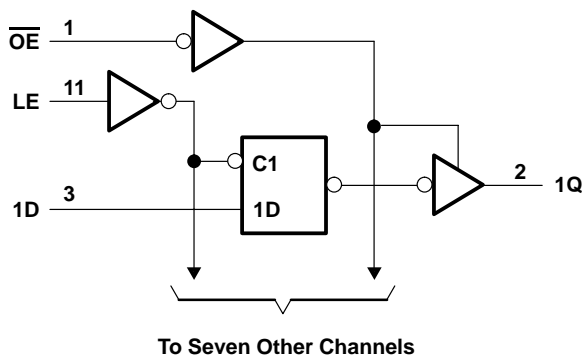
T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	PDIP – N	Tube	SN74ALS373AN	SN74ALS373AN	
			SN74AS373N	SN74AS373N	
	SOIC – DW	Tube	SN74ALS373ADW	ALS373A	
			SN74ALS373ADWR		
			Tube	SN74AS373DW	AS373
				SN74AS373DWR	
	SOP – NS	Tape and reel	SN74ALS373ANSR	ALS373A	
SN74AS373NSR			74AS373		
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS373AJ	SNJ54ALS373AJ	
			SNJ54AS373J	SNJ54AS373J	
	CFP – W	Tube	SNJ54ALS373AW	SNJ54ALS373AW	
	LCCC – FK	Tube	SNJ54ALS373AFK	SNJ54ALS373AFK	
			SNJ54AS373FK	SNJ54AS373FK	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic diagram (positive logic)



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

absolute maximum ratings over operating free-air temperature range (SN54ALS373A, SN74ALS373A) (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to any output in the high state or power-off state	5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54ALS373A			SN74ALS373A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ALS373A		SN74ALS373A		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_w	Pulse duration, LE high	12		10		ns
t_{su}	Setup time, data before LE↓	10		10		ns
t_h	Hold time, data after LE↓	7		7		ns



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS373A			SN74ALS373A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$		-1.5			-1.5			V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$		$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.4	3.3					
		$I_{OH} = -2.6\text{ mA}$				2.4	3.2		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	0.25	0.4			V
		$I_{OL} = 24\text{ mA}$				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$	20			20			μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$	-20			-20			μA
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$	0.1			0.1			mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$	20			20			μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$	-0.1			-0.1			mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	-20	-112	-30	-112			mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	9	16	9	16			mA
		Outputs low	16	25	16	25			
		Outputs disabled	17	27	17	27			

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$				UNIT
			SN54ALS373A		SN74ALS373A		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	17	2	12	ns
t_{PHL}			1	19	4	16	
t_{PLH}	LE	Any Q	6	29	6	22	ns
t_{PHL}			1	27	7	23	
t_{PZH}	\overline{OE}	Any Q	6	22	1	18	ns
t_{PZL}			5	24	5	20	
t_{PHZ}	\overline{OE}	Any Q	2	16	1	10	ns
t_{PLZ}			2	24	2	12	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

absolute maximum ratings over operating free-air temperature range (SN54AS373, SN74AS373) (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to any output in the high state or power-off state	5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54AS373			SN74AS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54AS373		SN74AS373		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_w	Pulse duration, LE high	5.5*		4.5*		ns
t_{su}	Setup time, data before LE↓	2*		2*		ns
t_h	Hold time, data after LE↓	3*		3*		ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS373			SN74AS373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$		$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -12\text{ mA}$	2.4	3.2					
		$I_{OH} = -15\text{ mA}$					2.4	3.3	
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 32\text{ mA}$	0.27		0.5				V
		$I_{OL} = 48\text{ mA}$					0.32	0.5	
I_{OZH}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$	50			50			μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$	-50			-50			μA
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$	0.1			0.1			mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$	20			20			μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$	-0.02	-0.5		-0.02	-0.5		mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	-30	-112		-30	-112		mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	55	90		55	90		mA
		Outputs low	55	85		55	85		
		Outputs disabled	65	100		65	100		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$				UNIT
			SN54AS373		SN74AS373		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	9	3.5	6	ns
t_{PHL}			3	8	3.5	6	
t_{PLH}	LE	Any Q	6.5	14.5	6.5	11.5	ns
t_{PHL}			5	9	5	7.5	
t_{PZH}	\overline{OE}	Any Q	2	7.5	2	6.5	ns
t_{PZL}			4.5	10.5	4.5	9.5	
t_{PHZ}	\overline{OE}	Any Q	3	10	3	6.5	ns
t_{PLZ}			3	8	3	7	

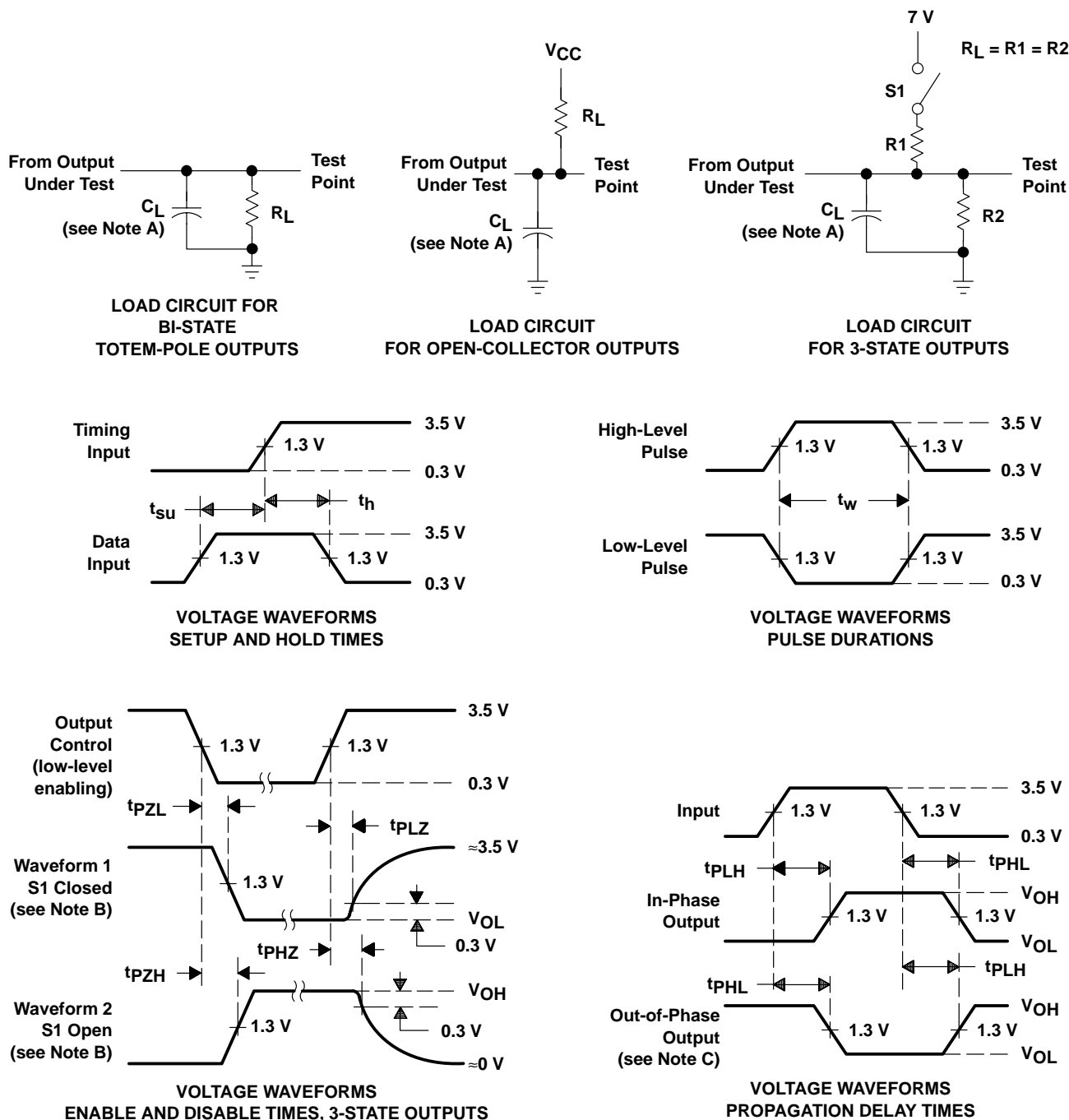
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - When measuring propagation delay items of 3-state outputs, switch S1 is open.
 - All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265