SN54HCT02, SN74HCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

SCLS065B - NOVEMBER 1988 - REVISED MAY 1997

Inputs Are TTL-Voltage Compatible

 Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

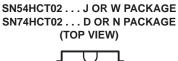
description

These devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54HCT02 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74HCT02 is characterized for operation from -40° C to 85° C.

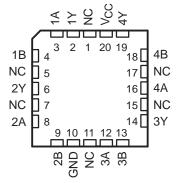
FUNCTION TABLE (each gate)								
INP	UTS	OUTPUT						
Α	В	Y						
Н	Х	L						
Х	Н	L						
L	L	н						

logic symbol[†]

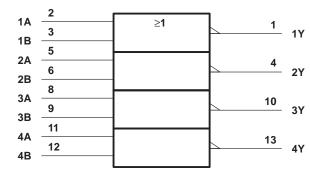


		1 1		
1Y [1	\cup	14] ∨ _{cc}
1A [2		13] 4Y
	3		12] 4B
2Y [4		11] 4A
2A [5		10] 3Y
_			9] 3B
GND [7		8] 3A

SN54HCT02 . . . FK PACKAGE (TOP VIEW)

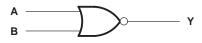


NC - No internal connection



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range[†]

Supply voltage range, V_{CC} Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	
Output clamp current, I_{R} ($V_{O} < 0$ or $V_{O} > V_{CC}$) (see Note 1)	
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	
Continuous current through V _{CC} or GND	
Package thermal impedance, θ_{JA} (see Note 2): D package	127°C/W
N package	78°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN	SN54HCT02		SN74HCT02			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	\$ 5.5	4.5	5	5.5	V
VIH	High-level input voltage	$V_{CC} = 4.5 V \text{ to } 5.5 V$	2	ľ.	5,	2			V
VIL	Low-level input voltage	$V_{CC} = 4.5 V \text{ to } 5.5 V$	0	R	0.8	0		0.8	V
VI	Input voltage		0	E.	VCC	0		VCC	V
VO	Output voltage		0	20	VCC	0		VCC	V
tt	Input transition (rise and fall) time		<u>9</u> C	5	500	0		500	ns
ТА	Operating free-air temperature		-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		vcc	T _A = 25°C			SN54HCT02		SN74HCT02		UNIT
PARAMETER				MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
Vou	V _{OH} V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		V
VOH		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7	N	3.84		
Ve	$V_{I} = V_{IH} \text{ or } V_{IL}$	I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
VOL		$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	v
lj	VI = VCC or 0		5.5 V		±0.1	±100	1	±1000		±1000	nA
ICC	$V_I = V_{CC} \text{ or } 0,$	IO = 0	5.5 V			2	DNG	40		20	μA
ΔI_{CC}^{\ddagger}	One input at 0.5 V of Other inputs at 0 or		5.5 V		1.4	2.4	PRO1	3		2.9	mA
Ci			4.5 V to 5.5 V		3	10		10		10	pF

 \ddagger This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.



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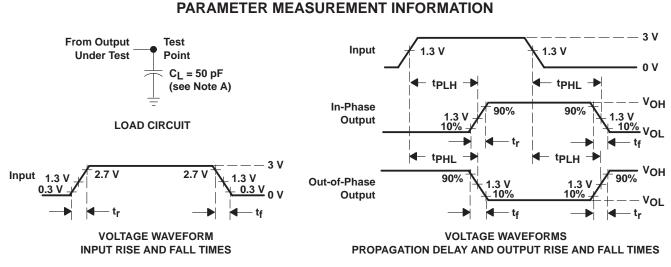
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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	Vaa	Τį	λ = 25°C	;	SN54HCT02	SN74HCT02	UNIT
PARAMETER	(INPUT)	(OUTPUT)	Vcc	MIN	TYP	MAX	MIN MAX	MIN MAX	UNIT
.	A or B	Y	4.5 V		11	20	30	25	-
^t pd	AOIB			5.5 V		10	18	27	22
• .		V	4.5 V		9	15	22	19	-
t		T	5.5 V		8	14	20	17	ns

operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	No load	20	pF



- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 6 ns, t_f = 6 ns.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms



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