TEXAS INSTRUMENTS

CD54/74HC534, CD54/74HCT534, CD54/74HC564, CD54/74HCT564

High Speed CMOS Logic Octal D-Type Flip-Flop, Three-State Inverting Positive-Edge Triggered

Features

- **Buffered Inputs**

- **Common Three-State Output-Enable Control**

- **Three-State Outputs**

- **Bus Line Driving Capability**

- **Typical Propagation Delay = 13ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C (Clock to Output)**

- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**

- **Wide Operating Temperature Range . . . -55°C to 125°C**

- **Balanced Propagation Delay and Transition Times**

- **Significant Power Reduction Compared to LSTTL Logic ICs**

- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The 'HC534, 'HCT534, 'HC564, and 'HCT564 are high speed Octal D-Type Flip-Flops manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL loads. Due to the large output drive capability and the three-state feature, these devices are ideally suited for interfacing with bus lines in a bus organized system. The two types are functionally identical and differ only in their pinout arrangements.

The 'HC534, 'HCT534, 'HC564, and 'HCT564 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are inverted and transferred to the Q outputs on the positive going transition of the CLOCK input. When a high logic level is applied to the OUTPUT ENABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The HCT logic family is speed, function, and pin compatible with the standard LS logic family.

Ordering Information

| PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC534F3A	-55 to 125	20 Ld CERDIP
CD74HC534E	-55 to 125	20 Ld PDIP
CD54HCT534F3A	-55 to 125	20 Ld CERDIP
CD74HCT534E	-55 to 125	20 Ld PDIP
CD54HC564F3A	-55 to 125	20 Ld CERDIP
CD74HC564E	-55 to 125	20 Ld PDIP
CD74HC564M	-55 to 125	20 Ld SOIC
CD54HCT564F3A	-55 to 125	20 Ld CERDIP
CD74HCT564E	-55 to 125	20 Ld PDIP
CD74HCT564M	-55 to 125	20 Ld SOIC

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Pinouts

CD54HC534, CD54HCT534
(CERDIP)
CD74HC534, CD74HCT534
(PDIP)
TOP VIEW

$\overline{OE}$	1	20	V_{CC}
$\overline{Q0}$	2	19	$\overline{Q7}$
D0	3	18	D7
D1	4	17	D6
$\overline{Q1}$	5	16	$\overline{Q6}$
$\overline{Q2}$	6	15	$\overline{Q5}$
D2	7	14	D5
D3	8	13	D4
$\overline{Q3}$	9	12	$\overline{Q4}$
GND	10	11	$\overline{CP}$
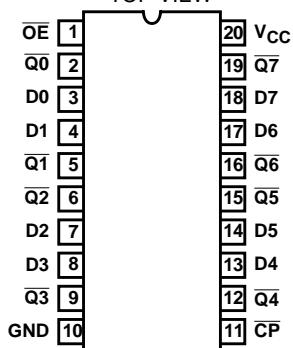
CD54HC564, CD54HCT564
(CERDIP)
CD74HC564, CD74HCT564
(PDIP, SOIC)
TOP VIEW

$\overline{OE}$	1	20	V_{CC}
D0	2	19	$\overline{Q0}$
D1	3	18	$\overline{Q1}$
D2	4	17	$\overline{Q2}$
D3	5	16	$\overline{Q3}$
D4	6	15	$\overline{Q4}$
D5	7	14	$\overline{Q5}$
D6	8	13	$\overline{Q6}$
D7	9	12	$\overline{Q7}$
GND	10	11	CP
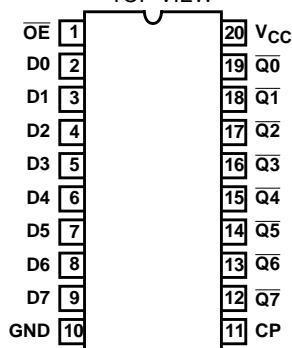
Functional Diagram
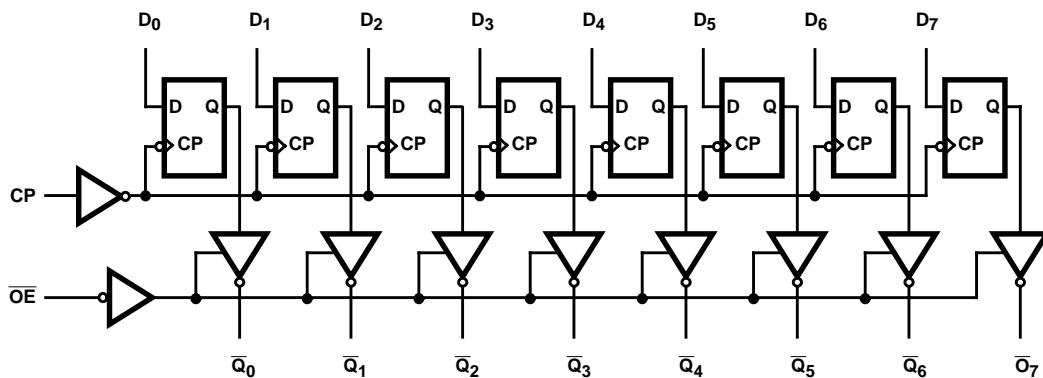
TRUTH TABLE

INPUTS			OUTPUT
$\overline{OE}$	CP	Dn	$\overline{Qn}$
L	↑	H	L
L	↑	L	H
L	L	X	No Change
H	X	X	Z

NOTE:
H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↑ = Transition from Low to High Level
Z = High Impedance State

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
   For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . $\pm$20mA
DC Output Diode Current, I_{OK}
   For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . $\pm$20mA
DC Drain Current, per Output, I_O
   For -0.5V < V_O < V_{CC} + 0.5V . . . . $\pm$35mA
DC Output Source or Sink Current per Output Pin, I_O
   For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . $\pm$25mA
DC V_{CC} or Ground Current, I_{CC} . . . . $\pm$50mA

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (^{o}C/W)
   PDIP Package   125
   SOIC Package   120
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
  (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
   HC Types . . . . .2V to 6V
   HCT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V . . . . 500ns (Max)
  6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	$\pm$0.1	-	$\pm$1	-	$\pm$1	μA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V$_I$ (V)	TEST CONDITIONS I$_O$ (mA)	V$_{CC}$ (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Quiescent Device Current	I$_{CC}$	V$_{CC}$ or GND	0	6	-	-	8	-	80	-	160	µA
Three- State Leakage Current	V$_{IL}$ or V$_{IH}$	V$_O$ = V$_{CC}$ or GND	-	6	-	-	±0.5	-	±5.0	-	±10	µA
HCT TYPES												
High Level Input Voltage	V$_{IH}$	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V$_{IL}$	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V$_{OH}$	V$_{IH}$ or V$_{IL}$	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V$_{OL}$	V$_{IH}$ or V$_{IL}$	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I$_I$	V$_{CC}$ and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I$_{CC}$	V$_{CC}$ or GND	0	5.5	-	-	8	-	80	-	160	µA
Three- State Leakage Current	V$_{IL}$ or V$_{IH}$	V$_O$ = V$_{CC}$ or GND	-	5.5	-	-	±0.5	-	±5.0	-	±10	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI$_{CC}$	V$_{CC}$ -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE: For dual-supply systems theoretical worst case (V$_I$ = 2.4V, V$_{CC}$ = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
D0 - D7	0.15
CP	0.30
$\overline{OE}$	0.55

NOTE: Unit load is ΔI$_{CC}$ limit specific in DC Electrical Specifications Table, e.g., 360µA max. at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Maximum Clock Frequency	f_{MAX}	2	6	-	-	5	-	-	4	-	-	MHz
		4.5	30	-	-	25	-	-	20	-	-	MHz
		6	35	-	-	29	-	-	23	-	-	MHz
Clock Pulse Width	t_W	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Setup Time Data to Clock	t_{SU}	2	60	-	-	75	-	-	90	-	-	ns
		4.5	12	-	-	15	-	-	18	-	-	ns
		6	10	-	-	13	-	-	15	-	-	ns
Hold Time Data to Clock	t_H	2	5	-	-	5	-	-	5	-	-	ns
		4.5	5	-	-	5	-	-	5	-	-	ns
		6	5	-	-	5	-	-	5	-	-	ns
HCT TYPES												
Maximum Clock Frequency	f_{MAX}	4.5	25	-	-	20	-	-	16	-	-	MHz
Clock Pulse Width	t_W	4.5	20	-	-	25	-	-	30	-	-	ns
Setup Time Data to Clock	t_{SU}	4.5	20	-	-	25	-	-	30	-	-	ns
Hold Time Data to Clock (534)	t_H	4.5	5	-	-	5	-	-	5	-	-	ns
Hold Time Data to Clock (564)	t_H	4.5	3	-	-	3	-	-	3	-	-	ns

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay Clock to Output	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	165	-	205	-	250	ns
			4.5	-	-	33	-	41	-	50	ns
		C_L = 15pF	5	-	13	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	28	-	35	-	43	ns
Output Disable to Q (534)	t_{PLZ}, t_{PHZ}	C_L = 50pF	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	26	-	33	-	38	ns

Switching Specifications C_L = 50pF, Input t_r, t_f = 6ns **(Continued)**

| PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Output Disable to Q (564)	t_{PLZ}, t_{PHZ}	C_L = 50pF	2	-	-	135	-	170	-	205	ns
			4.5	-	-	27	-	34	-	41	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	23	-	29	-	35	ns
Output Enable to Q	t_{PZL}, t_{PZH}	C_L = 50pF	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	26	-	33	-	38	ns
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	5	-	60	-	-	-	-	-	MHz
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Input Capacitance	C_I	C_L = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	C_O	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	32	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay Clock to Output	t_{PHL}, t_{PLH}	C_L = 50pF	4.5	-	-	35	-	44	-	53	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
Output Disable to Q	t_{PLZ}, t_{PHZ}	C_L = 50pF	4.5	-	-	30	-	38	-	45	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
Output Enable to Q	t_{PZL}, t_{PZH}	C_L = 50pF	4.5	-	-	35	-	44	-	53	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
Maximum Clock Frequency	f_{MAX}	C_L = 15pF	5	-	50	-	-	-	-	-	MHz
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	12	-	15	-	18	ns
Input Capacitance	C_I	C_L = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	C_O	-	-	20	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	-	36	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per package.

5. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_O$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.
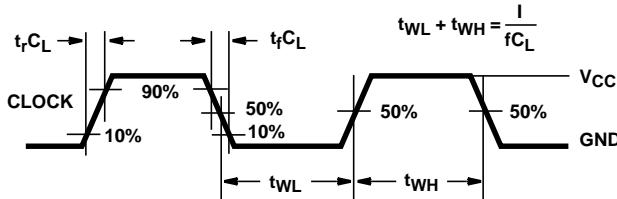
CD54/74HC534, CD54/74HCT534, CD54/74HC564, CD54/74HCT564

Test Circuits and Waveforms

NOTE: Outputs should be switching from 10% V_CC to 90% V_CC in accordance with device truth table. For f_MAX, input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**
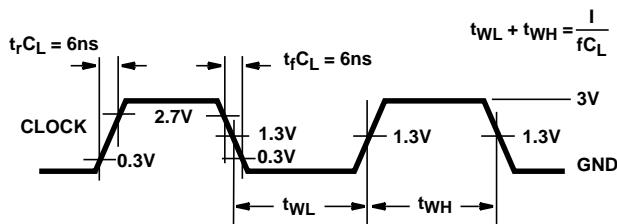
NOTE: Outputs should be switching from 10% V_CC to 90% V_CC in accordance with device truth table. For f_MAX, input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH
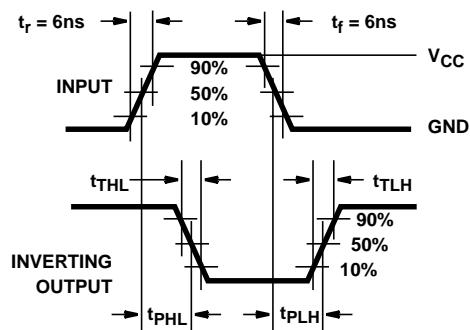
FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC
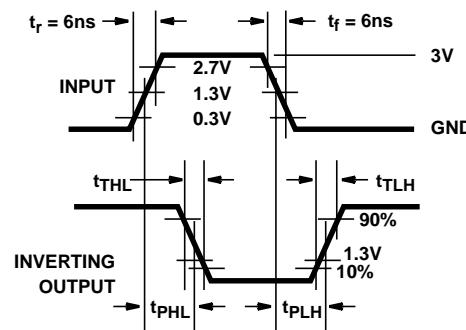
FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC
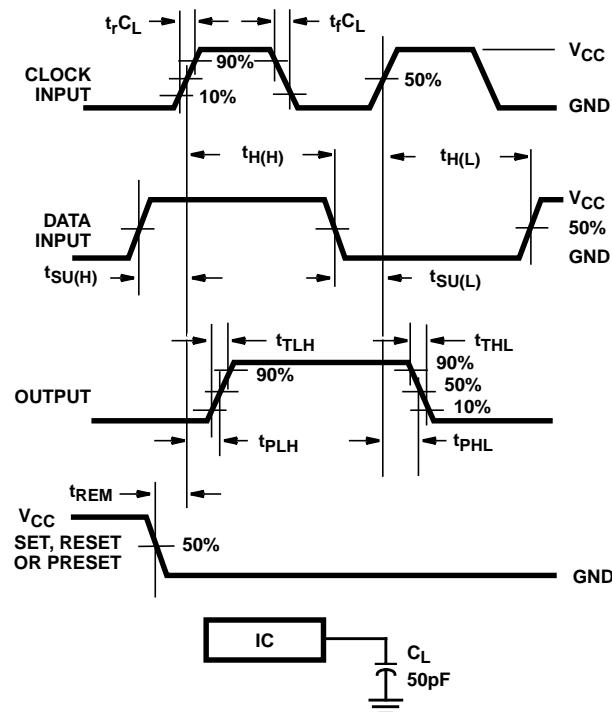
FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS
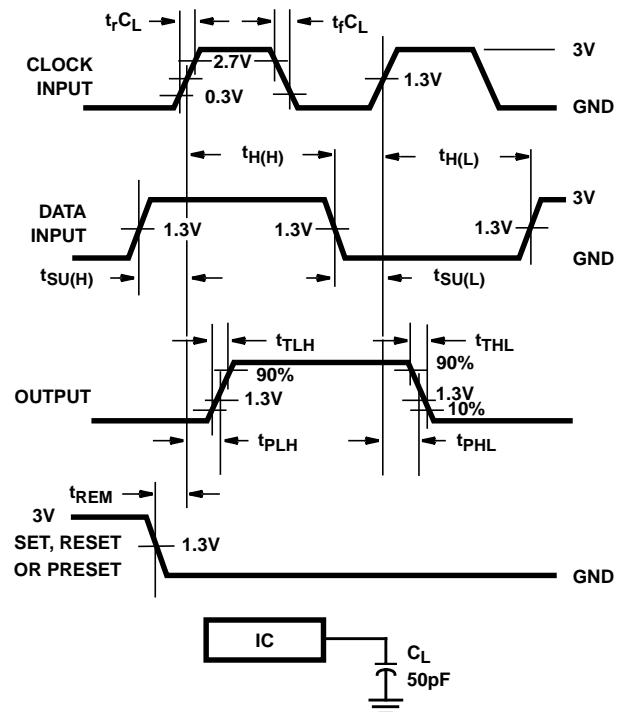
FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)
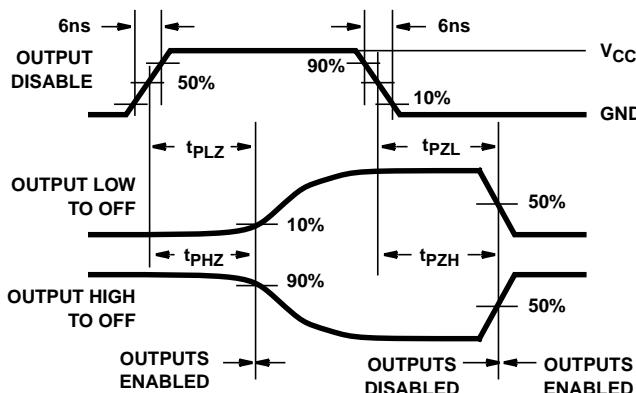
**FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM**
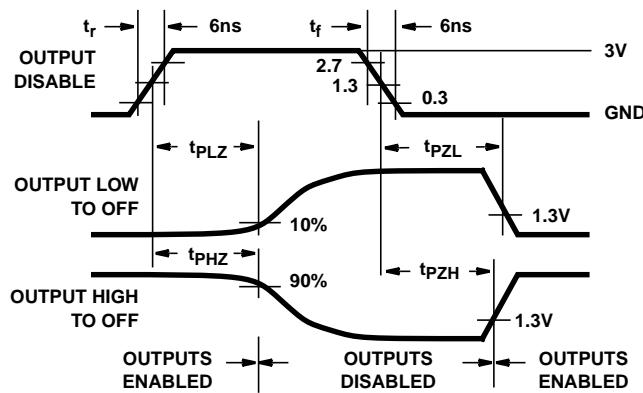
FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM
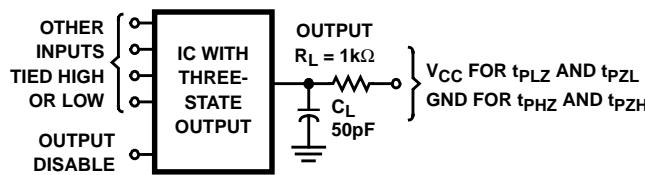
NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC}, $C_L = 50pF$.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

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