Data sheet acquired from Harris Semiconductor
SCHS187A

January 1998 - Revised May 2000

CD54/74HC533, CD54/74HCT533, CD54/74HC563, CD74HCT563

High Speed CMOS Logic Octal Inverting Transparent Latch, Three-State Outputs

Features

- **Common Latch-Enable Control**
- **Common Three-State Output Enable Control**
- **Buffered Inputs**
- **Three-State Outputs**
- **Bus Line Driving Capacity**
- **Typical Propagation Delay = 13ns at V_{CC} = 5V, C_L = 15pF, T_A = 25^{o}C (Data to Output)**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{o}C to 125^{o}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The ’HC533, ’HCT533, ’HC563, and CD74HCT563 are high speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices.

The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the three-state outputs. When the output enable ($\overline{OE}$) is high the outputs are in the high impedance state. The latch operation is independent of the state of the output enable.

The ’HC533 and ’HCT533 are identical in function to the ’HC563 and CD74HCT563 but have different pinouts. The ’HC533 and ’HCT533 are similar to the ’HC373 and ’HCT373; the latter are non-inverting types.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD54HC533F3A	-55 to 125	20 Ld CERDIP
CD74HC533E	-55 to 125	20 Ld PDIP
CD54HCT533F3A	-55 to 125	20 Ld CERDIP
CD74HCT533E	-55 to 125	20 Ld PDIP
CD54HC563F3A	-55 to 125	20 Ld CERDIP
CD74HC563E	-55 to 125	20 Ld PDIP
CD74HCT563E	-55 to 125	20 Ld PDIP
CD74HCT563M	-55 to 125	20 Ld SOIC

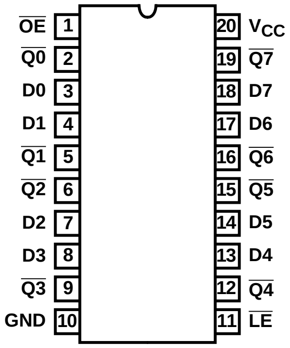
NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number are available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

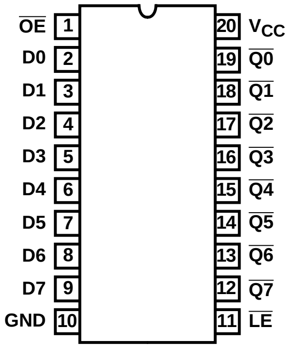
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Pinouts

CD54HC533, CD54HCT533
(CERDIP)
CD74HC533, CD74HCT533
(PDIP, SOIC)
TOP VIEW

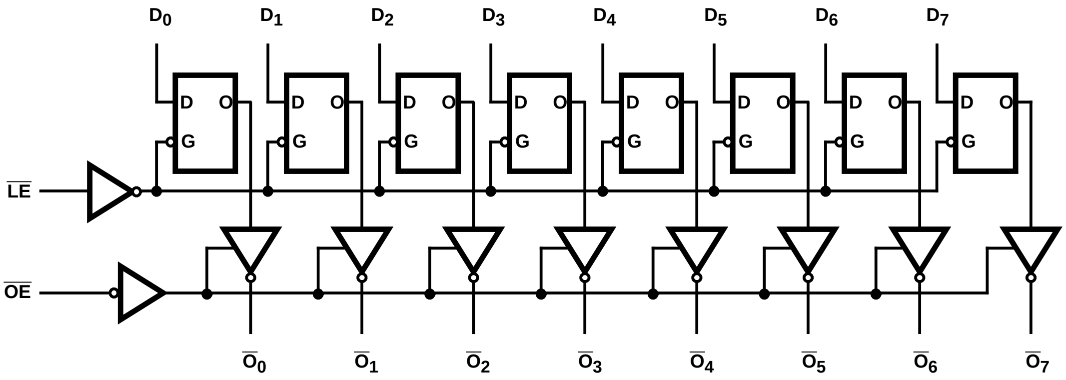


CD54HC563
(CERDIP)
CD74HC563, CD74HCT563
(PDIP, SOIC)
TOP VIEW



Functional Block Diagram

HC/HCT533



TRUTH TABLE

$\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$	$\overline{\text{LATCH}}$ $\overline{\text{ENABLE}}$	DATA	Q OUTPUT
L	H	H	L
L	H	L	H
L	L	l	H
L	L	h	L
H	X	X	Z

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don’t Care, Z = High Impedance State, l = Low voltage level one set-up time prior to the high to low latch enable transition, h = High voltage level one set-up time prior to the high to low latch enable transition.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
  For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
  For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Drain Current, per Output, I_O
  For -0.5V < V_O < V_{CC} + 0.5V . . . . ±35mA
DC Output Source or Sink Current per Output Pin, I_O
  For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . -55^{o}C to 125^{o}C
Supply Voltage Range, V_{CC}
  HC Types . . . . 2V to 6V
  HCT Types . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V. . . . . 500ns (Max)
  6V . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (^{o}C/W)
  PDIP Package 125
  SOIC Package 120
Maximum Junction Temperature . . . . 150^{o}C
Maximum Storage Temperature Range . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . 300^{o}C
  (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

		TEST CONDITIONS			25^{o}C			-40^{o}C TO 85^{o}C		-55^{o}C TO 125^{o}C		
PARAMETER	**SYMBOL**	**V_I (V)**	**I_O (mA)**	**V_{CC} (V)**	**MIN**	**TYP**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Three-State Leakage Current	-	V_{IL} or V_{IH}	V_O = V_{CC} or GND	6	-	-	±0.5	-	±5	-	±10	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	-	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Three-State Leakage Current	-	V_{IL} or V_{IH}	V_O = V_{CC} or GND	5.5	-	-	±0.5	-	±5	-	±10	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
D0 - D7	0.15
$\overline{LE}$	0.30
$\overline{OE}$	0.55

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25^{o}C			-40^{o}C TO 85^{o}C		-55^{o}C TO 125^{o}C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
$\overline{LE}$ Pulse Width	t_W	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Set-up Time Data to $\overline{LE}$	t_{SU}	-	2	50	-	-	65	-	75	-	ns
			4.5	10	-	-	13	-	15	-	ns
			6	9	-	-	11	-	13	-	ns
Hold Time, Data to $\overline{LE}$ (533)	t_H	-	2	35	-	-	45	-	55	-	ns
			4.5	7	-	-	9	-	11	-	ns
			6	6	-	-	8	-	7	-	ns
Hold Time, Data to $\overline{LE}$ (563)	t_H	-	2	4	-	-	4	-	4	-	ns
			4.5	4	-	-	4	-	4	-	ns
			6	4	-	-	4	-	4	-	ns
HCT TYPES											
$\overline{LE}$ Pulse Width	t_W	-	4.5	16	-	-	20	-	24	-	ns
Set-up Time Data to $\overline{LE}$	t_W	-	4.5	10	-	-	13	-	15	-	ns
Hold Time, Data to $\overline{LE}$ (533)	t_H	-	4.5	8	-	-	10	-	12	-	ns
Hold Time, Data to $\overline{LE}$ (563)	t_H	-	4.5	5	-	-	5	-	5	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25^{o}C		-40^{o}C TO 85^{o}C	-55^{o}C TO 125^{o}C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, Data to Qn (HC533)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	165	205	250	ns
			4.5	-	33	41	50	ns
			6	-	28	35	43	ns
		C_L = 15pF	5	13	-	-	-	ns
Propagation Delay, Data to Qn (HC563)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		C_L = 15pF	5	12	-	-	-	ns
Propagation Delay, $\overline{LE}$ to Qn (HC533)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
			6	-	30	37	45	ns
		C_L = 15pF	5	14	-	-	-	ns
Propagation Delay, $\overline{LE}$ to Qn (HC563)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	165	205	250	ns
			4.5	-	33	41	50	ns
			6	-	28	35	43	ns
		C_L = 15pF	5	13	-	-	-	ns

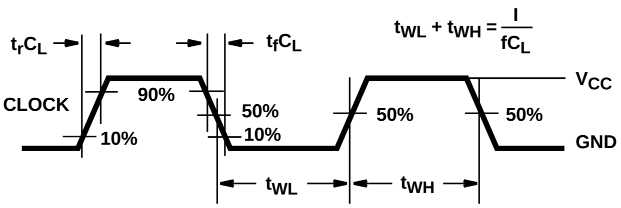
Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Enable Times (HC533)	t_{PZH}, t_{PZL}	C_L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		C_L = 15pF	5	12	-	-	-	ns
Disable Times (HC533)	t_{PHZ}, t_{PLZ}	C_L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		C_L = 15pF	5	12	-	-	-	ns
Enable and Disable Times (HC563)	t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	C_L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		C_L = 15pF	5	12	-	-	-	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
Three-State Output Capacitance	C_O	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	42	-	-	-	pF
HCT TYPES								
Propagation Delay, Data to Qn (HC/HCT533)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	34	43	51	ns
		C_L = 15pF	5	14	-	-	-	ns
Propagation Delay, Data to Qn (HC/HCT563)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	30	38	45	ns
		C_L = 15pF	5	12	-	-	-	ns
Propagation Delay, $\overline{LE}$ to Qn (HC/HCT533)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	38	48	57	ns
		C_L = 15pF	5	16	-	-	-	ns
Propagation Delay, $\overline{LE}$ to Qn (HC/HCT563)	t_{PZL}, t_{PZH}	C_L = 50pF	4.5	-	35	44	53	ns
		C_L = 15pF	5	14	-	-	-	ns
Enable Times (HC/HCT533)	t_{PLZ}, t_{PZH}	C_L = 50pF	4.5	-	35	44	53	ns
		C_L = 15pF	5	14	-	-	-	ns
Disable Times (HC/HCT533)	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	30	38	45	ns
		C_L = 15pF	5	12	-	-	-	ns
Enable and Disable Times (HC/HCT563)	t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	C_L = 50pF	4.5	-	35	44	53	ns
		C_L = 15pF	5	14	-	-	-	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	42	-	-	-	pF

NOTES:

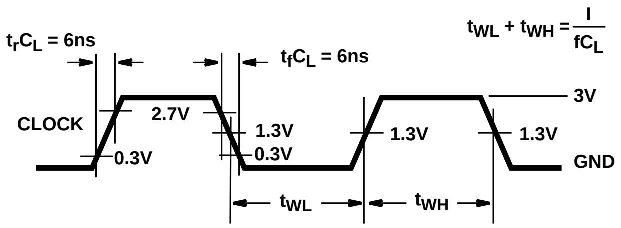
5. C_{PD} is used to determine the no-load dynamic power consumption, per latch.
6. P_D (total power per latch) = $C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$ where f_i = Input Frequency, f_o = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

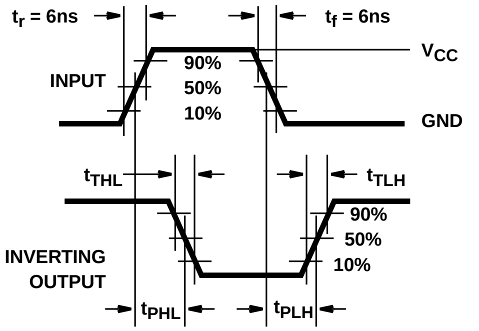


FIGURE 3. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

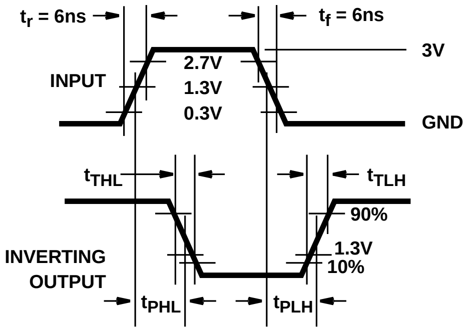


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

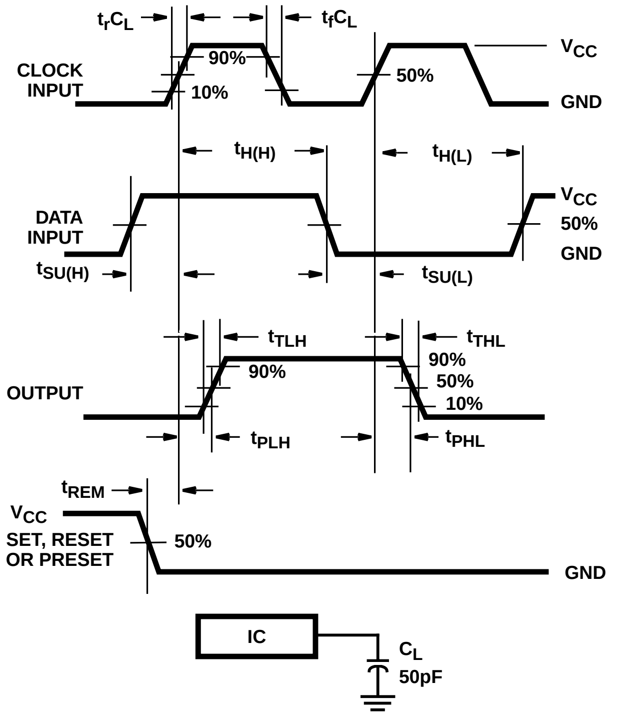


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

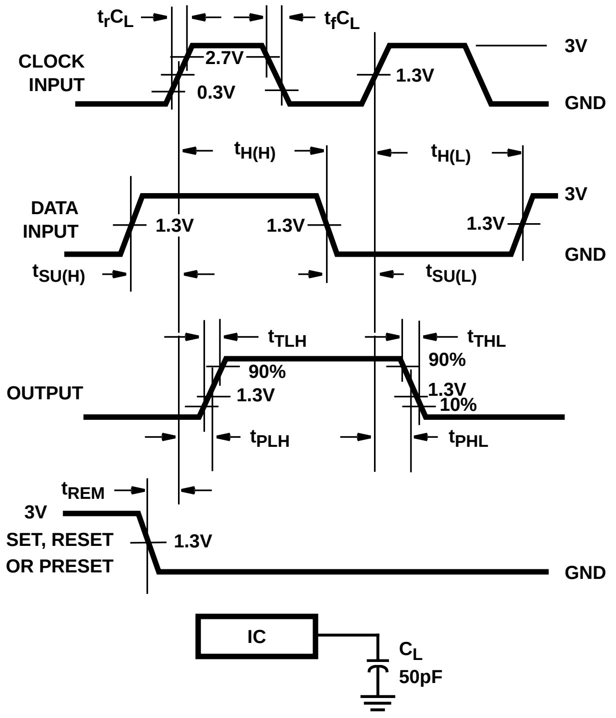


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

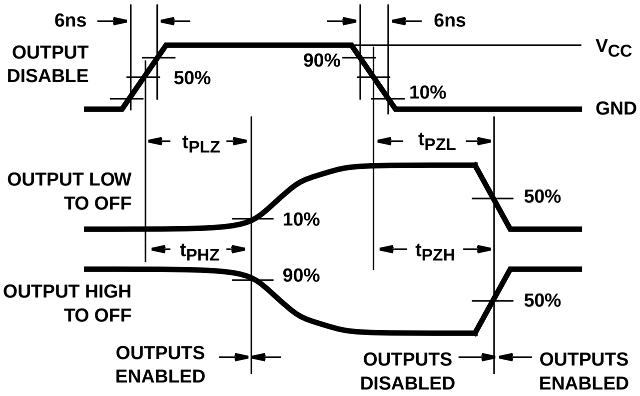


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

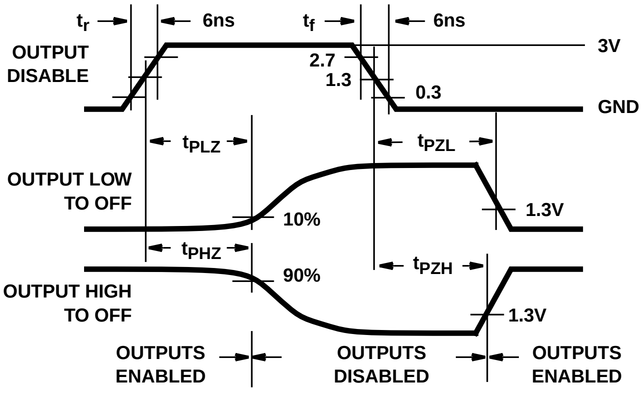
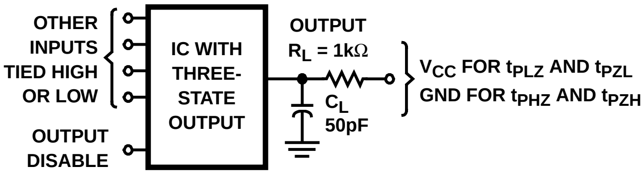


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC}, $C_L = 50pF$.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

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