ADS7822

SBAS062A – JANUARY 1996 – REVISED MARCH 2005

12-Bit, High-Speed, 2.7V *micro*Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **75kHz SAMPLING RATE**
- **MICRO POWER:**
  0.54mW at 75kHz
  0.06mW at 7.5kHz
- **POWER DOWN: 3μA max**
- **MINI-DIP-8, SOIC-8, AND MSOP-8**
- **PSEUDO-DIFFERENTIAL INPUT**
- **SERIAL INTERFACE**

APPLICATIONS

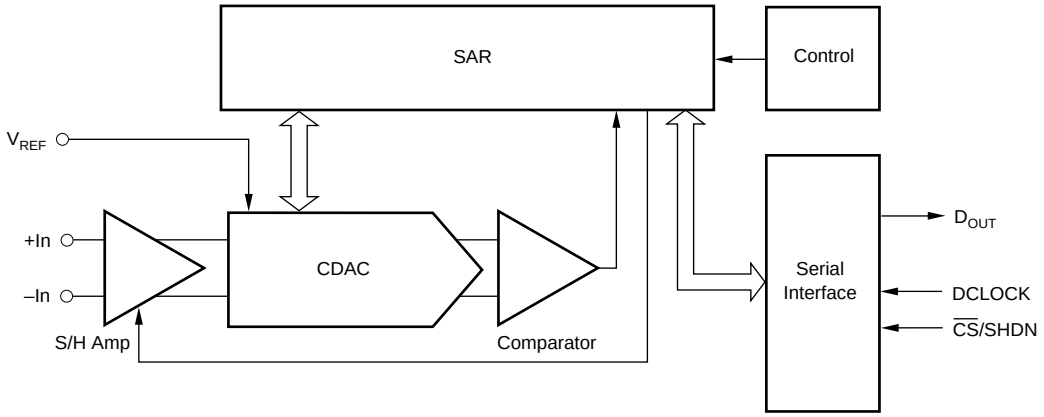
- **BATTERY-OPERATED SYSTEMS**
- **REMOTE DATA ACQUISITION**
- **ISOLATED DATA ACQUISITION**
- **SIMULTANEOUS SAMPLING, MULTI-CHANNEL SYSTEMS**

DESCRIPTION

The ADS7822 is a 12-bit sampling analog-to-digital (A/D) converter with ensured specifications over a 2.7V to 5.25V supply range. It requires very little power even when operating at the full 75kHz rate. At lower conversion rates, the high speed of the device enables it to spend most of its time in the power-down mode—the power dissipation is less than 60μW at 7.5kHz.

The ADS7822 also features operation from 2.0V to 5V, a synchronous serial interface, and a pseudo-differential input. The reference voltage can be set to any level within the range of 50mV to V_{CC}.

Ultra low power and small size make the ADS7822 ideal for battery-operated systems. It is also a perfect fit for remote data acquisition modules, simultaneous multi-channel systems, and isolated data acquisition. The ADS7822 is available in a plastic mini-DIP-8, an SOIC-8, or an MSOP-8 package.



SPECIFICATIONS: $+V_{CC}$ = +2.7V

At –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 75kHz, f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7822			ADS7822B			ADS7822C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT											
Full-Scale Input Span	+In – (–In)	0		V_{REF}	0		V_{REF}	0		V_{REF}	V
Absolute Input Range	+In	–0.2		V_{CC} +0.2	–0.2		V_{CC} +0.2	–0.2		V_{CC} +0.2	V
	–In	–0.2		+1.0	–0.2		+1.0	–0.2		+1.0	V
Capacitance			25			25			25		pF
Leakage Current			±1			±1			±1		µA
SYSTEM PERFORMANCE											
Resolution			12			12			12		Bits
No Missing Codes		11			12			11			Bits
Integral Linearity Error		–2	±0.5	+2	–1	±0.5	+1	–0.75	±0.25	+0.75	LSB[1]
Differential Linearity Error		–2	±0.5	+2	–1	±0.5	+1	–0.75	±0.25	+0.75	LSB
Offset Error		–3		+3	–3		+3	–1		+1	LSB
Gain Error		–3		+3	–3		+3	–1		+1	LSB
Noise			33			33			33		µVrms
Power Supply Rejection			82			82			82		dB
SAMPLING DYNAMICS											
Conversion Time				12			12			12	Clk Cycles
Acquisition Time		1.5			1.5			1.5			Clk Cycles
Throughput Rate				75			75			75	kHz
DYNAMIC CHARACTERISTICS											
Total Harmonic Distortion	V_{IN} = 2.5Vp-p at 1kHz		–82			–82			–82		dB
SINAD	V_{IN} = 2.5Vp-p at 1kHz		71			71			71		dB
Spurious Free Dynamic Range	V_{IN} = 2.5Vp-p at 1kHz		86			86			86		dB
REFERENCE INPUT											
Voltage Range		0.05		V_{CC}	0.05		V_{CC}	0.05		V_{CC}	V
Resistance	$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			5			5		GΩ
	$\overline{CS}$ = V_{CC}		5			5			5		GΩ
Current Drain	At Code 710h		8	40		8	40		8	40	µA
	f_{SAMPLE} = 7.5kHz		0.8			0.8			0.8		µA
	$\overline{CS}$ = V_{CC}		0.001	3		0.001	3		0.001	3	µA
DIGITAL INPUT/OUTPUT											
Logic Family			CMOS			CMOS			CMOS		
Logic Levels:											
V_{IH}	I_{IH} = +5µA	2.0		5.5	2.0		5.5	2.0		5.5	V
V_{IL}	I_{IL} = +5µA	–0.3		0.8	–0.3		0.8	–0.3		0.8	V
V_{OH}	I_{OH} = –250µA	2.1			2.1			2.1			V
V_{OL}	I_{OL} = 250µA			0.4			0.4			0.4	V
Data Format		Straight Binary			Straight Binary			Straight Binary			
POWER SUPPLY REQUIREMENTS											
V_{CC}	Specified Performance	2.7		3.6	2.7		3.6	2.7		3.6	V
	See Notes 2 and 3	2.0		2.7	2.0		2.7	2.0		2.7	V
	See Note 3	3.6		5.25	3.6		5.25	3.6		5.25	V
Quiescent Current			200	325		200	325		200	325	µA
	f_{SAMPLE} = 7.5kHz[4,5]		20			20			20		µA
	f_{SAMPLE} = 75kHz[5]		180			180			180		µA
Power Down	$\overline{CS}$ = V_{CC}			3			3			3	µA
TEMPERATURE RANGE											
Specified Performance		–40		+85	–40		+85	–40		+85	°C

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 0.61mV.
(2) The maximum clock rate of the ADS7822 is less than 1.2MHz in this power supply range.
(3) See the Typical Performance Curves for more information.
(4) f_{CLK} = 1.2MHz, $\overline{CS}$ = V_{CC} for 145 clock cycles out of every 160.
(5) See the Power Dissipation section for more information regarding lower sample rates.

SPECIFICATIONS: $+V_{CC}$ = +5V

At –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7822 MIN	ADS7822 TYP	ADS7822 MAX	ADS7822B MIN	ADS7822B TYP	ADS7822B MAX	UNITS
ANALOG INPUT								
Full-Scale Input Span	+In – (–In)	0		V_{REF}	0		V_{REF}	V
Absolute Input Range	+In	–0.2		V_{CC} +0.2	–0.2		V_{CC} +0.2	V
	–In	–0.2		+1.0	–0.2		+1.0	V
Capacitance			25			25		pF
Leakage Current			±1			±1		µA
SYSTEM PERFORMANCE								
Resolution			12			12		Bits
No Missing Codes		11			12			Bits
Integral Linearity Error		–2		+2	–1		+1	LSB[1]
Differential Linearity Error			±0.8		–1	±0.5	+1	LSB
Offset Error		–3		+3	–3		+3	LSB
Gain Error		–4		+4	–3		+3	LSB
Noise			33			33		µVrms
Power Supply Rejection			70			70		dB
SAMPLING DYNAMICS								
Conversion Time				12			12	Clk Cycles
Acquisition Time		1.5			1.5			Clk Cycles
Throughput Rate				200			200	kHz
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion	V_{IN} = 5Vp-p at 10kHz		–78			–78		dB
SINAD	V_{IN} = 5Vp-p at 10kHz		71			71		dB
Spurious Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz		79			79		dB
REFERENCE INPUT								
Voltage Range		0.05		V_{CC}	0.05		V_{CC}	V
Resistance	$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			5		GΩ
	$\overline{CS}$ = V_{CC}		5			5		GΩ
Current Drain	At Code 710h		40	100		40	100	µA
	f_{SAMPLE} = 12.5kHz		2.5			2.5		µA
	$\overline{CS}$ = V_{CC}		0.001	3		0.001	3	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			CMOS		
Logic Levels:								
V_{IH}	I_{IH} = +5µA	3.0		5.5	3.0		5.5	V
V_{IL}	I_{IL} = +5µA	–0.3		0.8	–0.3		0.8	V
V_{OH}	I_{OH} = –250µA	3.5			3.5			V
V_{OL}	I_{OL} = 250µA			0.4			0.4	V
Data Format			Straight Binary			Straight Binary		
POWER SUPPLY REQUIREMENTS								
V_{CC}	Specified Performance	4.5		5.25	4.75		5.25	V
Quiescent Current	f_{SAMPLE} = 200kHz		320	550		320	550	µA
Power Down	$\overline{CS}$ = V_{CC}			3			3	µA
TEMPERATURE RANGE								
Specified Performance		–40		+85	–40		+85	°C

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +5V, one LSB is 1.22mV.

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC}	+6V
Analog Input	–0.3V to (V_{CC} + 0.3V)
Logic Input	–0.3V to 6V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Reference Voltage	+5.5V

NOTE: (1) Stresses above these ratings may permanently damage the device.

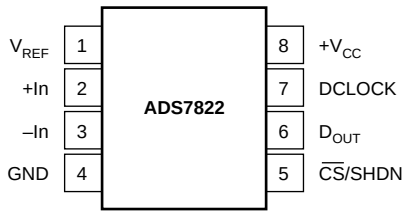
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Texas Instruments recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION

Top View **DIP, MSOP, SO**



PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	V_{REF}	Reference Input.
2	+In	Non Inverting Input.
3	–In	Inverting Input. Connect to ground or to remote ground sense point.
4	GND	Ground.
5	$\overline{CS}$/SHDN	Chip Select when LOW, Shutdown Mode when HIGH.
6	D_{OUT}	The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 edges.
7	DCLOCK	Data Clock synchronizes the serial data transfer and determines conversion speed.
8	+V_{CC}	Power Supply.

PACKAGE/ORDERING INFORMATION(1)

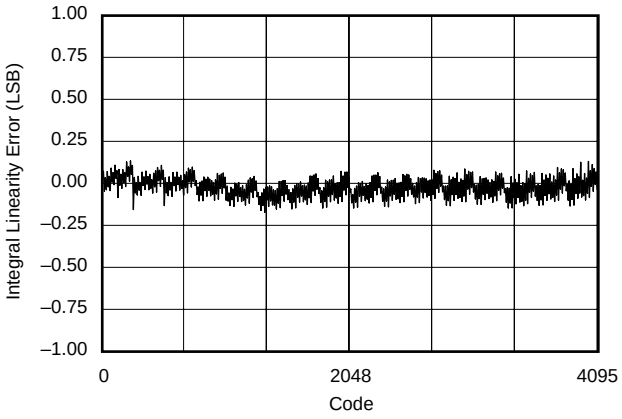
PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)	PACKAGE	PACKAGE DESIGNATOR	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING(2)	ORDERING NUMBER(3)	TRANSPORT MEDIA
ADS7822E	±2	±2	MSOP-8	DGK	–40°C to +85°C	A22	ADS7822E/250	Tape and Reel
ADS7822E	"	"	"	"	"	"	ADS7822E/2K5	"
ADS7822EB	±1	±1	MSOP-8	DGK	–40°C to +85°C	A22	ADS7822EB/250	Tape and Reel
ADS7822EB	"	"	"	"	"	"	ADS7822EB/2K5	"
ADS7822EC	±0.75	±0.75	MSOP-8	DGK	–40°C to +85°C	A22	ADS7822EC/250	Tape and Reel
ADS7822EC	"	"	"	"	"	"	ADS7822EC/2K5	"
ADS7822P	±2	±2	Plastic DIP-8	P	–40°C to +85°C	ADS7822P	ADS7822P	Rails
ADS7822PB	±1	±1	Plastic DIP-8	P	–40°C to +85°C	ADS7822PB	ADS7822PB	Rails
ADS7822PC	±0.75	±0.75	Plastic DIP-8	P	–40°C to +85°C	ADS7822PC	ADS7822PC	Rails
ADS7822U	±2	±2	SOIC-8	D	–40°C to +85°C	ADS7822U	ADS7822U	Rails
ADS7822U	"	"	"	"	"	"	ADS7822U/2K5	Tape and Reel
ADS7822UB	±1	±1	SOIC-8	D	–40°C to +85°C	ADS7822UB	ADS7822UB	Rails
ADS7822UB	"	"	"	"	"	"	ADS7822UB/2K5	Tape and Reel
ADS7822UC	±0.75	±0.75	SOIC-8	D	–40°C to +85°C	ADS7822UC	ADS7822UC	Rails
ADS7822UC	"	"	"	"	"	"	ADS7822UC/2K5	Tape and Reel

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Performance Grade information is marked on the reel.
(3) Models with a slash(/) are available only in tape and reel in quantities indicated (e.g. **/250** indicates 250 units per reel, **/2K5** indicates 2500 devices per reel). Ordering 2500 pieces of "ADS7822E/2K5" will get a single 2500-piece tape and reel.

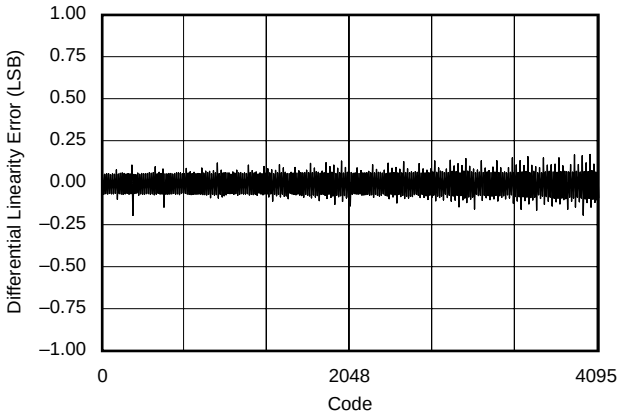
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 75kHz, f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

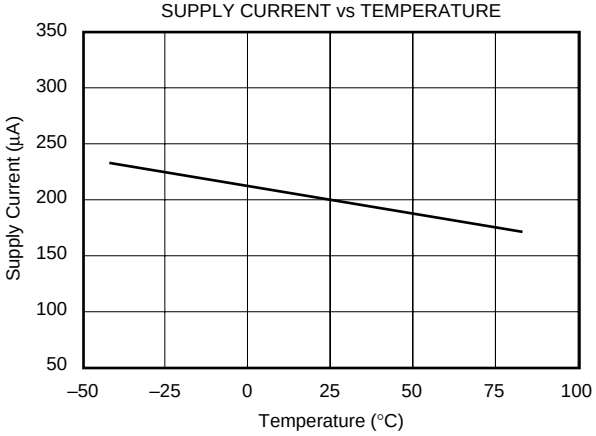
INTEGRAL LINEARITY ERROR vs CODE



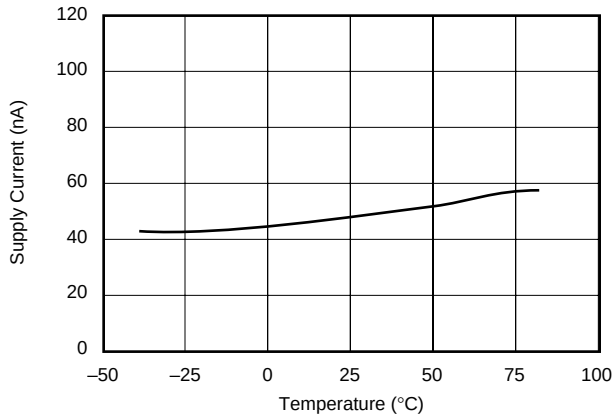
DIFFERENTIAL LINEARITY ERROR vs CODE



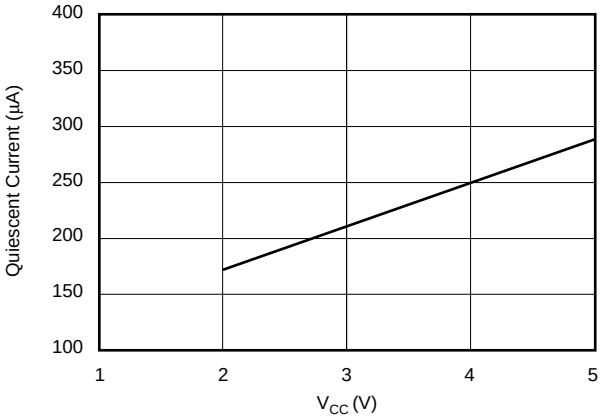
SUPPLY CURRENT vs TEMPERATURE



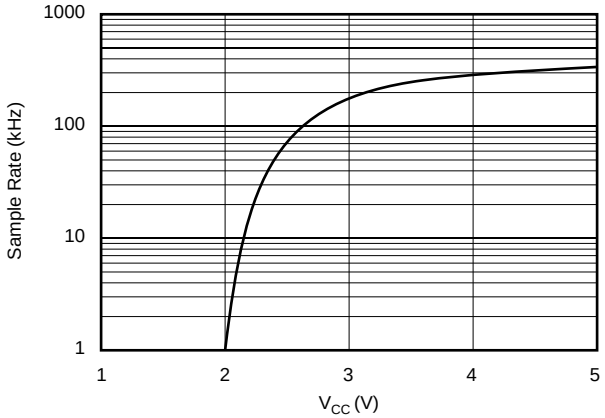
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs V_{CC}



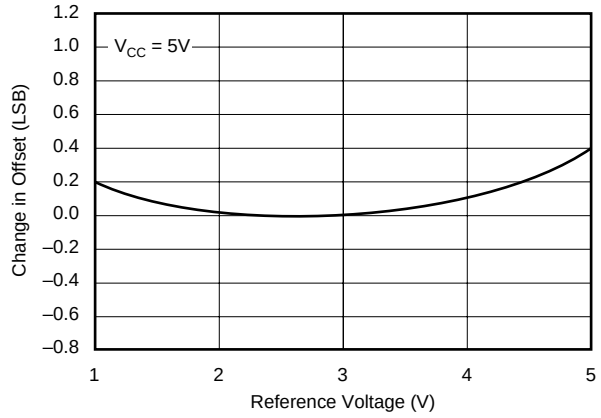
MAXIMUM SAMPLE RATE vs V_{CC}



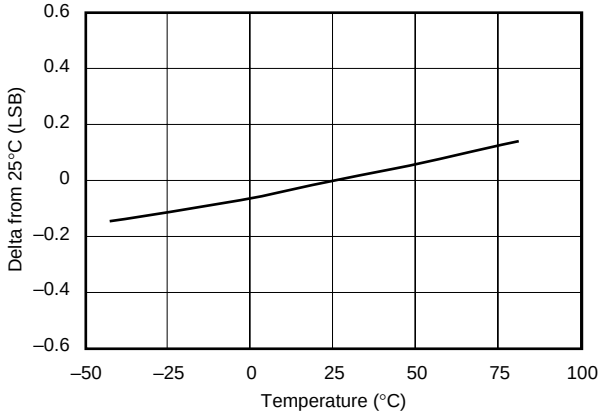
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_{CC} = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 75kHz, f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

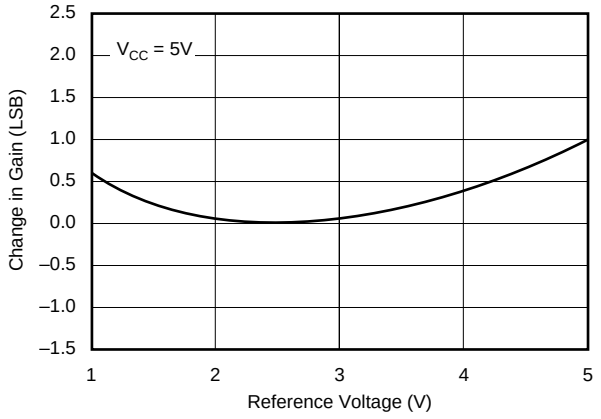
CHANGE IN OFFSET vs REFERENCE VOLTAGE



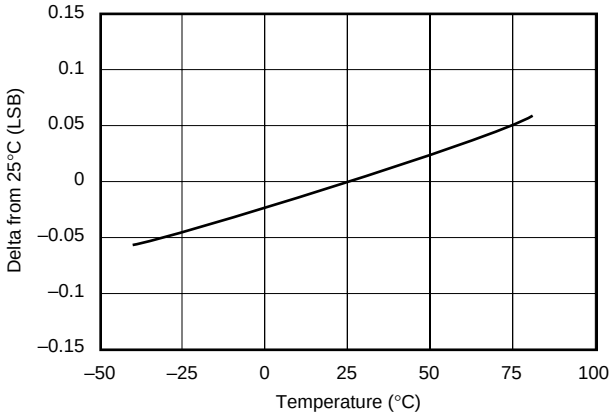
CHANGE IN OFFSET vs TEMPERATURE



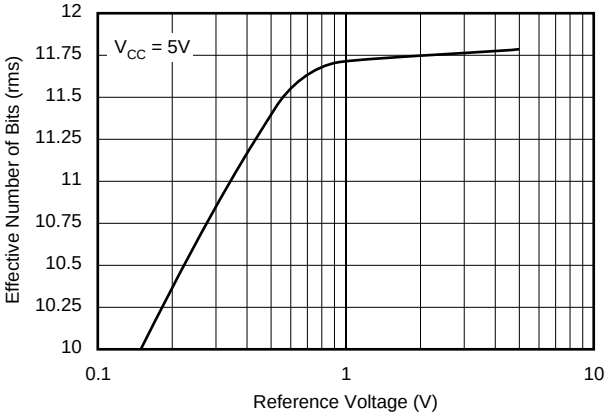
CHANGE IN GAIN vs REFERENCE VOLTAGE



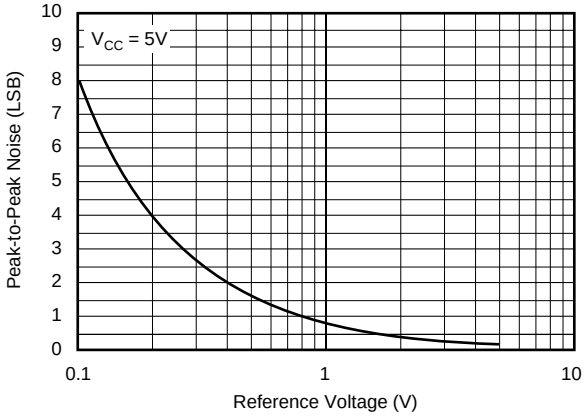
CHANGE IN GAIN vs TEMPERATURE



EFFECTIVE NUMBER OF BITS
vs REFERENCE VOLTAGE



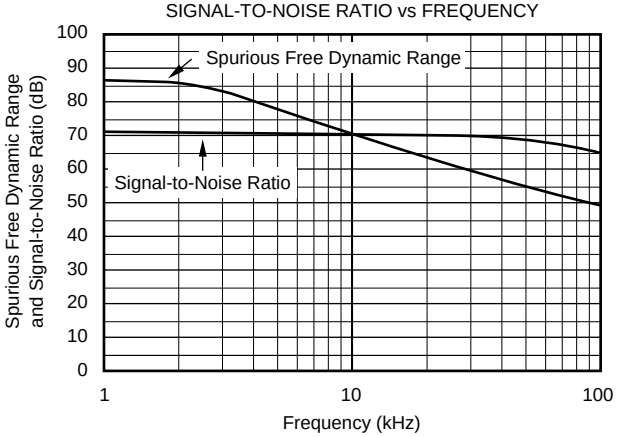
PEAK-TO-PEAK NOISE vs REFERENCE VOLTAGE



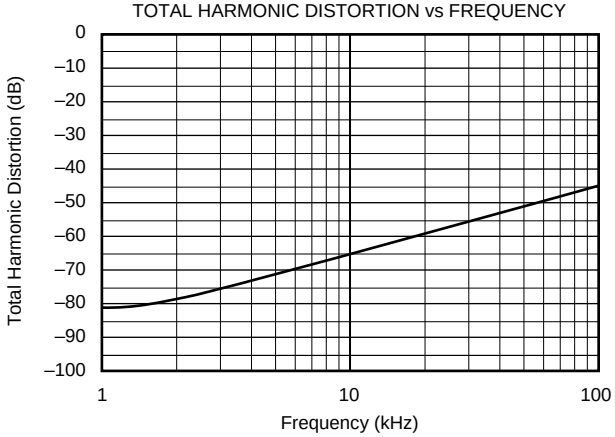
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_{CC} = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 75kHz, f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

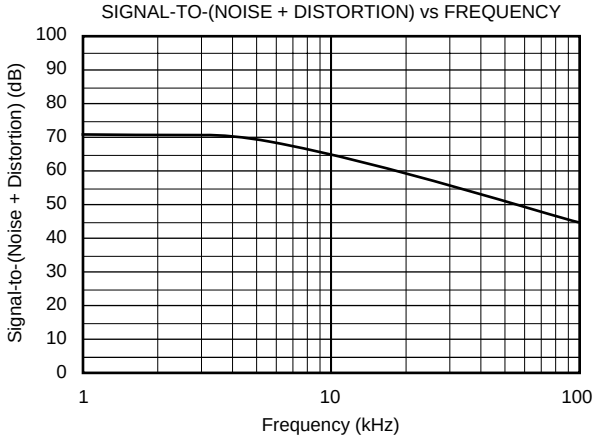
SPURIOUS FREE DYNAMIC RANGE and SIGNAL-TO-NOISE RATIO vs FREQUENCY



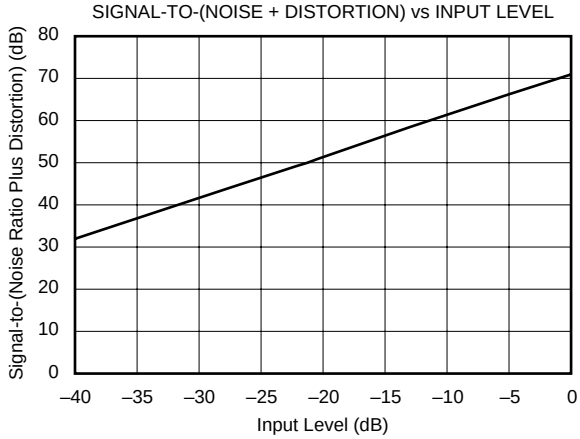
TOTAL HARMONIC DISTORTION vs FREQUENCY



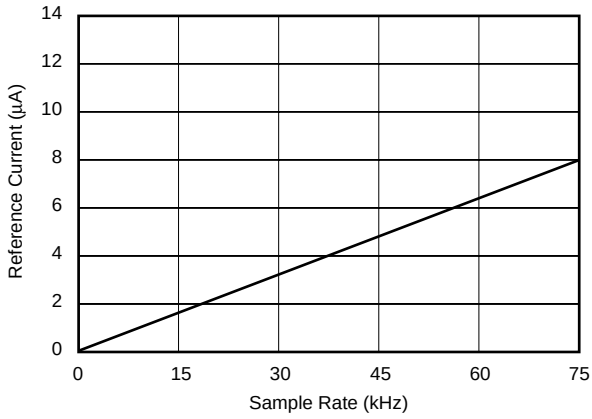
SIGNAL-TO-(NOISE + DISTORTION) vs FREQUENCY



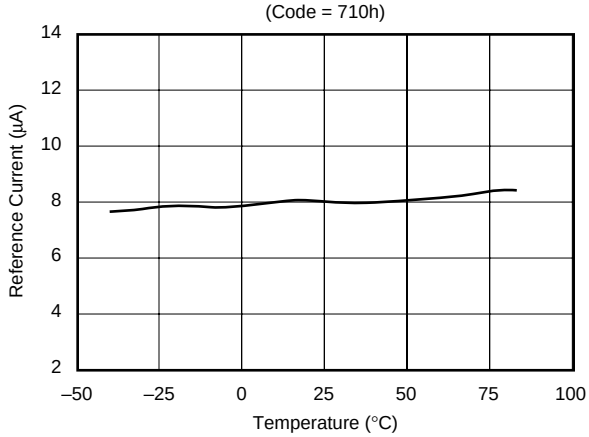
SIGNAL-TO-(NOISE + DISTORTION) vs INPUT LEVEL



REFERENCE CURRENT vs SAMPLE RATE



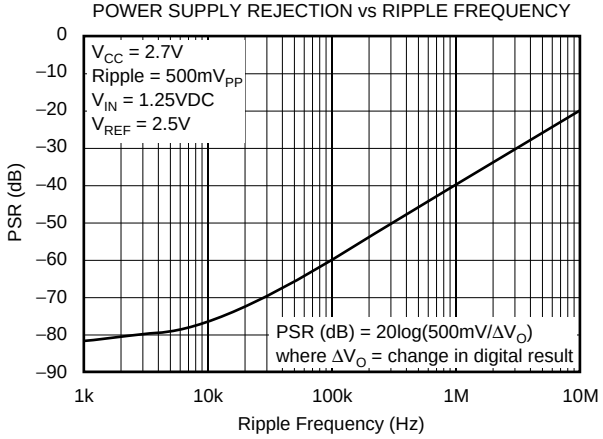
REFERENCE CURRENT vs TEMPERATURE (Code = 710h)



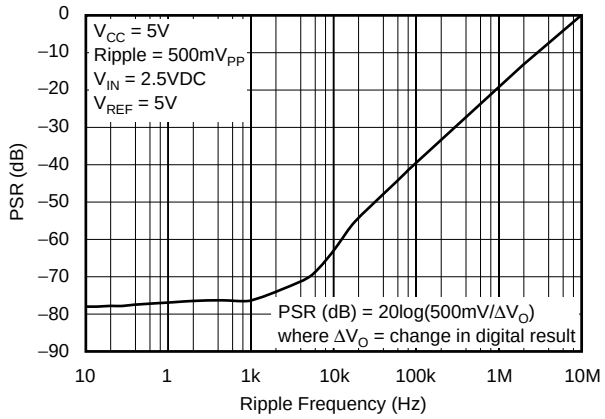
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_{CC} = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 75kHz, f_{CLK} = 16 • f_{SAMPLE}, unless otherwise specified.

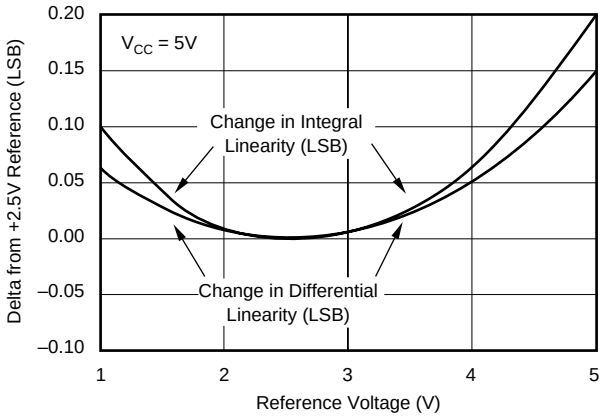
POWER SUPPLY REJECTION vs RIPPLE FREQUENCY



POWER SUPPLY REJECTION vs RIPPLE FREQUENCY



CHANGE IN INTEGRAL LINEARITY AND DIFFERENTIAL LINEARITY vs REFERENCE VOLTAGE



THEORY OF OPERATION

The ADS7822 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µ CMOS process. The architecture and process allow the ADS7822 to acquire and convert an analog signal at up to 75,000 conversions per second while consuming very little power.

The ADS7822 requires an external reference, an external clock, and a single power source (V_{CC}). The external reference can be any voltage between 50mV and V_{CC}. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS7822.

The external clock can vary between 10kHz (625Hz throughput) and 1.2MHz (75kHz throughput). The duty cycle of the clock is essentially unimportant as long as the minimum high and low times are at least 400ns (V_{CC} = 2.7V or greater). The minimum clock frequency is set by the leakage on the capacitors internal to the ADS7822.

The analog input is provided to two input pins: +In and –In. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS7822 after the conversion is complete and to obtain the serial data least significant bit first. See the digital timing section for more information.

ANALOG INPUT

The +In and –In input pins allow for a pseudo-differential input signal. Unlike some converters of this type, the –In input is not re-sampled later in the conversion cycle. When the converter goes into the hold mode, the voltage difference between +In and –In is captured on the internal capacitor array.

The range of the –In input is limited to –0.2V to +1V. Because of this, the differential input can be used to reject only small signals that are common to both inputs. Thus, the –In input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power-down mode. Essentially, the current into the ADS7822 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to a 12-bit settling level within 1.5 clock cycles. When the converter goes into the hold mode or while it is in the power down mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the –In input should not drop below GND – 200mV or exceed GND + 1V. The +In input should always remain within the range of GND – 200mV to V_{CC} + 200mV. Outside of these ranges, the converter's linearity may not meet specifications.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7822 will operate with a reference in the range of 50mV to V_{CC}. There are several important implications of this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 2.5V reference, the internal noise of the converter typically contributes only 0.32 LSB peak-to-peak of potential error to the output code. When the external reference is 50mV, the potential error contribution from the internal noise will be 50 times larger—16 LSBs. The errors due to the internal noise are gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult the typical performance curves "Effective Number of Bits vs Reference Voltage" and "Peak-to-Peak Noise vs Reference Voltage." Note that the effective number of bits (ENOB) figure is calculated based on the converter's signal-to-(noise + distortion) ratio with a 1kHz, 0dB input signal. SINAD is related to ENOB as follows

$$SINAD = 6.02 \bullet ENOB + 1.76$$

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to external sources of error such as nearby digital signals and electromagnetic interference.

DIGITAL INTERFACE

SIGNAL LEVELS

The digital inputs of the ADS7822 can accommodate logic levels up to 6V regardless of the value of V_{CC}. Thus, the ADS7822 can be powered at 3V and still accept inputs from logic powered at 5V.

The CMOS digital output (D_{OUT}) will swing 0V to V_{CC}. If V_{CC} is 3V and this output is connected to a 5V CMOS logic input, then that IC may require more supply current than normal and may have a slightly longer propagation delay.

SERIAL INTERFACE

The ADS7822 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface as shown in Figure 1 and Table I. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

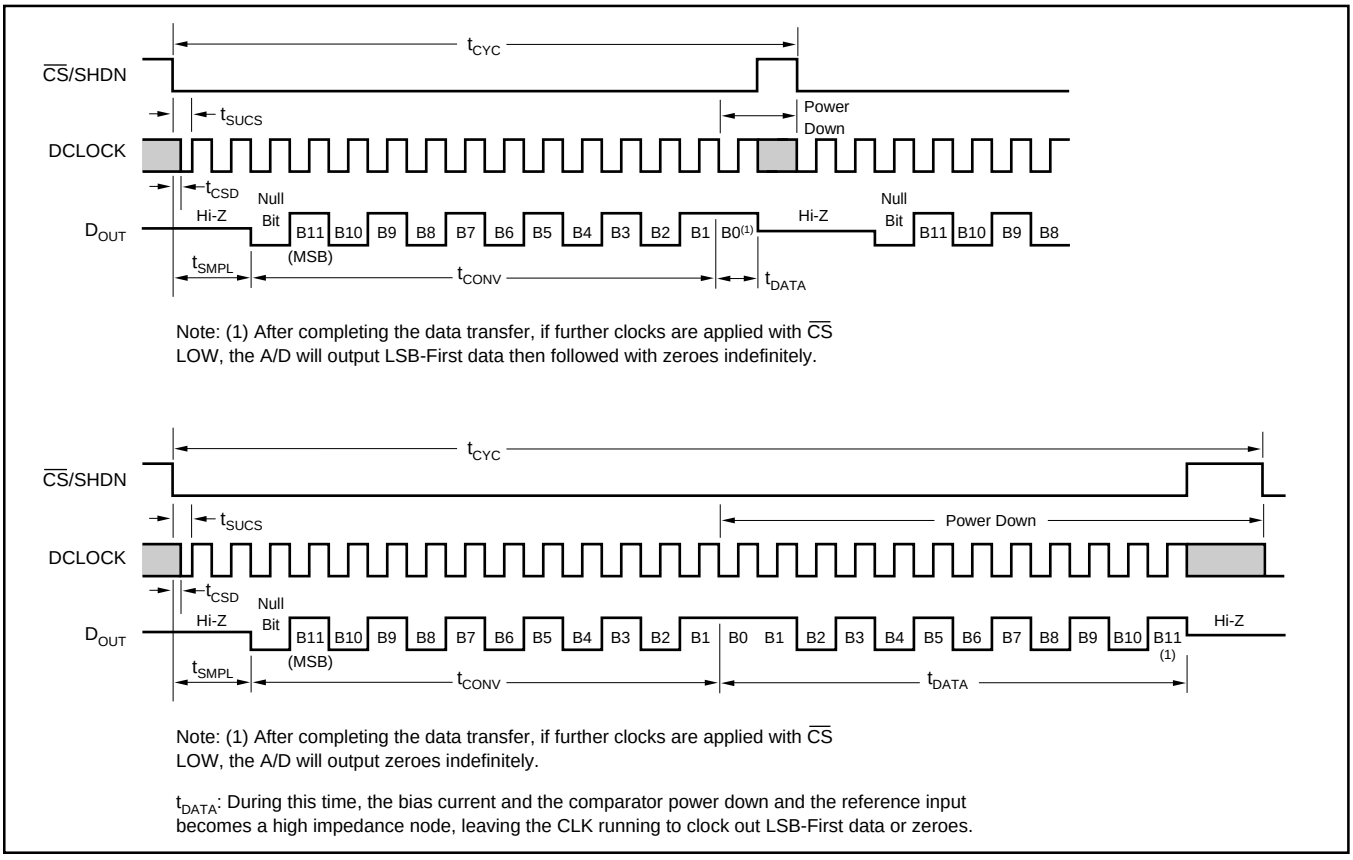


FIGURE 1. ADS7822 Basic Timing Diagrams.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	1.5		2.0	Clk Cycles
t_{CONV}	Conversion Time		12		Clk Cycles
t_{CYC}	Throughput Rate			75	kHz
t_{CSD}	$\overline{CS}$ Falling to DCLOCK LOW			0	ns
t_{SUCS}	$\overline{CS}$ Falling to DCLOCK Rising	30			ns
t_{hDO}	DCLOCK Falling to Current D_{OUT} Not Valid	15			ns
t_{dDO}	DCLOCK Falling to Next D_{OUT} Valid		130	200	ns
t_{dis}	$\overline{CS}$ Rising to D_{OUT} Tri-State		40	80	ns
t_{en}	DCLOCK Falling to D_{OUT} Enabled		75	175	ns
t_f	D_{OUT} Fall Time		90	200	ns
t_r	D_{OUT} Rise Time		110	200	ns

TABLE I. Timing Specifications (V_{CC} = 2.7V and above, –40°C to +85°C.

A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 1.5 to 2.0 clock periods of the conversion cycle are used to sample the input signal. After the second falling DCLOCK edge, D_{OUT} is enabled and will output a LOW value for one clock period. For the next 12 DCLOCK periods, D_{OUT} will output the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks will repeat the output data but in a least significant bit first format.

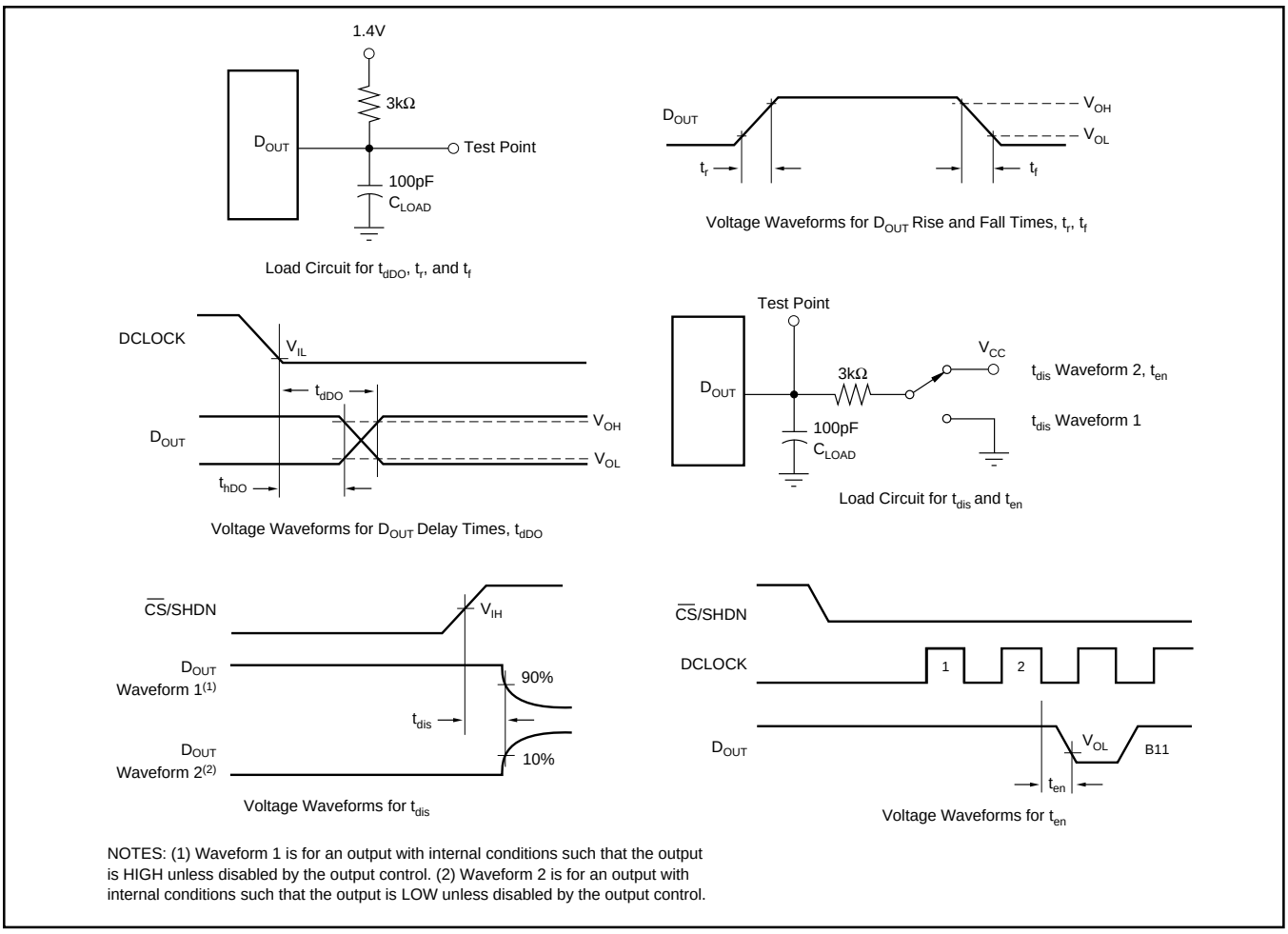
After the most significant bit (B11) has been repeated, D_{OUT} will tri-state. Subsequent clocks will have no effect on the converter. A new conversion is initiated only when $\overline{CS}$ has been taken HIGH and returned LOW.

DATA FORMAT

The output data from the ADS7822 is in straight binary format as shown in Table II. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise.

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Full Scale Range	V_{REF}		
Least Significant Bit (LSB)	V_{REF}/4096		
Full Scale	V_{REF} –1 LSB	1111 1111 1111	FFF
Midscale	V_{REF}/2	1000 0000 0000	800
Midscale – 1 LSB	V_{REF}/2 – 1 LSB	0111 1111 1111	7FF
Zero	0V	0000 0000 0000	000

TABLE II. Ideal Input Voltages and Output Codes.



NOTES: (1) Waveform 1 is for an output with internal conditions such that the output is HIGH unless disabled by the output control. (2) Waveform 2 is for an output with internal conditions such that the output is LOW unless disabled by the output control.

FIGURE 2. Timing Diagrams and Test Circuits for the Parameters in Table I.

POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design allow the ADS7822 to convert at up to a 75kHz rate while requiring very little power. Still, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS7822 scales directly with conversion rate. So, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that will satisfy the requirements of the system.

In addition, the ADS7822 is in power-down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is HIGH (see Figure 1). Ideally, each conversion should occur as quickly as possible, preferably at a 1.2MHz clock rate. This way, the converter spends the longest possible time in the power-down mode. This is very important as the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components) but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously, until the power-down mode is entered.

Figure 3 shows the current consumption of the ADS7822 versus sample rate. For this graph, the converter is clocked at 1.2MHz regardless of the sample rate—$\overline{CS}$ is HIGH for the remaining sample period. Figure 4 also show current consumption versus sample rate. However, in this case, the DCLOCK period is 1/16th of the sample period—$\overline{CS}$ is HIGH for one DCLOCK cycle out of every 16.

There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode that is enabled when $\overline{CS}$ is HIGH. While both shutdown the analog section, the digital section is completely shutdown only when $\overline{CS}$ is HIGH. Thus, if $\overline{CS}$ is left LOW at the end of a conversion and the converter is continually clocked, the power consumption will not be as low as when $\overline{CS}$ is HIGH. See Figure 5 for more information.

Power dissipation can also be reduced by lowering the power supply voltage and the reference voltage. The ADS7822 will operate over a V_{CC} range of 2.0V to 5.25V. However, at voltages below 2.7V, the converter will not run at a 75kHz sample rate. See the typical performance curves for more information regarding power supply voltage and maximum sample rate.

SHORT CYCLING

Another way of saving power is to utilize the $\overline{CS}$ signal to short-cycle the conversion. Because the ADS7822 places the latest data bit on the D_{OUT} line as it is generated, the converter can easily be short-cycled. This term means that the conversion can be terminated at any time. For example, if only 8 bits of the conversion result are needed, then the conversion can be terminated (by pulling $\overline{CS}$ HIGH) after the 8th bit has been clocked out.

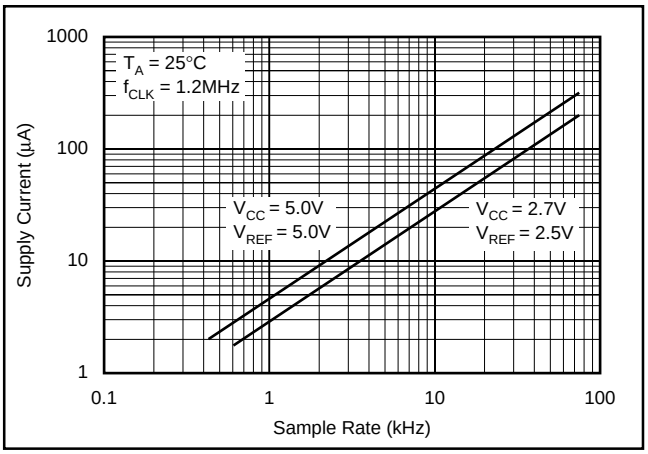


FIGURE 3. Maintaining f_{CLK} at the Highest Possible Rate Allows Supply Current to Drop Linearly with Sample Rate.

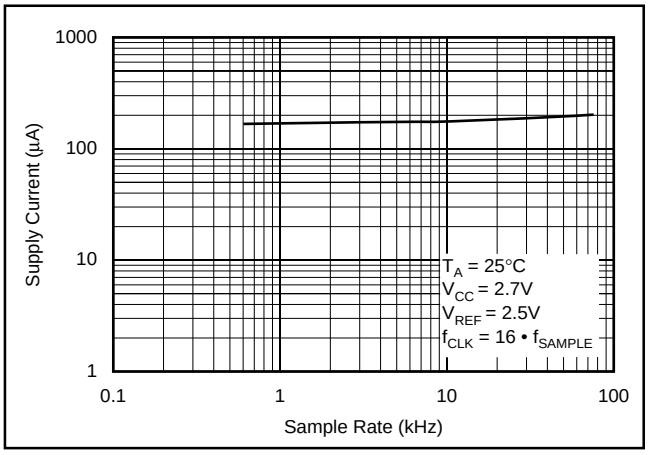


FIGURE 4. Scaling f_{CLK} Reduces Supply Current Only Slightly with Sample Rate.

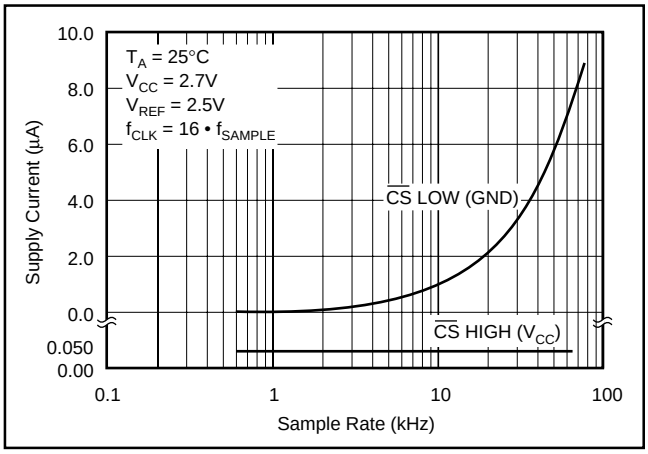


FIGURE 5. Shutdown Current with $\overline{CS}$ HIGH is 50nA Typically, Regardless of the Clock. Shutdown Current with $\overline{CS}$ LOW Varies with Sample Rate.

This technique can be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 12-bit conversion result may not be needed. If so, the conversion can be terminated after the first n-bits, where n might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system, as they spend more time in the power-down mode.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7822 circuitry. This will be particularly true if the reference voltage is low and/or the conversion rate is high. At a 75kHz conversion rate, the ADS7822 makes a bit decision every 830ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 12-bit level all within one clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter's DCLOCK signal—as the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS7822 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the ADS7822 package as possible. In addition, a 1 to 10µF capacitor and a 5Ω or 10Ω series resistor may be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1µF capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op amp, be careful that the op amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS7822 draws very little current from the reference on average, there are still instantaneous current demands placed on the external reference circuitry.

Also, keep in mind that the ADS7822 offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50Hz or 60Hz), can be difficult to remove.

The GND pin on the ADS7822 should be placed on a clean ground point. In many cases, this will be the "analog" ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power supply connection point. The ideal layout will include an analog ground plane for the converter and associated analog circuitry.

APPLICATION CIRCUITS

Figures 6 and 7 show some typical application circuits for the ADS7822. Figure 6 uses an ADS7822 and a multiplexer to provide for a flexible data acquisition circuit. A resistor string provides for various voltages at the multiplexer input. The selected voltage is buffered and driven into V_{REF}. As shown in Figure 6, the input range of the ADS7822 is programmable to 100mV, 200mV, 300mV, or 400mV. The 100mV range would be useful for sensors such as the thermocouple shown.

Figure 7 shows a basic data acquisition system. The ADS7822 input range is 0V to V_{CC}, as the reference input is connected directly to the power supply. The 5Ω resistor and 1µF to 10µF capacitor filter the microcontroller "noise" on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of the noise.

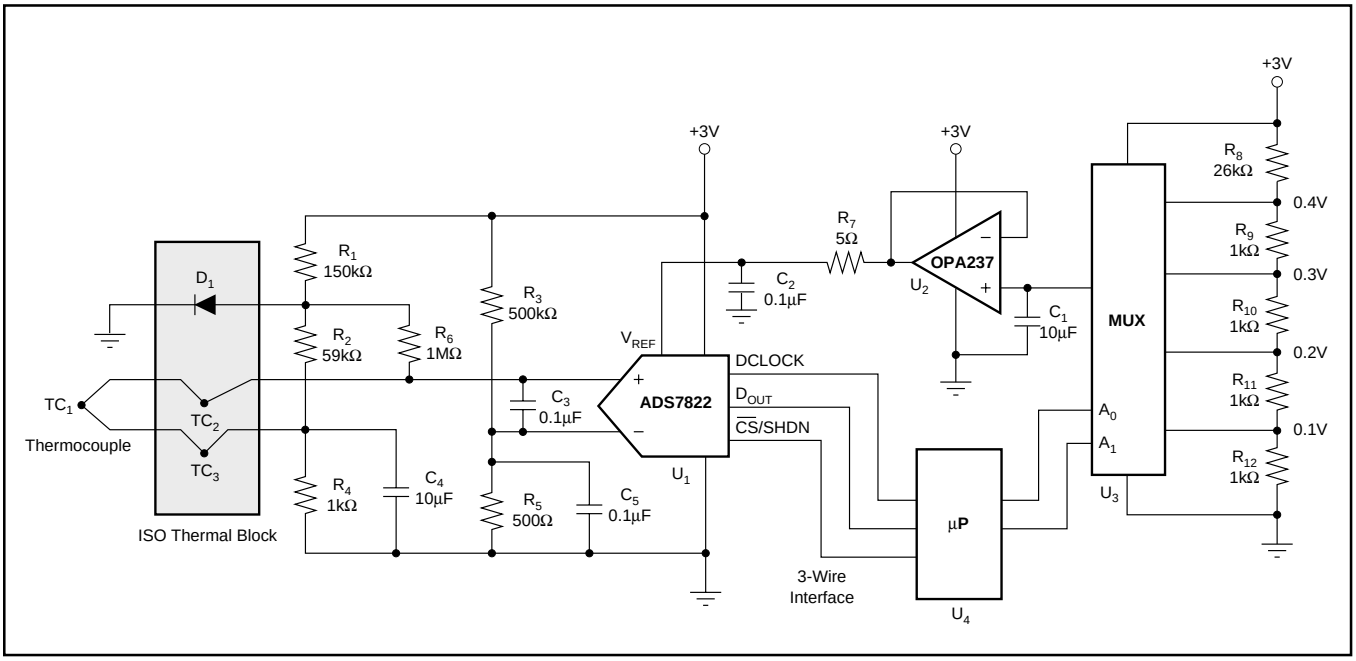


FIGURE 6. Thermocouple Application Using a MUX to Scale the Input Range of the ADS7822.

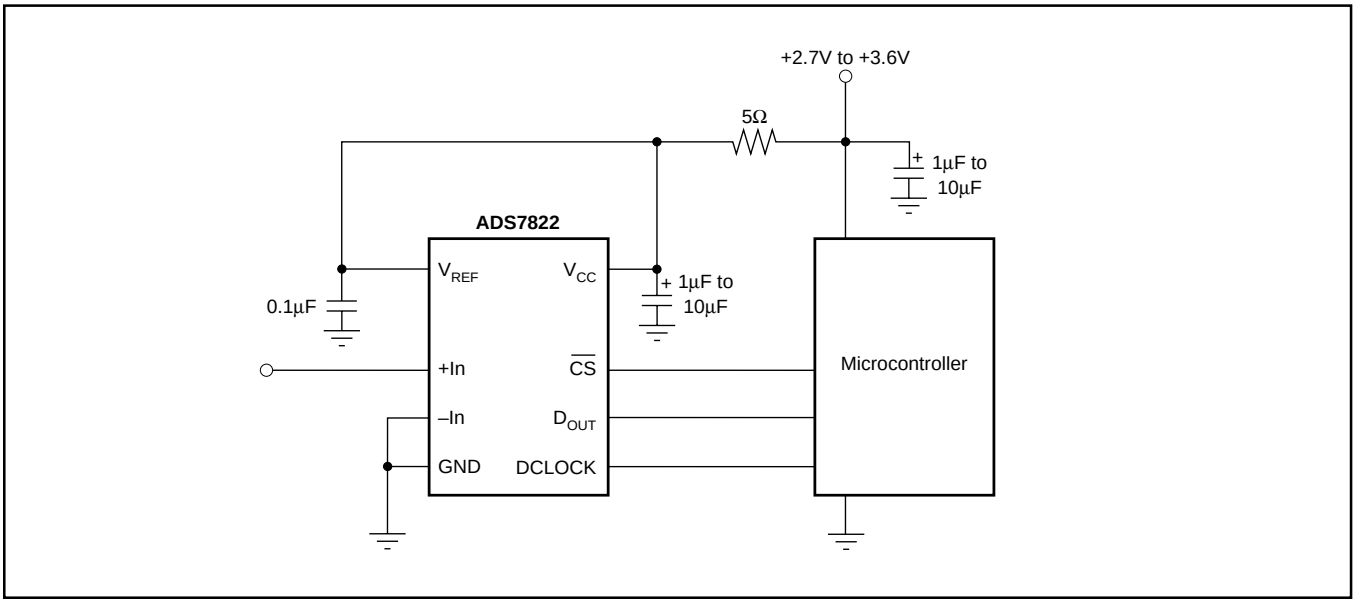


FIGURE 7. Basic Data Acquisition System.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS7822E/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822E/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822E/2K5G4	ACTIVE	MSOP	DGK	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
ADS7822EB/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822EB/250G4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822EB/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822EB/2K5G4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822EC/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822EC/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822EC/2K5G4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822P	ACTIVE	PDIP	P	8	50	TBD	Call TI	Level-NA-NA-NA
ADS7822PB	ACTIVE	PDIP	P	8	50	TBD	Call TI	Level-NA-NA-NA
ADS7822PC	ACTIVE	PDIP	P	8	50	TBD	Call TI	Level-NA-NA-NA
ADS7822U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822UB	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822UB/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822UC	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822UC/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822UC/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS7822UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check

http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

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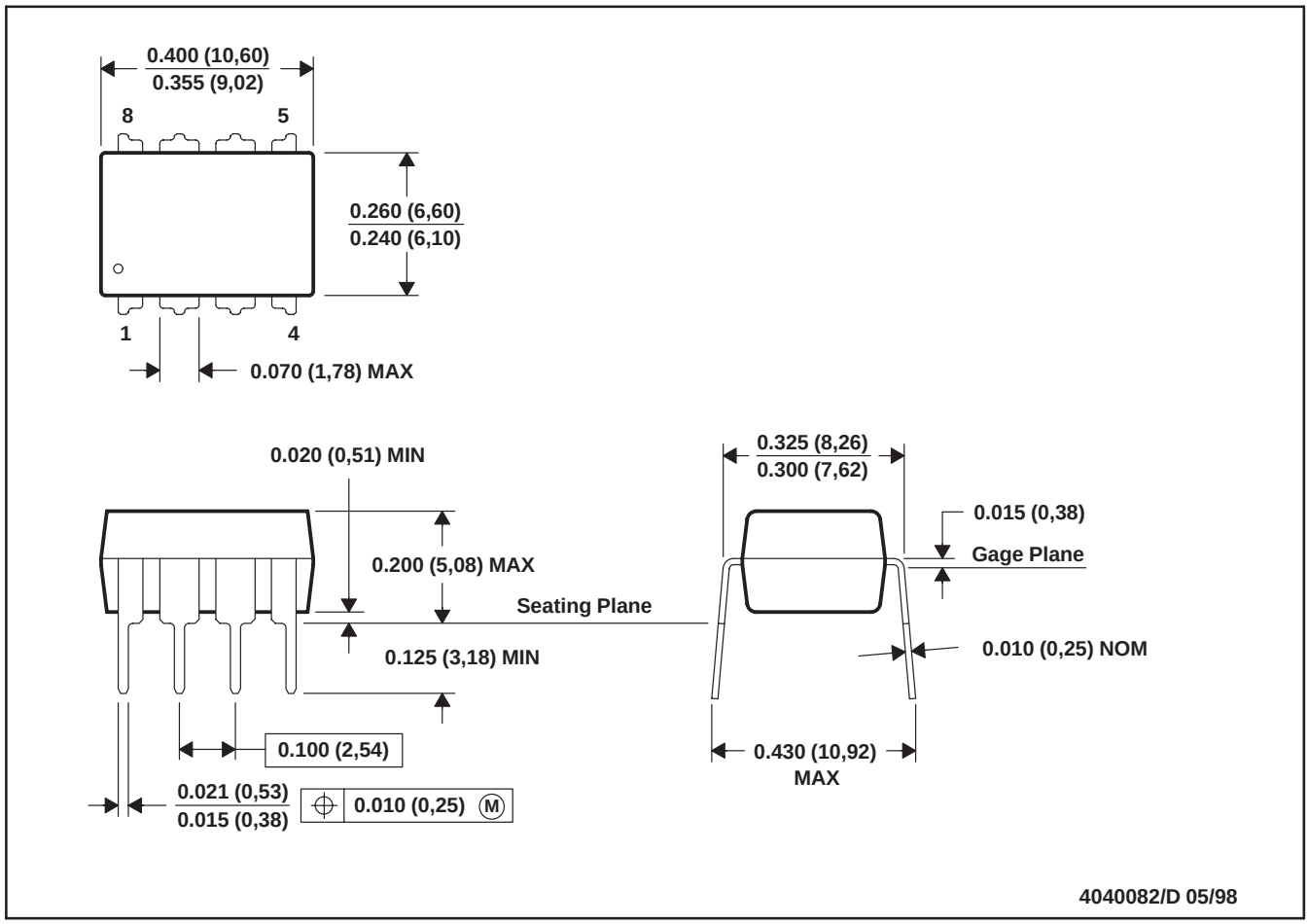

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

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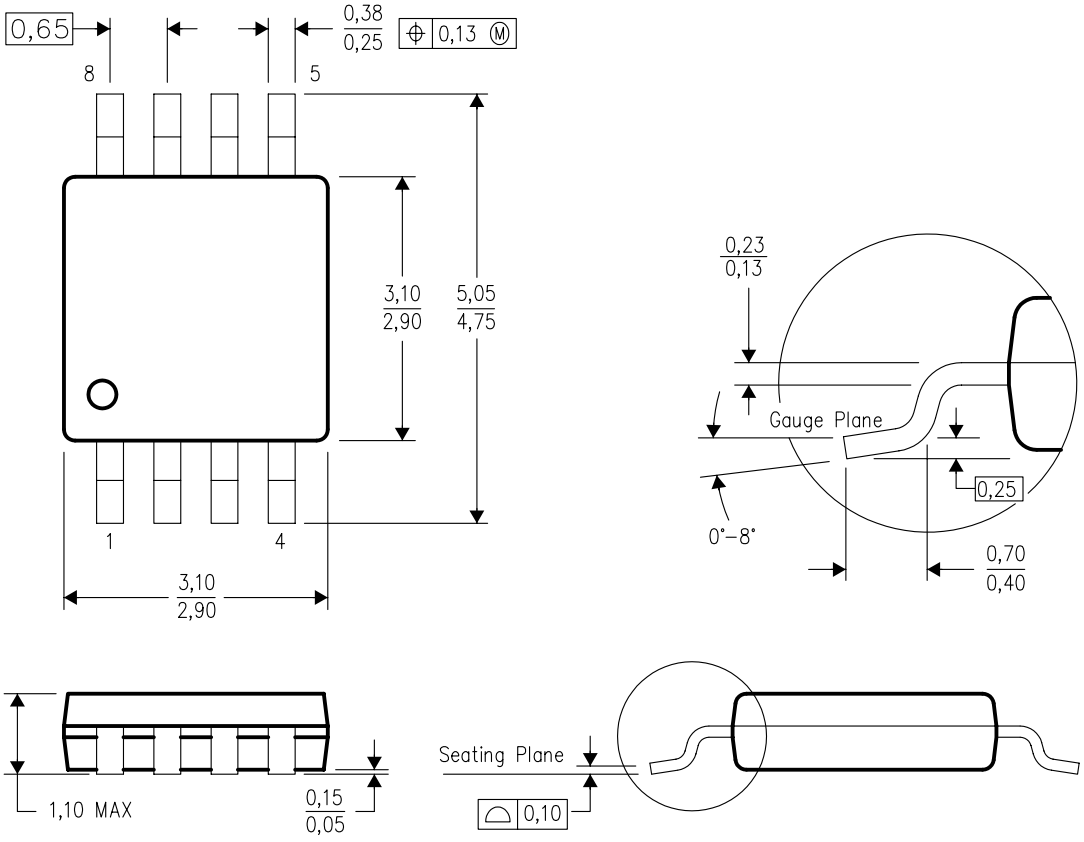
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/D 12/03

NOTES:
A. All linear dimensions are in millimeters.
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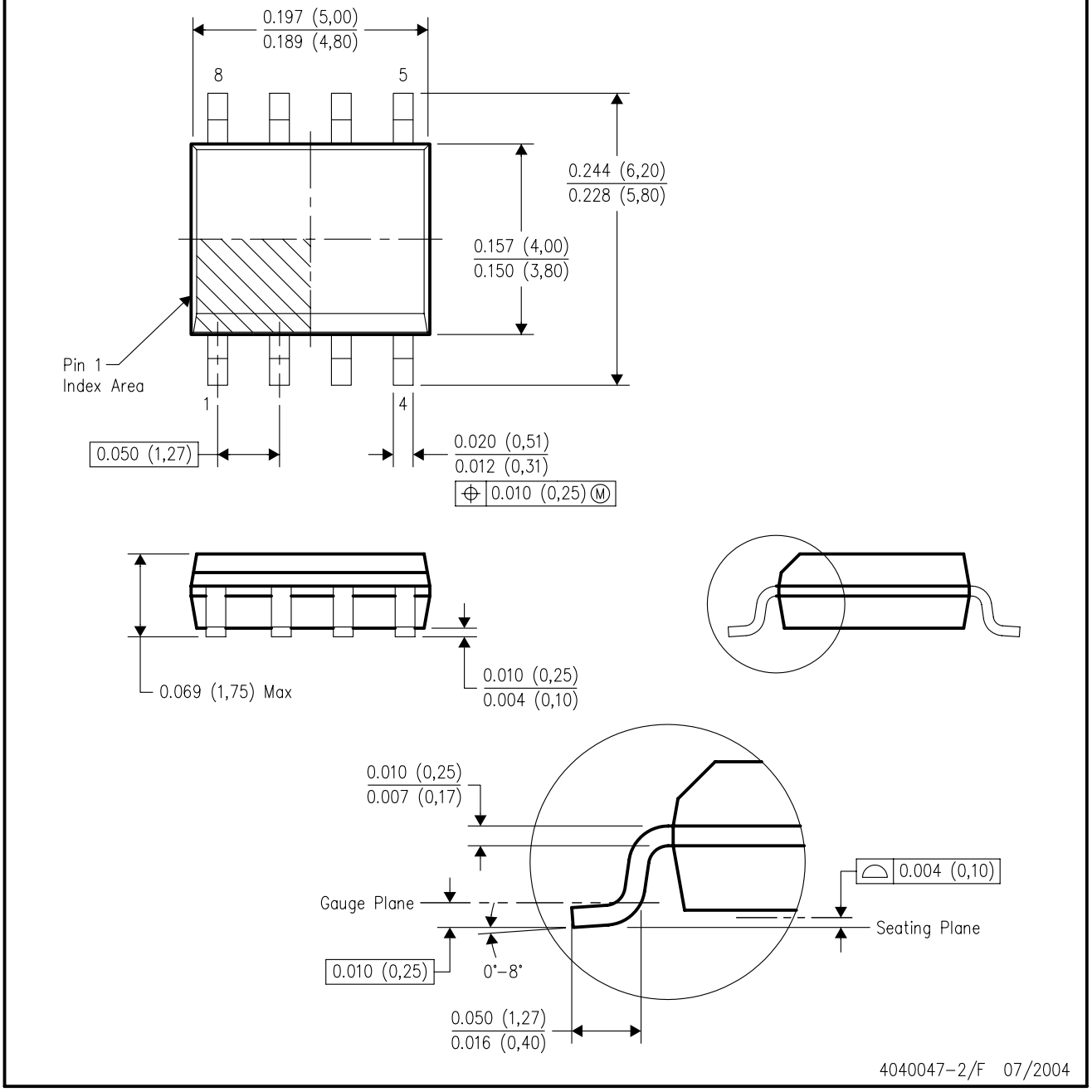
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation AA.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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